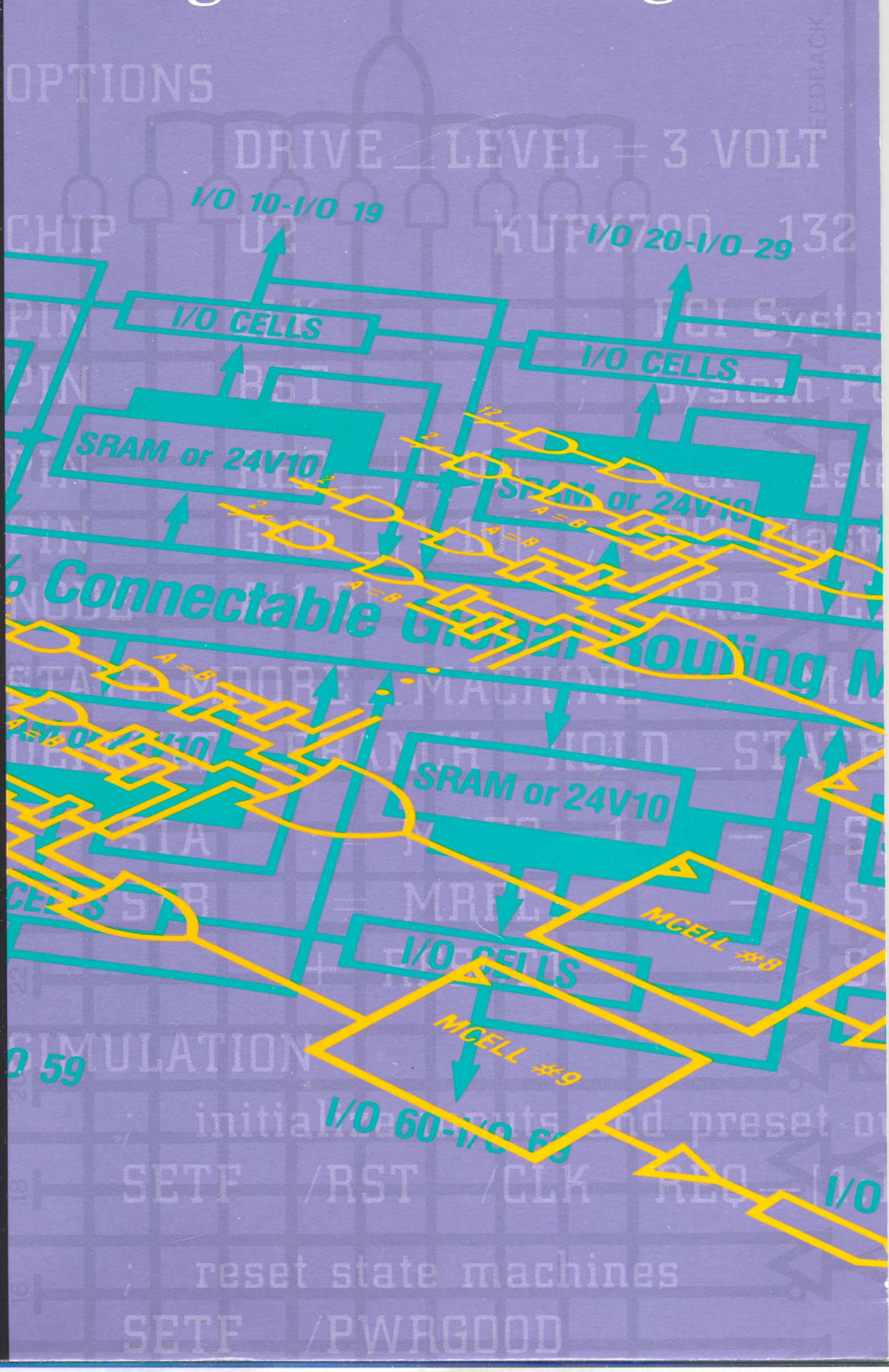
Programmable Logic

FLEXlogic FPGA's

High Performance PLDs



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Programmable Logic

In 1985, Intel began supplying programmable logic devices with a series of 1.5 micron CMOS PLDs. Four years later, Intel introduced the first members of its high-speed Programmable Logic Device (iPLD) family. With high speed, low power consumption, and a range of integration capabilities, these iPLDs are ideally suited for high-performance microcomputer system applications. Following growth and innovation on low density programmable logic devices, Intel has announced the FLEXlogic family of FPGA devices. As the Intel Programmable Logic family grows, it continues to present new opportunities for design innovation in high performance systems.

Intel's programmable logic devices provide a complete range of design entry, simulation compilation and programming tools. Intel PLDs – based on erasable programmable read-only memory for instant reconfiguration – offer designers the ability to customize their own system logic by tailoring the devices to meet performance requirements.

This handbook contains data sheets, application notes and technical papers for Intel's PLD family, including information on PLDshell Plus, the design software program used to design, compile and program Intel's PLDs.

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PROGRAMMABLE LOGIC

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Intel FPGAs and PLDs

Order Number: 296832-003

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Programmable Logic Overview

October 1993

Order Number: 296032-008

Programmable Logic Overview

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INTRODUCTION TO INTEL'S PLD FAMILY

In 1992, Intel introduced a new line of high-speed Programmable Logic Devices (iPLDs) aimed at augmenting high-performance microcomputer environments. This new family of devices provides high-speed support logic for the fast microcomputer systems of today. At the same time, our advanced CMOS process allows our PLDs to significantly reduce power consumption and system heat dissipation, problems that plagued the previous generation of bipolar PLDs.

Major benefits of Intel's iPLD family are:

Industry's Highest Speed PLDs	• High Speed — 100 MHz + Registered — < 7 ns t_{PD}
Specially Designed Register and Output Circuits	• Lowest Noise CMOS for Simplified High-Speed System Design • Best Solution for Metastable Conditions
Superset of Popular CMOS and Bipolar PLDs	• Compatible with Existing Design Methods • Fewer Manufacturing Line Items
Built on Standard CMOS EPROM Technology	• High Reliability/Quality — Lower Failure Rates — 100% Programming Yields

Intel's high-performance iPLDs, along with the existing 5CXXX family of devices, can be classified as "User-Defined Logic" circuits. User-defined logic circuits allow system designers to tailor building block solutions to their individual systems requirements. This customization provides the needed performance, reliability, and space reduction as well as design security.

This document discusses the reasons for the trend to user-defined logic devices, briefly describes some implementation alternatives, and provides detail on a solution that can be implemented completely by the user, i.e., the programmable logic device. Details on Intel's PLD product line, including terminology, nomenclature, architectural features, and developmental tools, are also described in this document.

WHY USER DEFINED LOGIC?

System designers prefer user customized ICs for the following reasons:

a. SMALLER SYSTEM SIZES: Customized components allow for reducing chip count and saving board space, resulting in smaller system physical dimensions.

b. LOWER SYSTEM COSTS: When custom LSI or VLSI components are used instead of standard SSI and MSI logic elements, there is a considerable saving in component cost per system, assembly and manufacturing cost, printed circuit board area and board costs and inventory costs.

c. HIGHER PERFORMANCE: Reduced number of ICs contributes to faster system speeds as well as lower power consumption.

d. HIGHER RELIABILITY: Since probability of failure is directly related to the number of ICs in the system, a system composed of customized LSI & VLSI chips is statistically much more reliable than the identical system made up of SSI/MSI devices.

e. DESIGN SECURITY: Systems designed with standard components can be replicated relatively easily whereas systems that contain user customized ICs cannot be copied because "reverse engineering" of the customized components is extremely difficult. Thus, use of customized ICs allows for the protection of proprietary designs.

f. INCREASED FLEXIBILITY: Customized components allow for the tailoring of systems to the end user's specific needs relatively easily. This also allows for upgradability and obsolescence protection.

USER DEFINED IC—IMPLEMENTATION ALTERNATIVES

Currently, the choices available to the system designer for customization of ICs (see Figure 1) are as follows:

(1) user programmable ICs—programmable logic devices, including Field Programmable Gate Arrays (FPGAs)

(2) mask programmable ICs—gate arrays

(3) standard cell based ICs

(4) full custom ICs

Alternatives (1) & (2) are usually called 'Semicustom' because in these methods only a few (less than three) of the mask layers involved in the manufacture of the IC, are customized to the users' specifications. The later two alternatives (3) & (4), involve customization of all mask layers required to manufacture the ICs to the users' specifications and are therefore called 'Custom'.

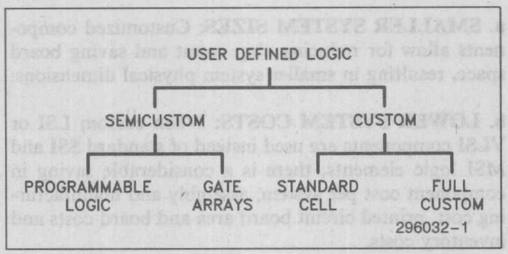

Figure 1. User-Defined Logic Implementation Choices

PROGRAMMABLE LOGIC

Most user Programmable Logic Devices (PLD) are internally structured as variations of the PLA (programmable logic array) architecture, that is composed of an array of 'AND' gates connected to an array of 'OR' gates (see Figure 2). Programmable logic devices make use of the fact that any logic equation can be converted to an equivalent 'Sum-of-Products' form and can thus be implemented in the 'AND' and 'OR' architecture. This basic PLA structure has been augmented in most PLDs with input and output blocks containing registers, latches and feedback options, that let the user implement sequential logic functions in addition to combinational logic.

The number and locations of the programmable connections between the 'AND' and 'OR' matrices as well as the input and output blocks are predetermined by the architecture of the PLD. The user, depending on his logic requirements, determines which of these connections he would like to remain open and which he would like to close, through the programming of the PLD. Programmability of these connections is achieved using various memory technologies such as fuses, EPROM cells, EEPROM cells or Static RAM cells (see Figure 3).

User programmability allows for instant customization, very similar to user programmable memories such as PROMs or EPROMs. The user can purchase a PLD off-the-shelf, use a development system running on a personal computer and, in a matter of a few hours, have customized silicon in his hands. Figure 4 compares user-defined logic alternatives.

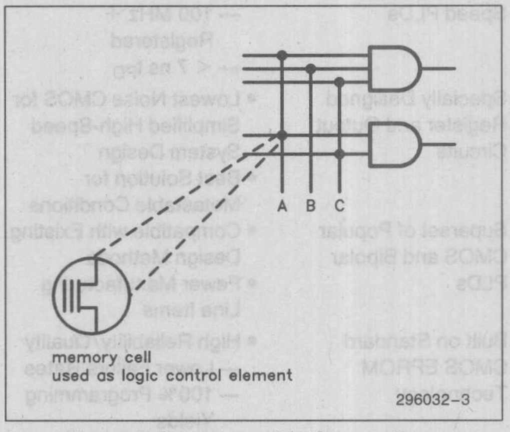

Figure 3. Programmable Connections

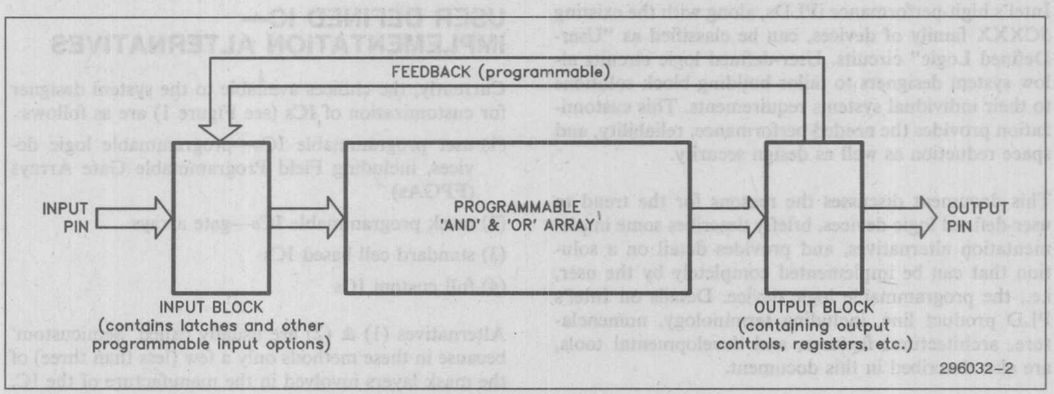

Figure 2. General Architecture of a PLD

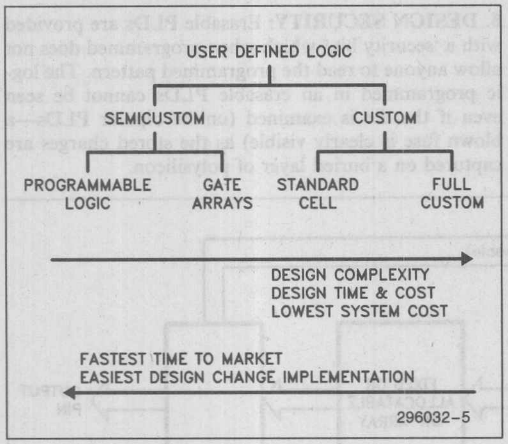

Figure 4. User-Defined Logic Alternatives Compared

LIMITATIONS OF BIPOLAR FUSE TECHNOLOGY FOR PROGRAMMABLE LOGIC DEVICES

Until 1985, all PLDs were built using Bipolar fuse technology. The bipolar fuse based devices, although offering the users the benefits of quick time to market and low development costs, had several inherent limitations.

a. HIGH POWER CONSUMPTION: Bipolar processes by nature are power hungry and as a consequence also make for very hot systems, often requiring cooling aids such as heat sinks and fans. They also cannot operate at lower voltages (2–3V) and have a lower level of noise immunity than MOS devices.

b. LOWER INTEGRATION: A fuse takes up a large amount of silicon area; this fact in conjunction with the large power requirements makes for smaller levels of integration.

c. ONE-TIME PROGRAMMABILITY: Bipolar fuses can only be blown once and cannot be reprogrammed. This does not allow for easy prototyping and could result in significant losses when preprogrammed parts are inventoried and design changes occur.

d. TESTABILITY: Since fuses can only be blown once, bipolar PLDs can only be destructively tested. Thus, testing is usually done by sampling or through additional testing elements incorporated in the chips, which can be blown to examine electrical characteristics. However, such testing methods never allow for 100% testability of all parts shipped. Thus, most users of bipolar programmable logic devices resort to extensive post-programming testing, specific to their applications.

ERASABLE PROGRAMMABLE LOGIC DEVICES

Erasable programmable logic devices result from the matching of CMOS EPROM technology with the architectures of programmable logic devices. Erasable PLDs use EPROM cells as logic control elements and therefore, when housed in windowed ceramic packages, can be erased with UV light and reprogrammed. Figure 5 shows the architecture of Intel erasable PLDs.

Other than the obvious benefit of reprogrammability, erasable PLDs offer several very significant benefits over bipolar PLDs. These are:

1. LOW POWER CONSUMPTION: Due to the CMOS technology, these products consume an order of magnitude less power than the equivalent bipolar devices. This allows for the design of complete CMOS systems, that can operate at lower voltages (less than 5V). Also, this makes for cooler systems that do not require cooling systems like fans.

2. GREATER LOGIC DENSITY: EPROM cells are an order of magnitude smaller than the smallest fuses. This means that the same function can be accommodated in significantly smaller die area, or that greater amounts of logic can now be incorporated on a single chip. Thus higher integration programmable logic devices result with the use of EPROM elements.

3. TESTABILITY: Since the EPROM cells are erasable, the entire EPROM array of the PLD can be 100% factory tested. Thus, before the part is shipped to the customers, it can be completely tested by the programming and erasure of all the EPROM logic control bits. This testing is therefore independent of any application, in contrast to the bipolar PLDs that need application specific testing.

4. ARCHITECTURAL ENHANCEMENTS: The inherent testability of the EPROM elements allows for

significant architectural improvements over bipolar PLDs. New features, such as buried registers, programmable registers, programmable clock control, etc., can now be incorporated because of this testability. These new features allow for greatly increased utilization of the erasable PLDs and use of these devices in newer applications.

5. DESIGN SECURITY: Erasable PLDs are provided with a 'security bit,' which when programmed does not allow anyone to read the programmed pattern. The logic programmed in an erasable PLDs cannot be seen even if the die is examined (unlike bipolar PLDs—a blown fuse is clearly visible) as the stored charges are captured on a buried layer of polysilicon.

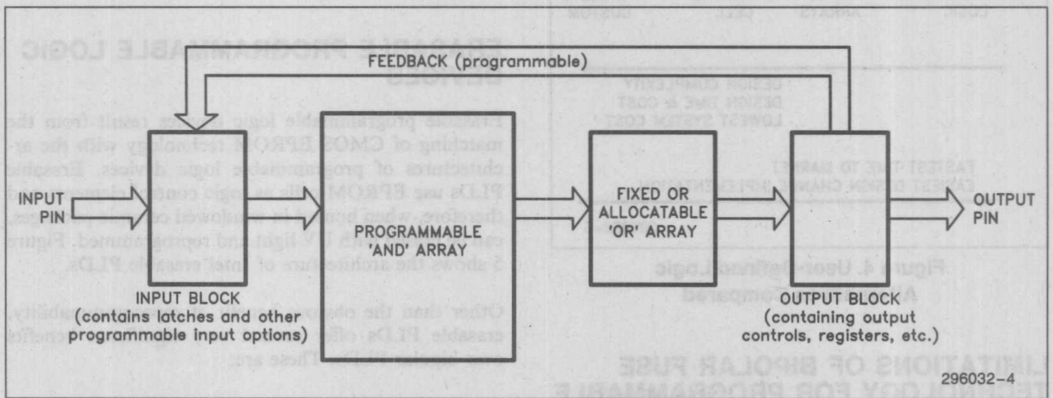

Figure 5. Architecture of Intel Erasable PLDs

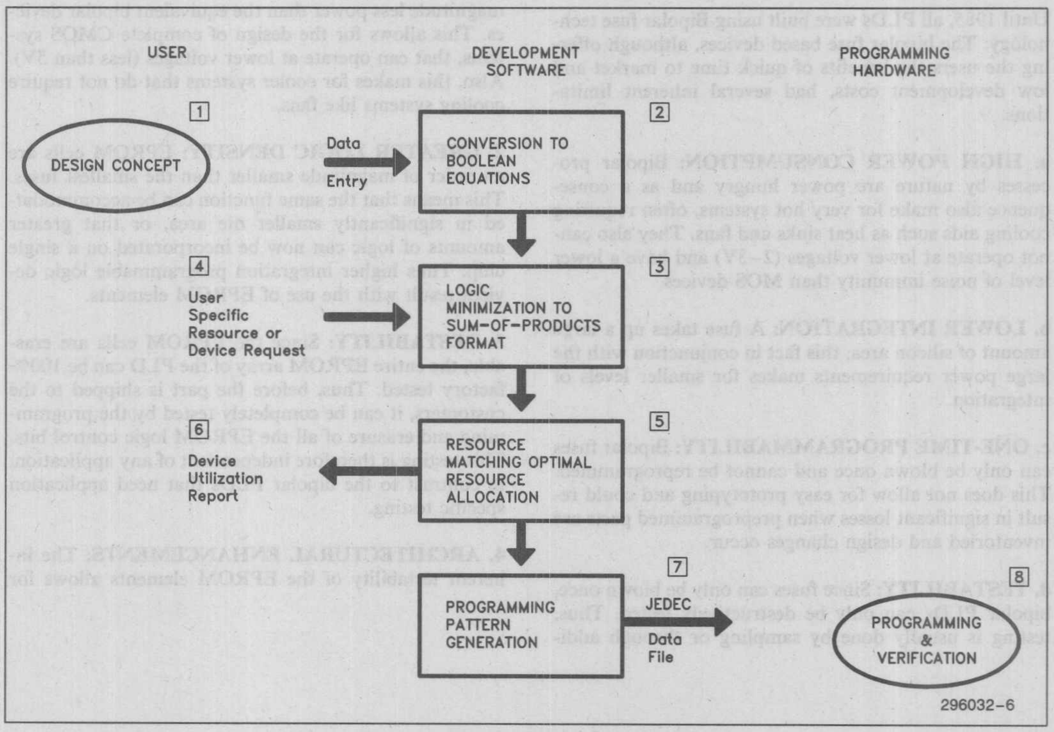

Figure 6. The PLD Design Process

The steps in a generalized design process of programmable logic is shown in Figure 6 and described in the following paragraphs.

STEP 1: The user decides on the logic he wants implemented in the PLD and enters the design into the PC or workstation. This **Design Entry** may be done by the following methods: (i)**SCHEMATIC CAPTURE**—A 'Mouse' or some other graphics input device is used to input schematics of the logic, (ii)**NET LIST ENTRY**—If the user has a hand drawn schematic he can enter the design into the computer by describing the symbols and interconnections in words using a standardized format called a net list (without using a graphics input device), (iii)**STATE EQUATION/DIAGRAM ENTRY**—Entry of a sequential design involving states and transitions between states. In the state diagram method circles represent states and the arrows interconnecting them represent the transitions. Equations or a state table can also be used to define a state machine, and (iv)**BOOLEAN EQUATIONS**—this is the most common design entry method. The logic is described in boolean algebraic equations.

STEP 2: The software converts all design entry data into boolean equations.

STEP 3: The boolean equations entered are converted to the sum of products format after logic reduction (minimization of the logic through heuristic algorithms).

STEP 4: The user has the ability to choose the PLD he would like the design implemented on. He can enter device choice and/or he can also enter in specific choices on the device as regards pinout he would like etc . . .

STEP 5: The software optimizes the logic equations to fit into the device using the minimum amount of resources (resources are input pins, output pins, registers and product terms and macrocells). This step is where the user requirements as regards required pins are taken into account. The user requests are viewed as constraints during the optimization process.

STEP 6: The software, at the end of the resource optimization/allocation, produces a report detailing the resources used up in fitting the design on the PLD. This report allows the user to incrementally stuff in logic by going back to Step 1 from this stage. Also, if the design overflowed the PLD, i.e., did not fit in the user chosen device, the software lists out the resources needed to complete the fit. The requirements such as four more inputs, one register more and one more output (are needed to complete the design) gives the user data in choosing a bigger PLD or in partitioning the intial design to fit into two devices.

STEP 7: The next step is to generate the appropriate programming pattern for the PLD. This is a standard "JEDEC" format interface and allows the output of the design software to be compatible with any piece of PROM programming hardware.

STEP 8: PROM programmer is used to program the pattern stored in the JEDEC file onto the PLD. Also, at this stage fuse programmed PLDs (bipolar) are functionally tested using test vectors included in the JEDEC file information.

CMOS TECHNOLOGY IN PLDs

Erasable PLDs are manufactured with Intel's proprietary CMOS technology. The backbone of the process is the integration of both a P and an N channel MOS transistor on the same substrate. In addition, erasable PLD's programmable architecture makes use of Intel's proven EPROM cell for programmable array interconnections as well as macrocell configuration bits. These cells are programmed electrically and erased with ultraviolet light. For details on Intel's CMOS technology and EPROM cells technology, refer to the *Components Quality/Reliability Handbook,* Order Number 210997.

CHMOS DESIGN GUIDELINES

Designing with Intel PLDs is relatively straightforward if the following guidelines are observed:

- Minimize the occurrence of ESD (electro-static discharge) when storing or handling PLDs.
- Observe good design rules in printed circuit board layout.
- Provide adequate decoupling capacitance at both the device and the board level.
- Connect all unused inputs to V_{CC} or GND (CMOS inputs should not be left floating).

Electrostatic Discharge

The two most common sources of electrostatic discharge are the human body and a charged environment.

A charged human body that touches a device lead discharges electricity into the device. Electrostatic discharge from people handling devices has long been recognized by manufacturers and users of all MOS products. Human body static electricity can be controlled by using ground straps and anti-static spray on carpeted floors. CMOS devices should also be stored and carried in conductive tubes or anti-static foam to minimize exposure to ESD from people.

Discharge also occurs when an integrated circuit is charged to one potential and then contacts a conductor at another potential. This type of ESD can be reduced

equipment, removing static generators such as paper from the work area, and erasing PLDs in metal tubes, metal trays, or conductive foam.

PCB Layout

The best PCB performance is obtained when close attention is paid to V_{CC}, GND, and signal traces. V_{CC} and GND should be gridded to minimize inductive reactance and to approximate a trace layer. Clocks should be laid out to minimize crosstalk. Ensure adequate power supply and ground pins on the board connector.

Decoupling

Decouple each PLD with a high-frequency ceramic capacitor in the range of 0.01 μF to 0.2 μF, depending on board frequency and current consumption. For most applications, a 0.1 μF capacitor will suffice. The following equation produces the exact value:

$$C = \frac{\Delta I_{CC}}{\Delta V / \Delta T}$$

where C = capacitor value

ΔI_{CC} = maximum switched current

ΔV = switching level

ΔT = switching time

For boards that contain mixed logic (PLDs and TTL), observe both PLD and TTL decoupling practices.

Unused Inputs

To minimize noise receptivity and power consumption, all unused inputs to PLDs should be connected to V_{CC} or GND. By default, PLDshell Plus software assigns unused inputs to GND. These pins shown on the pinout representation of the PLDshell Plus report file, should be connected to ground on the PCB. Pins listed as RESERVED on the report file must be left floating. Pins marked N.C. have no internal device connections and can also be left floating.

BOOLEAN MINIMIZATION TECHNIQUES FOR SOP ARCHITECTURES

Minimization plays an important role in logic design. Methods for minimization can be grouped into two classes. Class 1 includes manual methods for minimization, such as Boolean reduction or Karnaugh mapping. Class 2 is computer-assisted minimization.

to a certain point. Past that point, however, computer-assisted minimization plays a crucial part in efficient design. Even at the computer-assisted stage, the choice of minimizer software has an impact on time and the confidence level of the reduced equation (i.e., is it in the smallest possible form).

PLDshell Plus software includes a minimizer that uses the ESPRESSO algorithms. ESPRESSO was developed by U.C. Berkeley. The primary advantage of the ESPRESSO minimizer becomes apparent when designing large finite state machines or complex, product-term intensive logic designs. In these cases, ESPRESSO arrives at the minimize solution sooner, and frequently reduces the logic to a smaller number of product terms.

For more information on ESPRESSO, refer to *Logic Minimization Algorithms for VLSI Synthesis,* Brayton, Hachtel, McMullen, and Sangiovanni-Vincentelli, Kluwer Academic Publishers.

References

[BRO 81] D.W. Brown, "A State-Machine Synthesizer—SMS", Proc. 18th Design Automation Conference, pp. 301–304. Nashville, June 1981.

[HON 74] S. J. Hong, R. G. Cain and D. L. Ostapko, "MINI": A heuristic approach to logic minimization." *IBM Journal of Research and Development,* Vol. 18, pp. 443–458, September 1974.

LOGIC REFRESHER COURSE

Minimization of PLD logic equations is normally performed by sophisticated algorithms that eliminate the need for tedious manual reductions. The sections provided here contain logic reference tables for cases where manual reduction techniques may be desirable.

Boolean Algebra

The Sum-of-Product architecture used in PLDs makes Boolean algebra ideal for design analysis. The following tables summarize standard Boolean functions.

Properties

A*B	= B * A	Commutative Property
A + B	= B + A	
A * (B * C)	= (A * B) *C	Associative Property
A + (B + C)	= (A + B) + C	
A * (B + C)	= A * B + A * C	Distributive Property
A + B * C	=(A + B) * (A + C)	

Postulates

0 * 0 = 0	0 + 0 = 0	$\overline{0}$ = 1
0 * 1 = 0	0 + 1 = 1	$\overline{1}$ = 0
1 * 1 = 1	1 + 1 = 1	

Theorems

A * 0 = 0	A + 0 = A	$\overline{\overline{A}}$ = A
A * 1 = A	A + 1 = 1	
A * A = A	A + A = A	
A * $\overline{A}$ = 0	A + $\overline{A}$ = 1	

DeMorgan's Theorems

$\overline{(A + B + C + D)}$	=	$\overline{A} * \overline{B} * \overline{C} * \overline{D}$
$\overline{(A * B * C * D)}$	=	$\overline{A} + \overline{B} + \overline{C} + \overline{D}$

Logic Functions

A * A	=	A **AND** A
A + A	=	A **OR** A
$\overline{A}$	=	A **NOT**
A ⊕ B = A **EXCLUSIVE OR** B	=	A$\overline{B}$ + $\overline{A}$B

Karnaugh Maps

Graphical representation of data is usually easier to analyze than strings of ones and zeros. The Karnaugh Map techniques take advantage of this capability and provide an important tool to the logic designer.

Two Variables

B \ A	0	1
0	0	2
1	1	3

296032–7

Three Variables

C \ AB	00	01	11	10
0	0	2	6	4
1	1	3	7	5

296032–8

Four Variables

CD \ AB	00	01	11	10
00	0	4	12	8
01	1	5	13	9
11	3	7	15	11
10	2	6	14	10

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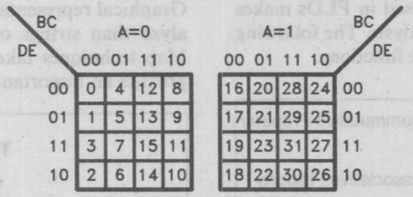
Five Variables



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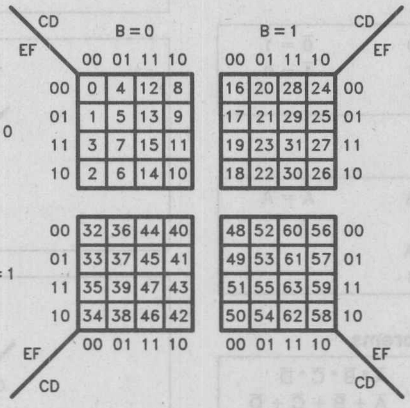
Six Variables



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Flip-Flop Tables

This subsection includes truth tables and excitation tables for the flip-flops supported by PLDs.

D Truth Table

D	Q_N	Q_{N+1}
0	0	0
0	1	0
1	0	1
1	1	1

D Excitation Table

Q_N	Q_{N+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

T Truth Table

T	Q_N	Q_{N+1}
0	0	0
0	1	1
1	0	1
1	1	0

T Excitation Table

Q_N	Q_{N+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

JK Truth Table

J	K	Q_N	Q_{N+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

JK Excitation Table

Q_N	Q_{N+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

SR Truth Table

S	R	Q_N	Q_{N+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	Illegal	

JK Excitation Table

Q_N	Q_{N+1}	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

NOTES:
Q_N = Present State
Q_{N+1} = Next State
X = Don't Care

AUTOMATIC STANDBY MODE (TURBO BIT)

Most Intel PLDs contain a programmable bit, the Turbo Bit, that optimizes devices for speed or power savings. When TURBO = ON, EPLDs are optimized for speed. When TURBO = OFF, they are optimized for power savings by automatically entering standby mode when input or I/O transitions are not detected over a short period of time. The following paragraphs describe how the Turbo Bit affects power and speed in PLDs.

Turbo Off (Low Power)

Most Intel PLDs contain circuitry that monitors inputs and feedbacks for transitions. When a transition is detected while the device is in standby mode, the circuit generates an active pulse. The leading edge of this pulse wakes the device up and the device responds according to its programming, changing outputs as necessary. If no new transitions occur during the active pulse, the device enters standby mode again. Outputs are always held valid in standby mode. Input transitions that occur during the active mode interval retrigger the active pulse. The active pulse is different depending on the device (5C060, 5AC312, etc), but is typically several times the propagation delay for a particular device.

In applications with infrequent input transitions, standby mode can result in significant power savings (see the appropriate data sheet for standby power vs. active power). The slight speed loss associated with waking up a device is in the range of 0–30 ns, which is small enough to allow standby mode to be used with most applications (see the appropriate data sheet for effect of Turbo Bit on performance).

Turbo On (Faster Speed)

In cases where the slight speed loss associated with waking a device from standby mode cannot be traded off to save power, the Turbo bit can be enabled for maximum speed operation. With the Turbo Bit enabled, the device is always in active mode, thus avoiding the wakeup delay. Note that data sheet performance is specified with the Turbo Bit enabled.

The Turbo Bit is enabled/disabled via a TURBO = ON or TURBO = OFF statement in a PLDshell Plus PDS or ADF option statements. It can also be enabled/disabled by editing the JEDEC file using device programming software. With TURBO = ON the device will be programmed for high speed; with TURBO = OFF the device will be programmed for automatic standby (power savings). The default (erased) state is OFF.

PAL*/GAL* TO PLD REPLACEMENT

Already in wide use throughout the electronics industry are numerous different Programmable Logic Devices. Most common PALs and GALs can be replaced or upgraded with the following Intel PLDs:

85C220

The 85C220 is a direct, drop-in replacement for most 20-pin PALs/GALs, although some PALs have an incompatible architecture. The 85C220 runs at up to 100 MHz with external feedback.

85C224

The 85C224 is a direct, drop-in replacement for most 24-pin PALs/GALs, although some PALS have an incompatible architecture. The 85C224 runs at up to 100 MHz with external feedback.

iPLD610

The 85C060/PLD610 is NOT a drop-in replacement for any 24-pin bipolar PAL, though it can functionally replace many higher-density devices. Some modification of CLK and OE signals may be required.

85C22V10/iPLD22V10

The iPLD22V10 is a direct, drop-in replacement for all 24-pin PALs/GALs. The 85C22V10 includes superset features such as Invertible CLK and expanded feedback options.

*PAL is a registered trademark of Advanced Micro Devices.
*GAL is a registered trademark of Lattice Semiconductor, Incorporated.

85C220 As a 20-Pin PAL Replacement

100% Compatible	
10H8, -2	16R6A
12H6, -2	16R4A
14H4, -2	16L8A
16H2, -2	16RP6A
10L8, -2	16RP4A
12L6, -2	16P8A
16L8, A-2, A-4	16R8A
16R4, A-2, A-4	16RP8A
14L4, -2	16V8A
16L2, -2	18P8
16R8, A-2, A-4	18V8
16R6, A-2, A-4	
16P8, -2	
16RP8, -2	
16RP6, -2	
16RP4, -2	
16V8	

85C224 As a 24-Pin PAL Replacement

100% Compatible	
14L8	20L8A
16L6	20R8A
18L4	20R6A
20L2	20R4A
20L8	20V8
20R8	
20R6	
20R4	

iPLD610 As a 24-Pin PAL Replacement

Modified Replacement
20RA10
22V10
32V10
26V10
26V12

85C22V10/iPLD22V10 As a 24-Pin PAL Replacement

100% Compatible
22V10
22VP10

QUALITY/RELIABILITY

Intel PLDs meet the same Quality and Reliability standards as Intel's microprocessors and memories. Reliabillty is not just tested, but is designed into each component Intel manufactures. This assures you that Intel PLDs will meet your system's quality/reliability needs through its life.

The methods used to guarantee the quality and reliability of Intel PLDs parallels the methods used with Intel EPROMs. Intel's *Component Quality/Reliability Handbook,* together with *Reliability Report RR-35, EPROM Reliability Data Summary,* can provide the generic information needed to assess Intel's design and testing procedures for PLDs. Current quality data for specific PLDs is published in RR-64, *Intel PLD Quality/Reliability Data Summary,* printed in this handbook.

PACKAGING

Intel PLDs are available in several packages to meet the wide requirements of customer applications. Current information on available packages is available from your local Intel field sales engineer. Detailed information on package dimensions, etc. for a particular package is provided in *Packaging Outlines and Dimensions,* Order Number 321369, which covers all Intel packages.

SOFTWARE AND PROGRAMMING SUPPORT

Intel provides design software and programming equipment to support its PLDs. In addition, Intel PLDs are supported by all major compiler and programmer manufacturers. Refer to the appendix to this handbook for detailed information.

ORDERING INFORMATION

Intel PLDs and FPGAs are identified as follows:

M D 5 C X X X — S S

$\underbrace{\text{M}}\ \underbrace{\text{D}}\ \underbrace{\text{5 C}}\ \underbrace{\text{X X X}}_{\text{Device}}\ —\ \underbrace{\text{S S}}_{\text{Speed}}$

Family

FX	—	FLEXlogic FPGA (Field Programmable Gate Array)
PLD	—	Industry Standard PLD
5AC	—	Advanced Architecture PLD
5C	—	Standard Architecture PLD
85C	—	High Speed Enhanced Architecture PLD

Package Type

D	—	Hermetic, Type D (Cerdip) Dip
N	—	Plastic, Leaded Chip Carrier
P	—	Plastic Dip
X	—	Unpackaged Device
KU	—	Plastic QUAD Flatpack

A — Indicates automotive operating temperature range (−40°C to +125°C)

J — Indicates a JAN qualified device, but is for internal identification purposes only. All JAN devices must be ordered by M38510 part number. (Example: M38510/42001 BQB), and will be marked in accordance with MIL-M-38510 specifications.

L — Indicates extended operating temperature range (−40°C to +85°C) express product with 160 + 8 hrs. dynamic burn-in.

*M — Indicates military operating temperature range (−55°C to +125°C)

Q — Indicates commercial temperature range (0°C to +70°C) express product with 160 + 8 hrs. dynamic burn-in.

T — Indicates extended temperature range (−40°C to +85°C) express product without burn-in.

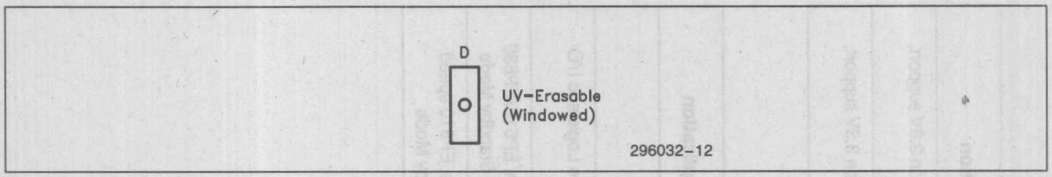
— No letter indicates commercial temperature range (0°C to +70°C) without burn-in.

Examples:

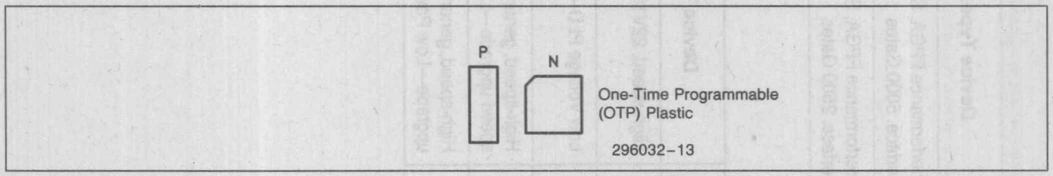
QD5C060-45 Commercial with burn-in, ceramic Dip, 060 (600 gate) device, 45 nanosecond.

*On military temperature devices, B suffix indicates MIL-STD-883C level B processing.

PLD PACKAGE TYPES



D = Windowed Ceramic DIP



P = Plastic DIP
N = Plastic PLCC

Refer to the Device Summary and each product's data sheet for available packages for a given part.

HIGH PERFORMANCE FLEXlogic DEVICES

FPGA	Packages	Pins	Mcells (Regs)	I/O	t_{PD} (ns)	f_{CNT1} (MHz)	t_{SU} (ns)	t_{CO} (ns)	I_{OL} (mA)	I_{CC} (mA) @ Freq. (MHz)	Device Type/Application
FX780	N KU	84 132	80 80	60 102	10, 15 10, 15	80 80	6.5 6.5	6.0 6.0	12 12	120 @ 80 120 @ 80	Highest performance FPGA, SRAM option 3.3V support, JTAG interface. 5000 Gates
FX740	N N	44 68	40 40	30 50	10, 15 10, 15	80 80	6.5 6.5	6.0 6.0	12 12	80 @ 80 80 @ 80	Highest performance FPGA, SRAM option 3.3V support, JTAG interface. 2500 Gates

HIGH PERFORMANCE INDUSTRY STANDARD DEVICES

PLD	Packages	Pins	Mcells (Regs)	I/O	t_{PD} (ns)	f_{CNT1} (MHz)	t_{SU} (ns)	t_{CO} (ns)	I_{OL} (mA)	I_{CC} (mA) @ Freq. (MHz)	Device Type/Application
PLD22V10	P, N	24, 28	10	22	7.5, 10, 15	111	3	6	16	130 @ 15	High-speed, 22V10
PLDLV22V10	P, N	24, 28	10	22	15	50	10	10	16	35 @ 15	Low Voltage PLD—3.3V Core Logic and I/O
PLD610	D, P, N	24, 28	16	20	10, 15, 25	74	7	6.5	12	105 @ 1	High-speed, general purpose; EP610/EP630 speed upgrade—Low Power Standby Mode
PLD910	D, P, N	40, 44	24	36	12, 15, 25	66.7	8	7	12	150 @ 1	High-speed, general purpose; EP910 speed upgrade—Low Power Standby Mode

PACKAGES:
D = Ceramic Dual In-Line Package (Windowed for UV Erase)
N = Plastic J-lead Chip Carrier (One-Time Programmable)
P = Plastic Dual In-Line Package (One-Time Programmable)
M = Military versions available (some speeds/packages); refer to Military Handbook (210461-009)
KU = Plastic Quad Flat Pack (One-Time Programmable)

*PAL is a registered trademark of Advanced Micro Devices, Inc.
*GAL is a registered trademark of Lattice Semiconductor, Corporation.

October 1993
Order Number: 296469-008

EXTENDED FEATURE DEVICES

PLD	Packages	Pins	Mcells (Regs)	I/O	t_{PD} (ns)	f_{CNT1} (MHz)	t_{SU} (ns)	t_{CO} (ns)	I_{OL} (mA)	I_{CC} (mA) @ Freq. (MHz)	Device Type/Application
5C031	D	20	8	18	40, 50	22	30	24	4	40 @ 10	General purpose PLDs; interface logic, state machine sequencers/controllers, Flexible I/O Architecture
5C032	D, P	20	8	18	30, 35, 40	25	23	17	4	30 @ 25	General purpose PLDs; interface logic, state machine sequencers/controllers
5C060	D, P N, M	24 28	16	20	45, 55	16.6	38	22	4	95 @ 96.6	General purpose PLDs; interface logic, state machine sequencers/controllers
5C090	D, P N, M	40 44	24	36	50, 60	16.4	38	23	4	150 @ 16.4	General purpose PLDs; interface logic, state machine sequencers/controllers
5C180	N, M	68	48	64	70, 75, 90	12.1	53	29	4	200 @ 12.2	General purpose PLDs; interface logic, state machine sequencers/controllers

PACKAGES:
D = Ceramic Dual In-Line Package (Windowed for UV Erase)
N = Plastic J-lead Chip Carrier (One-Time Programmable)
P = Plastic Dual In-Line Package (One-Time Programmable)
M = Military versions available (some speeds/packages); refer to Military Handbook (210461-009)

EXTENDED FEATURE DEVICES

PLD	Packages	Pins	Mcells (Regs)	I/O	t_{PD} (ns)	f_{CNT1} (MHz)	t_{SU} (ns)	t_{CO} (ns)	I_{OL} (mA)	I_{CC} (mA) @ Freq. (MHz)	Device Type/Application
5AC312	D, P N	24, 28	12	22	25, 30	33.3	15	15	8	100 @ 33.3	Advanced architecture, general purpose: dual feedback, p-term allocation, 2 Set/Reset OE p-terms, synchronous/asynchronous clocks
5AC324	D, P N	40, 44	24	36	25, 30	33	12.5	17.8	8	175 @ 33	Advanced architecture, general purpose: dual feedback, p-term allocation, 2 Set/Reset/OE p-terms, synchronous/asynchronous clocks

EXTENDED FEATURE DEVICES

PLD	Packages	Pins	Mcells (Regs)	I/O	t_{PD} (ns)	f_{CNT1} (MHz)	t_{SU} (ns)	t_{CO} (ns)	I_{OL} (mA)	I_{CC} (mA) @ Freq. (MHz)	Device Type/Application
85C220-80/66	D, P N	20 20	8	18	10, 12	80	7	5.5	12	60 @ 80	High-speed, 20-pin PAL/GAL superset (register optimized)—Low Power Standby Mode
85C220-100	N	20	8	18	7.5	100	4.5	5.5	24	115 @ 100	High-speed, 24-pin PAL/GAL superset (register optimized)
85C220-7/10	N	20	8	18	7.5, 10	74	7	6.5	24	105 @ 74	High-speed, 20-pin PAL/GAL superset (t_{PD} optimized)
85C224-80/66	D ,P N	24, 28	8	22	10, 12	80	7	5.5	12	60 @ 80	High-speed, 24-pin PAL/GAL superset (t_{PD} optimized)—Low Power Standby Mode
85C224-100	N	28	8	22	7.5	100	4.5	5.5	24	115 @ 100	High-speed, 24-pin PAL/GAL superset (register optimized)
85C224-7/10	N	28	8	22	7.5, 10, 15, 25	74	7	6.5	24	105 @ 74	High-speed, 24-pin PAL/GAL superset (register optimized)
85C22V10	D, P N	24 28	10	22	10, 15	71.4	7	7	16	130 @ 15	High-speed, 22V10 superset; Invertible CLK, Expanded Feedback options

PACKAGES:
D = Ceramic Dual In-Line Package (Windowed for UV Erase)
N = Plastic J-lead Chip Carrier (One-Time Programmable)
P = Plastic Dual In-Line Package (One-Time Programmable)

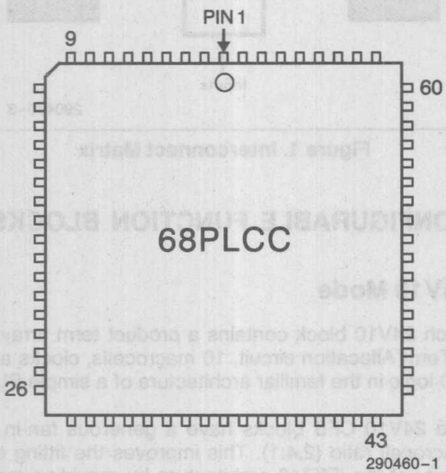
*PAL is a registered trademark of Advanced Micro Devices, Inc.
*GAL is a registered trademark of Lattice Semiconductor, Corporation.

Device Data Sheets 2

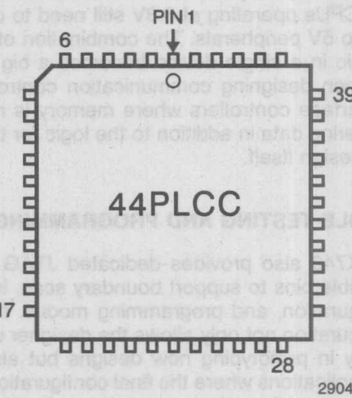
IFX740
10 ns FLEXlogic FPGA WITH SRAM OPTION

- **High Performance FPGA (Field Programmable Gate Array)**
  - **— Deterministic 10 ns Pin-to-Pin Propagation Delays**
  - **— 80 MHz System Clock Frequency**
- **2,500 Equivalent Logic Gates or up to 5,120 Bits of SRAM**
- **0.8μ CMOS Technology**
  - **— Power Management Options Minimize Active Power Consumption (1 mA/MHz)**
  - **— 1 mA Standby Version Available**
- **JTAG 1149.1 Compatible Test Port**
  - **— Supports Boundary Scan and In-Circuit Reconfiguration/ Programming**
- **Four Configurable Function Blocks (CFBs) Linked by a 100% Connectable Matrix**
  - **— Improves Fitting of Complex Designs**
- **Any CFB Can Be Either 24V10 Logic or SRAM Block**
  - **— Up to 40 Complex Macrocells**
  - **— 128 x 10 SRAM Configuration**
  - **— CFB Selectable 3.3V or 5V Outputs**
  - **— Open-Drain Output Option**
- **24V10 Macrocell Features**
  - **— Dual Feedback on All I/O Pins**
  - **— Allocation Supports up to 16 Product Terms per Macrocell with No Performance Penalty**
  - **— 12 Clocking Options**
  - **— Flexible Preset/Clear Options**
  - **— Selectable D/T Flip-Flops**
  - **— Fast 12-Bit Identity Compare Option**
- **Supported by Industry Standard Design and Programming Tools**

2



290460–1



290460–2

Package Options

Pins	Package	Macrocells	I/O	Inputs	Clocks	JTAG/V_{PP}	V_{CC}	GND
44	PLCC	40	30	0	2	5	3	4
68	PLCC	40	40	10	2	5	5	6

November 1993
Order Number: 290460-003

INTRODUCTION

The iFX740 is the second member of the Intel FLEXlogic FPGA (Field Programmable Gate Array) family. The iFX740 consists of four configurable function blocks (CFBs) linked by a 100% connectable matrix. Each CFB can be defined either as a 24V10 logic block or as a block of 128 x 10 SRAM. This combination will provide approximately 2,500 gates of logic in a choice of two PLCC packages.

FLEXIBLE PERFORMANCE

The iFX740 uses Intel's 0.8μ CHMOS EPROM technology to provide an 80 MHz external clock frequency with predictable 10 ns pin-to-pin delays. This advanced process technology combined with power management options enables very low active and standby power consumption.

FLEXIBLE FEATURES

The unique combination of features available in the iFX740 makes it ideal for a wide variety of applications. For example, the high performance and flexible clock options provided are designed to support functions such as bus control, custom cache control, and DRAM control for the current and next generation of Intel microprocessors. The very low power consumption and user selectable 5V/3.3V outputs allow the iFX740 to be used in mixed voltage applications such as portable or embedded systems where CPUs operating at 3.3V still need to communicate to 5V peripherals. The combination of SRAM and logic in a single device becomes a big advantage when designing communication controllers or bus interface controllers where memory is required for buffering data in addition to the logic for the controller design itself.

FLEXIBLE TESTING AND PROGRAMMING

The iFX740 also provides dedicated JTAG 1149.1 compatible pins to support boundary scan, in-circuit reconfiguration, and programming modes. In-circuit reconfiguration not only allows the designer ultimate flexibility in prototyping new designs but also supports applications where the final configuration is not fixed. New configurations may be downloaded to the iFX740 upon power-up to reflect changes in system organization or design requirements that cannot be determined at production time.

FLEXIBLE TOOLS SUPPORT

The FLEXlogic FPGA family is supported by industry standard design entry/programming environments including Intel's PLDshell Plus software. This software runs on Intel386™ or higher PC-compatible platforms.

INTERCONNECT

The Global interconnect Matrix that connects each of the CFB blocks is 100% connectable. Any combination of signals in the matrix can be routed into any CFB block, up to the maximum fan-in of the block (24).

This high degree of connectivity between CFB blocks eliminates routing problems during rework of a complex design.

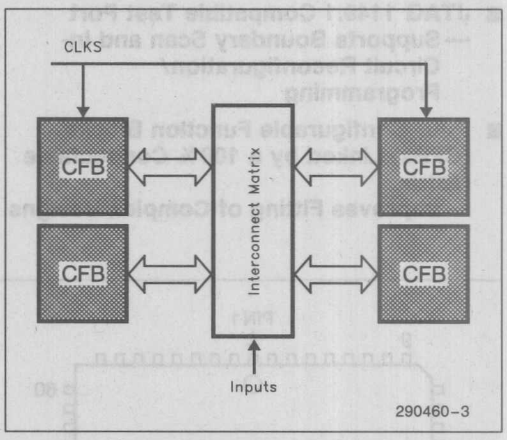


Figure 1. Interconnect Matrix

CONFIGURABLE FUNCTION BLOCKS

24V10 Mode

Each 24V10 block contains a product term array, a P-Term Allocation circuit, 10 macrocells, clocks and I/O logic in the familiar architecture of a simple PLD.

The 24V10 CFB blocks have a generous fan-in to macrocell ratio (2.4:1). This improves the fitting capacity of the iFX740 architecture by providing more available interconnect lines from the global interconnect matrix for each macrocell.

The 24V10 blocks also provide two asynchronous Clear/Preset control terms and two Output Enable control terms (with an inversion option for each). Within each 24V10 block an identity compare circuit is available that can perform a compare of up to 12 bits within the t_{PD} of the device.

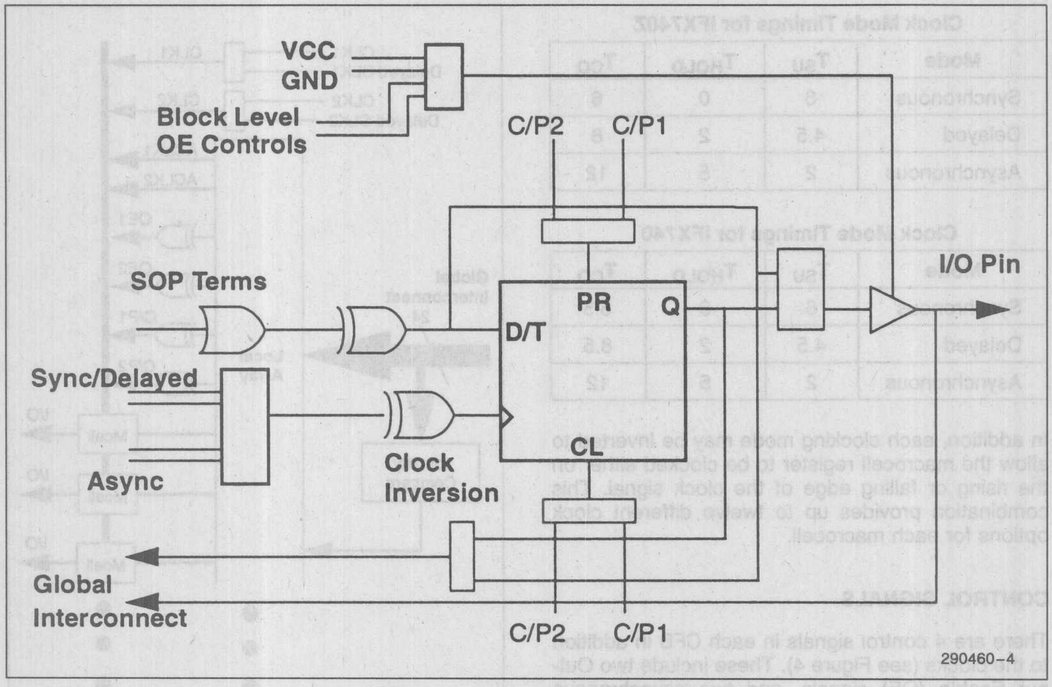


Figure 2. CFB as 24V10 Block

MACROCELL CONFIGURATIONS

Each I/O of the device has dual (internal and pin) feedback paths (see Figure 2). This allows macrocells to be used for buried logic while the I/O pins are used as inputs. Depending on the package used, some macrocell outputs may not be brought outside the package. These I/Os may still be used to provide buried logic since internal feedback is available. The macrocells can be configured either as a fast combinatorial block, a D-register, or a T-register. J/K and S/R registers are available as software emulations.

CLOCKING MODES

There are three clocking modes available for every macrocell (see Figure 3): *synchronous*, *delayed*, *asynchronous*. Table 1 shows the different timing options each clock mode offers.

Synchronous is the standard clock mode where the register clock is driven directly from one of the two global clock pins.

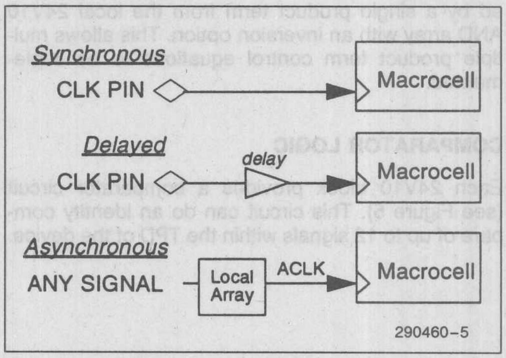


Figure 3. Clock Modes

Delayed clock is similar to *synchronous*, but there is a local delay added (within the CFB) to either of the two synchronous clock signals.

Asynchronous mode is where the register clock uses one of the two local CFB ACLK product terms.

Clock Mode Timings for iFX740Z

Mode	T_{SU}	T_{HOLD}	T_{CO}
Synchronous	6	0	6
Delayed	4.5	2	8
Asynchronous	2	5	12

Clock Mode Timings for iFX740

Mode	T_{SU}	T_{HOLD}	T_{CO}
Synchronous	6	0	6.5
Delayed	4.5	2	8.5
Asynchronous	2	5	12

In addition, each clocking mode may be inverted to allow the macrocell register to be clocked either on the rising or falling edge of the clock signal. This combination provides up to twelve different clock options for each macrocell.

CONTROL SIGNALS

There are 4 control signals in each CFB in addition to the clocks (see Figure 4). These include two Output Enable (OE) signals, and two asynchronous Clear/Preset signals. Each control signal is generated by a single product term from the local 24V10 AND array with an inversion option. This allows multiple product term control equations to be implemented.

COMPARATOR LOGIC

Each 24V10 block provides a comparator circuit (see Figure 5). This circuit can do an identity compare of up to 12 signals within the TPD of the device.

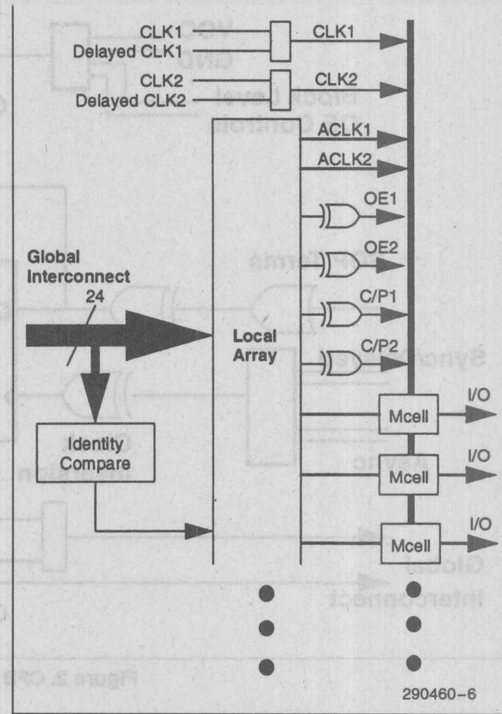


Figure 4. Control Signals

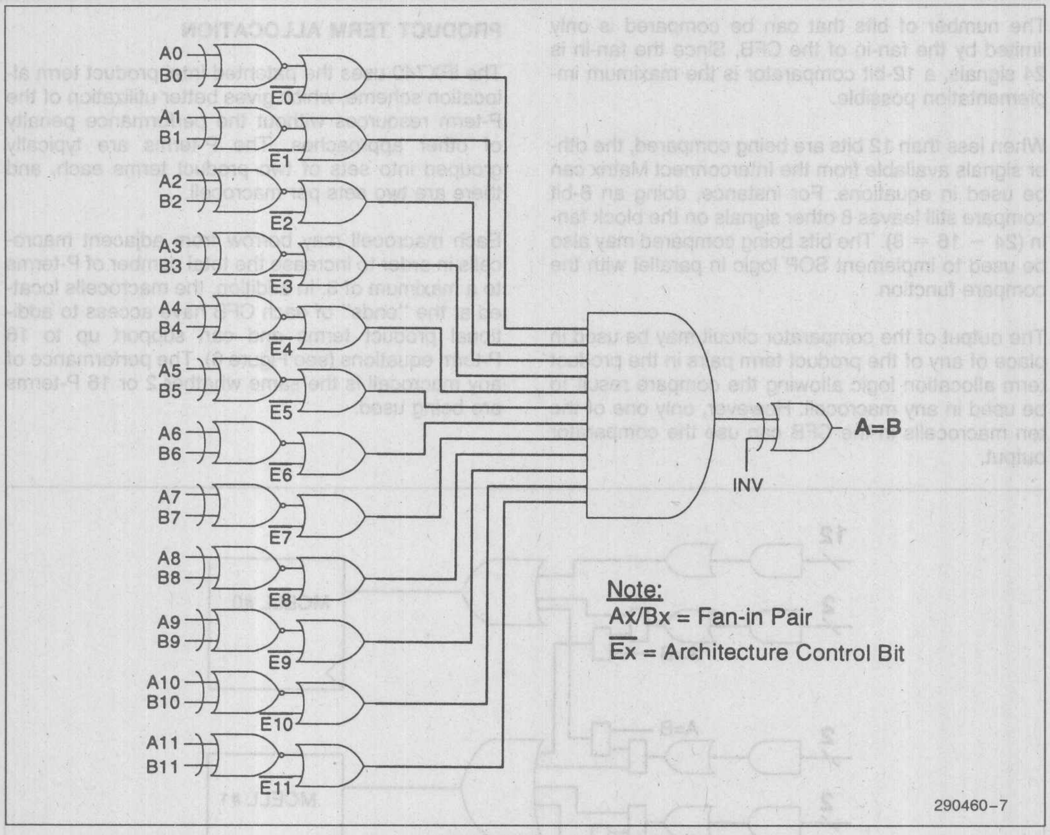


Figure 5. 12-Bit Identity Compare Logic

The number of bits that can be compared is only limited by the fan-in of the CFB. Since the fan-in is 24 signals, a 12-bit comparator is the maximum implementation possible.

When less than 12 bits are being compared, the other signals available from the Interconnect Matrix can be used in equations. For instance, doing an 8-bit compare still leaves 8 other signals on the block fan-in (24 − 16 = 8). The bits being compared may also be used to implement SOP logic in parallel with the compare function.

The output of the comparator circuit may be used in place of any of the product term pairs in the product term allocation logic allowing the compare result to be used in any macrocell. However, only one of the ten macrocells in the CFB can use the comparator output.

PRODUCT TERM ALLOCATION

The iFX740 uses the patented Intel product term allocation scheme, which gives better utilization of the P-term resources without the performance penalty of other approaches. The P-terms are typically grouped into sets of two product terms each, and there are two sets per macrocell.

Each macrocell may borrow from adjacent macrocells in order to increase the total number of P-terms to a maximum of 8. In addition, the macrocells located at the "ends" of each CFB have access to additional product terms and can support up to 16 P-term equations (see Figure 6). The performance of any macrocell is the same whether 2 or 16 P-terms are being used.

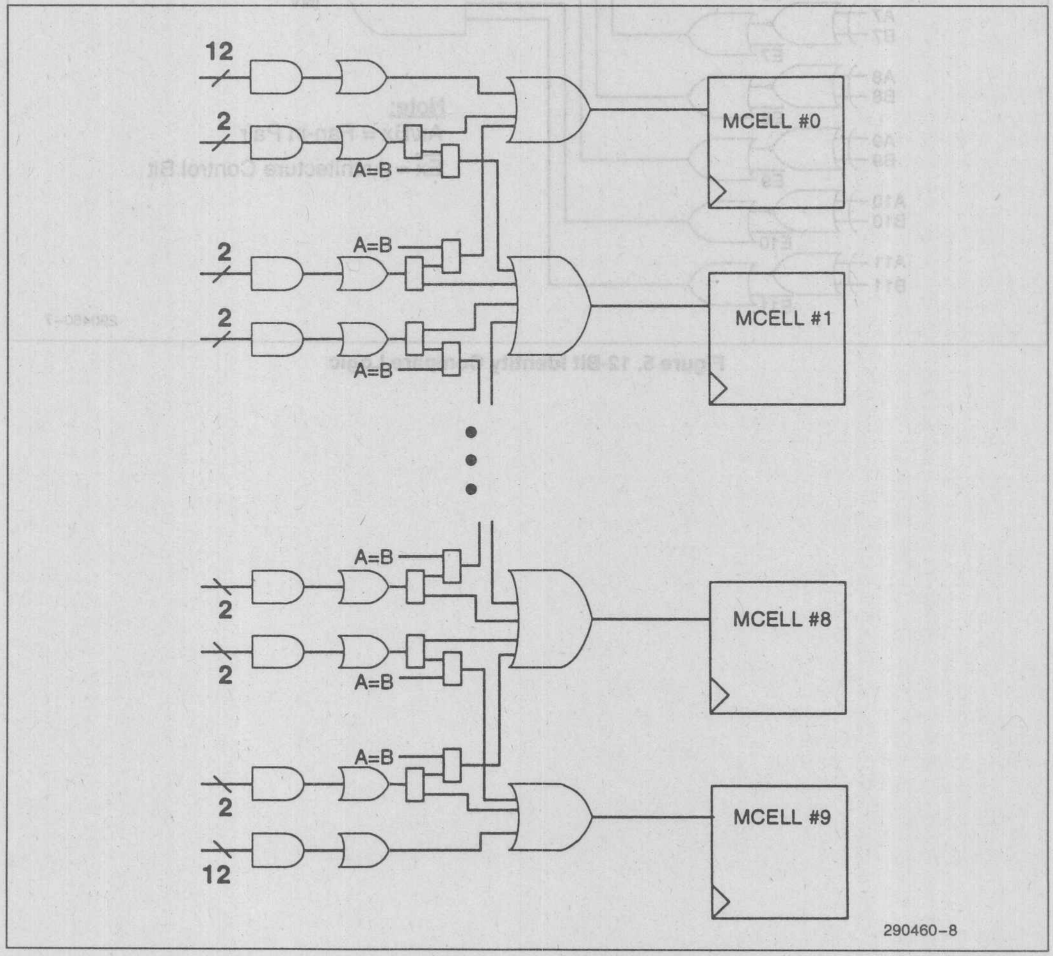


Figure 6. CFB Product Terms

SRAM Configuration

Each iFX740 CFB block can be configured as a 128 x 10 (128 words by 10 bits) SRAM block (see Figures 7 and 8). The SRAM is accessed in a conventional manner by using 7 bits of the 24 signal fan-in as address information and 10 bits as data-in. Three bits are used for $\overline{BE}$ (Block Enable), $\overline{WE}$, and $\overline{OE}$ controls (see Table 1).

Table 1. SRAM Function Table

Inputs			Cycle	I/O Pins
$\overline{BE}$	$\overline{WE}$	$\overline{OE}$		
1	X	X	None	Disabled
0	1	1	Read	Disabled
0	1	0	Read	Enabled
0	0	1	Write	Disabled
0	0	0	Write	Enabled

It is possible to define the SRAM memory either with a bidirectional I/O data bus or with a separate input data bus and output data bus.

The SRAM memory bits are initialized by the on-chip non-volatile configuration cells during power-up. Therefore, the data in the SRAM can be pre-configured at programming time. As long as no memory writes to this block are executed, the SRAM will contain a copy of the nonvolatile cells. In this way, the SRAM block can be used as read only memory (ROM).

When a CFB is configured as a SRAM, regular Sum-of-Product logic is unavailable in that block. All of the macrocells and p-terms have been converted to SRAM use.

Different sized SRAM organizations are possible by cascading multiple CFBs to increase the width or depth of the memory.

Input Configuration

Inputs, as well as I/O pins that are used as inputs, can be optimized for minimum standby current during either CMOS or TTL operation by using the "CMOS_LEVEL" and "TTL_LEVEL" keywords available in the PLDasm design language of PLDshell Plus. For 5V CMOS inputs, the "CMOS_LEVEL" keyword (the default condition for PLDasm) should be used. For TTL or 3.3V CMOS inputs, the "TTL_LEVEL" keyword should be used to minimize standby power consumption. Third party tools that support the FLEXlogic family provide input configuration in a method specific to each tool. For Additional information refer to Application Brief AB-27.

Output Configuration

3.3V SELECTION

The pins in an I/O block can operate at 3.3V by tying the appropriate V_{CCO} pins to a 3.3V power supply. While the iFX740 still requires 5V V_{CC} for normal operation, the V_{CCO} pin associated with each CFB block may be connected to either 5V or 3.3V to control the output voltages of the I/O pins in that block. This allows the iFX740 to be used in mixed voltage systems. For example, the iFX740 device may be used as an interface to bridge between a 3.3V CPU and 5V peripheral logic. In addition, all input pins are 5V safe so mixing 3.3V outputs and 5V inputs is supported.

OPEN DRAIN OUTPUT OPTION

The device can also be configured to enable an open drain output option for each I/O pin. If desired, more complex equations can be implemented by using multiple open drain outputs with an externally supplied pull-up resistor to emulate an additional OR plane.

TTL VERSUS CMOS OUTPUTS

There is a weak pullup provided for CMOS-compatible outputs. This pullup is always active in both 3.3V and 5V modes.

JTAG/IEEE 1149.1 TESTABILITY

The JTAG/IEEE 1149.1 Standard Boundary Scan architecture is implemented in the iFX740. This feature supports fault isolation testing of board designs at the component level and enhances production testing, field repair, and is ideal for Fault Tolerant applications.

The iFX740 boundary scan support consists of an Instruction Register, a Data Register, scan cells, and associated logic which are accessed through the Test Access Port (TAP). The TAP interface consists of three inputs: Test Mode Select (TMS), Test Data In (TDI) and Test Clock (TCK), and one output: Test Data Out (TDO).

The boundary scan cells of the iFX740 external signals are linked to form a shift register chain for all active pins. This chain provides a path which can be used to shift in test stimulus as well as shift out test response data for inspection.

For example, a continuity test may be performed between two JTAG devices on a circuit board by placing a known value on the output buffers of one de-

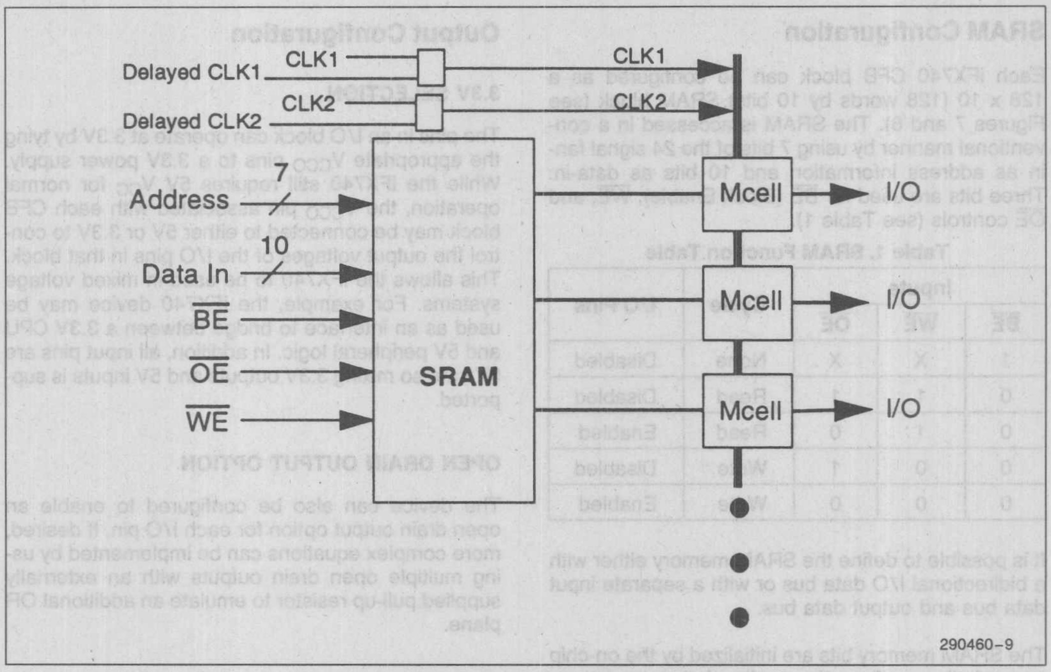


Figure 7. SRAM Overall Block Diagram

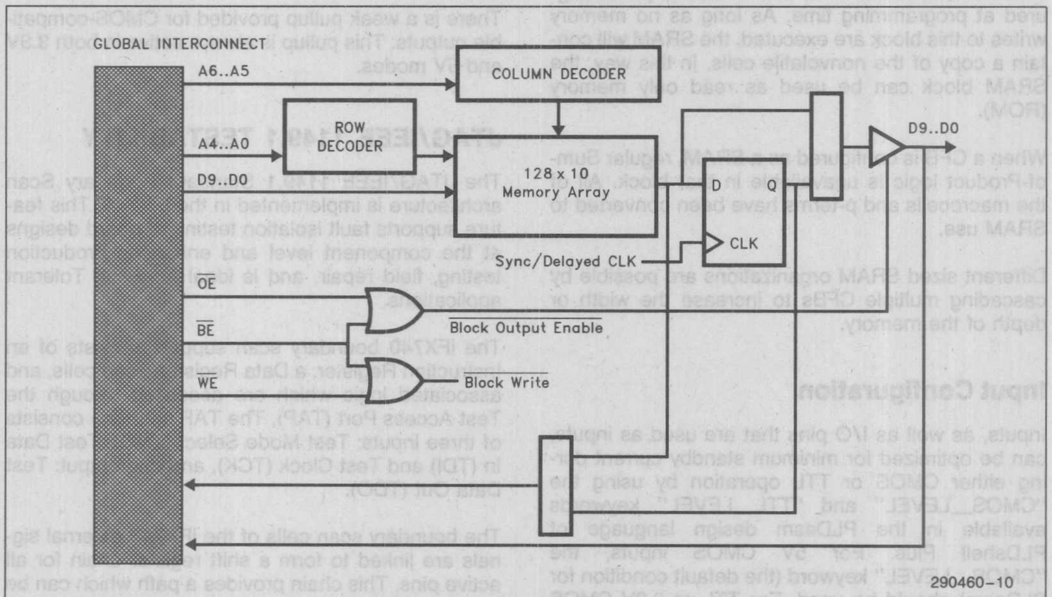


Figure 8. SRAM Functional Block Diagram

vice while observing the input buffers of the other device. This same technique may be used to perform simple in-circuit functional testing of the iFX740 for prototyping new system designs.

The 4-pin JTAG test interface is also used for standard programming, in-circuit reconfiguration, and in-circuit programming.

Boundary Scan Instructions

The iFX740 boundary scan Instruction Register (IR) supports public instruction opcodes, extended instruction opcodes used for the Program/Verify modes, and additional Intel private instructions.

Public Instructions

EXTEST (IR opcode 00000 binary):

The EXTEST instruction drives the output pins to the values contained in the boundary scan cells which allows testing of circuitry external to the iFX740 package, typically for printed circuit board interconnects.

BYPASS (IR opcode 11111 binary):

The BYPASS instruction selects the one bit ByPass Register, (BPR), to be connected to TDI and TDO.

SAMPLE/PRELOAD (IR opcode 00001 binary):

The SAMPLE/PRELOAD instruction is used for two functions. The SAMPLE/PRELOAD instruction 1) allows a snapshot of the values of the pins of the iFX740 in an unobtrusive manner and 2) preloads data to the iFX740 pins to be driven to the system circuit board when executing the EXTEST instruction.

IDCODE (IR opcode 00010 binary):

The IDCODE instruction selects the ID code register to be connected to TDI and TDO allowing the IDcode to be serially shifted out of TDO.

UESCODE (IR opcode 10110 binary):

The UESCODE instruction selects the User Electronic Signature (UES) register to be connected to TDI and TDO allowing the UES code to be serially shifted out of TDO.

HIZ (IR opcode 01000 binary):

The HIZ instruction sets all I/Os to a high impedance state.

IN-CIRCUIT RECONFIGURATION

The iFX740 supports in-circuit reconfiguration and in-circuit programming through the use of the 4-pin JTAG test port. Downloading a new configuration can be accomplished by simply shifting the new data into the device.

This may be done as many times as desired in a prototyping scenario. Once the final version of the design is confirmed it may be programmed into the non-volatile cells so that the configuration will not be lost even when the power is turned off. This is also done through the use of the JTAG test port plus the programming voltage pin (V_{PP}).

For more details on in-circuit reconfiguration and programming please refer to the iFX740 Device Programming and In-Circuit Reconfiguration Specification and supporting application notes.

SECURITY

A programmable security bit controls access to the data programmed into the device. Once this security bit is set, the design cannot be read out of the non-volatile cells or the SRAM. The state of the nonvolatile security bit at power-up determines access and cannot be changed by in-circuit reconfiguration.

SOFTWARE SUPPORT

PLDshell Plus

PLDshell Plus is a sophisticated development tool for Intel programmable logic and is all you need to begin designing with Intel FPGAs. With PLDshell Plus, you can develop, compile, and simulate efficient designs for Intel FPGAs and PLDs.

PLDshell Plus includes several enhancements over earlier versions:

- Design Merge
- SRAM Configuration Support
- Compare Operation Support
- Simulation Support for Intel FPGA
- Vector Notation
- Full Mouse Support
- Device Selector

DESIGN MERGE

PLDshell Plus can merge multiple PDS design files into any Intel PLD, including the Intel iFX740. The Merge function makes it easy for designers to consolidate multiple PLDs into a single, high-performance FPGA or PLD.

FPGA ARCHITECTURAL FEATURE SUPPORT

PLDshell Plus supports all of the innovative architectural features of the iFX740 through the implementation of new language syntax such as:

— SRAM configuration

— Compare operation

— Buried macrocells

— Clocking options

— 3.3V and 5V options

FUNCTIONAL SIMULATION

PLDshell Plus allows the designer to simulate the internal function of any Intel FPGA or PLD for rapid design verification.

PLDshell Plus provides the following simulation capabilities:

— Event-driven simulation of combinatorial, registered, and state machine designs

— Ability to set any input, preload any register, and compare any output against an expected value

— Ability to group signals together (form a vector) to simulate a bus

— Generation of test vectors from simulation results for inclusion in the JEDEC file

— Simulation history file with ability to output a subset of signals to a secondary trace file

DEVICE SELECTOR

The designer can develop the logic design first, and then use the PLDshell Plus device selector to pick a list of appropriate devices. After a design is compiled or estimated through PLDshell Plus a report file is generated. Contained in the report file is a listing of suggested devices appropriate for the target design.

SYSTEM REQUIREMENTS

Listed below are the minimum requirements for a system in order to use PLDshell Plus:

— Intel 386 based PC compatible

— 4MB RAM (minimum)

— VGA monitor/adaptor

— DOS 3.1 (or later)

THIRD-PARTY SUPPORT DESIGN SOFTWARE

Third party tools support will be provided by the following vendors:

- Cadence
  - — Composer*: Comprehensive suite of design entry, debug and documentation capabilities.
  - — Verilog-XL*: Digital logic simulator and interactive debug environment.
- Data I/O
  - — ABEL*: Design software allowing you to describe and implement logic designs.
- Logical Devices
  - — CUPL*: High level, universal design software package.
- Mentor Graphics
  - — Design Architect*: Integrated system of schematic, symbol, and text editors for capturing designs.
  - — QuickSim*: High performance logic simulator for function and performance verification.
- Minc
  - — PLDesigner-XL*: Powerful design tool that can be used for all types of programmable logic with automatic device selection, automatic partitioning and functional simulation.
- OrCAD
  - — PLD Tools* Schematic Design Tool*: Software tool environment including schematic entry, test vector generation and multiple forms of input.
  - — Verification/Simulation Tool*: Series of software tools for performing timing-based simulation of designs.
- Viewlogic
  - — ViewPLD* & Powerview*: Integrated schematic capture and simulation environment.

PROGRAMMING SUPPORT

Programming Support will be provided by a number of leading vendors, such as:

- Products in Motion (916) 363-0571
  - –PROTAG JTAG Programmer
- BP Microsystems
  - –PLD 1100
- Data I/O
  - –Unisite
  - –2900/3900
- Elan
  - –Model 6000
- Advin Systems Inc
  - –PILOT-U84
  - –PILOT-U40
- Logical Devices
  - –ALLPRO
- SMS
  - –Sprint Plus

DEVICE MODELS

Simulation models will be provided by the following vendors:

- Logic Modeling Corporation
  - –

Smart Model: Device model support for behavioral simulation through a variety of simulators.

- Viewlogic

ORDERING INFORMATION

f_{CNT1} (MHz)	F_{MAX} (MHz)	t_{PD} (ns)	I_{SB} (mA)	I_{CC} (mA/MHz)	Order Code	Package
80	100	10	20	1.0	N68FX740-10	68-Pin PLCC
					N44FX740-10	44-Pin PLCC
50	66.7	15	20	1.0	N68FX740-15	68-Pin PLCC
					N44FX740-15	44-Pin PLCC
80	100	10	1	1.0	N68FX740Z-10	68-Pin PLCC
					N44FX740Z-10	44-Pin PLCC
50	66.7	15	1	1.0	N68FX740Z-15	68-Pin PLCC
					N44FX740Z-15	44-Pin PLCC

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage (V_{CC})(1) .... −2.0V to +7.0V

Programming Supply Voltage (V_{PP})(1) .... −2.0V to +13.5V

DC Input Voltage (V_I)(1, 2) .... −0.5V to V_{CC} +0.5V

Storage Temperature (t_{stg}) ...... −65°C to +150°C

Ambient Temperature (t_{amb})(3) ... −10°C to +85°C

NOTES:

1. Voltages with respect to ground.
2. Minimum DC input is −0.5V. During transitions, the inputs may undershoot to −2.0V or overshoot to +7.0V for periods less than 20 ns under no load conditions.
3. Under bias. Extended temperature versions are also available.

NOTICE: This data sheet contains information on products in the sampling and initial production phases of development. The specifications are subject to change without notice. Verify with your local Intel Sales office that you have the latest data sheet before finalizing a design.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Units
V_{CC}/V_{CCO}	Supply Voltage −5V	4.75	5.25	V
V_{CCO}	Output Supply Voltage −3.3V	3.0	3.6	V
V_{IN}	Input Voltage	0	V_{CC}	V
V_O	Output Voltage	0	V_{CCO}	V
T_A	Operating Temperature	0	+70	°C
t_R	Input Rise Time		500	ns
t_F	Input Fall Time		500	ns

D.C. CHARACTERISTICS (T_A = 0°C to +70°C, V_{CC} = 5.0V ±5%)(4)

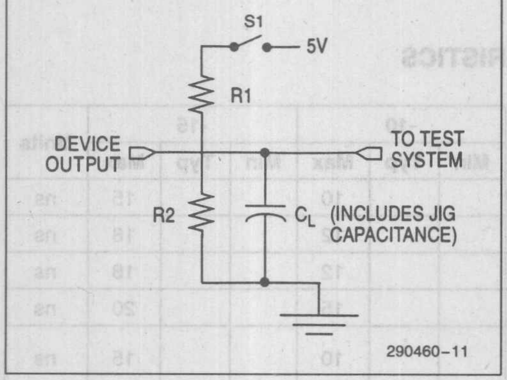
Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
V_{IH}(5)	High Level Input Voltage	2.0		V_{CC} +0.3	V	
V_{IL}(5)	Low Level Input Voltage	−0.3		0.8	V	
V_{OH}	5V TTL High Level Output	2.4			V	I/O = −4.0 mA D.C., V_{CC} = Min.
	5V CMOS High Level Output	V_{CC} −0.2			V	I/O = −20 μA D.C., V_{CC} = Min.
	3V High Level Output Voltage	V_{CC} −0.2			V	I/O = −20 μA D.C., V_{CC} = Min.
V_{OL}	5V Low Level Output Voltage			0.45	V	I/O = 12 mA D.C., V_{CC} = Min.
	3V Low Level Output Voltage			0.2	V	I/O = 20 μA D.C., V_{CC} = Min.
I_I(10)	Input Leakage Current			±10	μA	V_{CC} = Max., V_{IN} = GND or V_{CC}
I_{OZ}	Output Leakage Current			±50	μA	V_{CC} = Max., V_{OUT} = GND or V_{CC}
I_{SC}(6)	Output Short Circuit Current	−30		−120	mA	V_{CC} = Max., V_{OUT} = 0.5V

D.C. CHARACTERISTICS (T_A = 0°C to +70°C, V_{CC} = 5.0V ±5%)(4) (Continued)

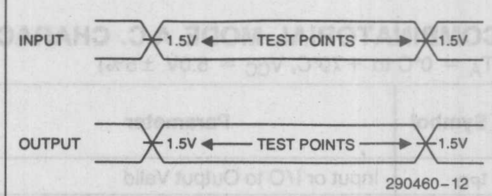
Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
I_{SB}	Standby Power Supply Current FX740		20		mA	$V_{IN} = V_{CC}$ or GND, Outputs Open
	Standby Power Supply Current FX740Z		1		mA	
I_{CC} Active	Power Supply Current FX740		1		mA per MHz	$V_{IN} = V_{CC}$ or GND, Device Programmed a Two 20-Bit Counters
	Power Supply Current FX740Z		1		mA per MHz	

NOTES:
4. Typical values are at T_A = 25°C, V_{CC} = 5V.
5. Absolute values with respect to device GND; all over and undershoots due to system and tester noise are included. Do not attempt to test these values without suitable equipment.
6. Not more than 1 output should be tested at a time. Duration of that test should not exceed 1 second.
10. Input leakage current on JTAG pins: ±25 μA.

A.C. TESTING LOAD CIRCUIT



A.C. TESTING INPUT, OUTPUT WAVEFORM



NOTE:
Inputs are driven at 3.0V for a Logic "1" and 0V for a Logic "0". Timing measurements are made at 1.5V. Outputs are measured at 1.5V. Device input rise and fall times <3 ns.

SWITCHING TEST CIRCUIT

Specification	S1	C_L	Commercial R1	Commercial R2	Measured Output Value
t_{PD}	Closed				1.5V
t_{PZX}	Z → H: Open Z → L: Closed	35 pF	330Ω	200Ω	1.5V
t_{PXZ}	H → Z: Open L → Z: Closed	5 pF			H → Z: V_{OH} − 0.5V L → Z: V_{OL} + 0.5V

PIN CAPACITANCE (T_A = 0°C to +70°C, V_{CC} = 5.0V ±5%)(7)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
C_{IN}	Input Capacitance	V_{IN} = 2V, f = 1.0 MHz		10	12	pF
C_{IO}	I/O Capacitance	V_{OUT} = 2V, f = 1.0 MHz		12	15	pF
C_{CLK}	Clock Pin Capacitance	V_{OUT} = 2V, f = 1.0 MHz		15	18	pF
C_{VPP}	V_{PP} Pin Capacitance	f = 1.0 MHz		12	15	pF

NOTES:
7. These values are evaluated at initial characterization and whenever design modifications occur that may affect capacitance.

COMBINATORIAL MODE A.C. CHARACTERISTICS
(T_A = 0°C to +70°C, V_{CC} = 5.0V ±5%)

Symbol	Parameter	-10 Min	-10 Typ	-10 Max	-15 Min	-15 Typ	-15 Max	Units
t_{PD}	Input or I/O to Output Valid			10			15	ns
t_{PZX}(8)	Input or I/O to Output Enable			12			18	ns
t_{PXZ}(8)	Input or I/O to Output Disable			12			18	ns
t_{CLR}	Input or I/O to Asynchronous Clear/Preset			15			20	ns
t_{COMP}	Comparator Input or I/O Feedback to Output Valid			10			15	ns

(T_A = 0°C to +70°C, V_{CC} = 5.0V ±5%)

Symbol	Parameter	Synchronous		Delayed Sync		Async		Units
		Min	Max	Min	Max	Min	Max	
f_{CNT1}	Max Counter Frequency $1/(t_{SU} + t_{CO1})$ - External Feedback	83.3		80		71.4		MHz
f_{CNT2}	Max Counter Frequency $1/(t_{CNT})$ - Internal Feedback	83.3		80		74.1		MHz
f_{MAX}	Max Frequency (Pipelined) $1/(t_{CP})$ - No Feedback	100		92.9		80		MHz
t_{SU}	Input or I/O Setup Time to CLK	6		4.5		2		ns
t_H	Input or I/O Hold Time from CLK	0		2		5		ns
t_{CO1}	CLK to Output Valid		6		8		12	ns
t_{CO2}	CLK to Output Valid Fed Through Combinatorial Macrocell		16		18		22	ns
t_{CNT}	Register Output Feedback to Register Input—Internal Path		12		12.5		13.5	ns
t_{CL}	CLK Low Time	4.5		4.5		5		ns
t_{CH}	CLK High Time	4.5		4.5		5		ns
t_{CP}	CLK Period	10		10.5		12.5		ns

REGISTER MODE—iFX740-10 CLOCK A.C. CHARACTERISTICS

(T_A = 0°C to +70°C, V_{CC} = 5.0V ±5%)

Symbol	Parameter	Synchronous		Delayed Sync		Async		Units
		Min	Max	Min	Max	Min	Max	
f_{CNT1}	Max Counter Frequency $1/(t_{SU} + t_{CO1})$ - External Feedback	80		76.9		71.4		MHz
f_{CNT2}	Max Counter Frequency $1/(t_{CNT})$ - Internal Feedback	80		76.9		71.4		MHz
f_{MAX}	Max Frequency (Pipelined) $1/(t_{CP})$ - No Feedback	100		92.9		80		MHz
t_{SU}	Input or I/O Setup Time to CLK	6		4.5		2		ns
t_H	Input or I/O Hold Time from CLK	0		2		5		ns
t_{CO1}	CLK to Output Valid		6.5		8.5		12	ns
t_{CO2}	CLK to Output Valid Fed Through Combinatorial Macrocell		16.5		18.5		22.5	ns
t_{CNT}	Register Output Feedback to Register Input—Internal Path		12.5		13		14	ns
t_{CL}	CLK Low Time	4.5		4.5		5		ns
t_{CH}	CLK High Time	4.5		4.5		5		ns
t_{CP}	CLK Period	10		10.5		12.5		ns

NOTE:

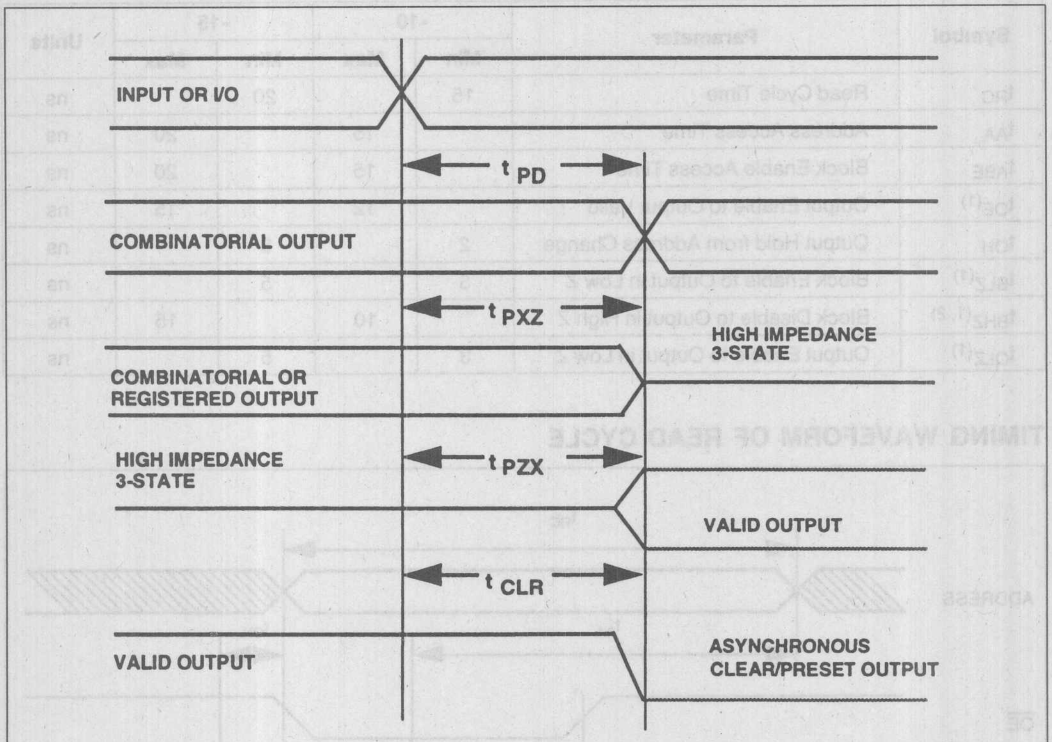
8. T_{PZX} and t_{PXZ} are measured at ±0.5V from steady state voltage as driven by specified output load. t_{PXZ} is measured with A C_L = 5 pF. Z → H and Z → L are measured at 1.5V on output.

REGISTER MODE—iFX740-15/iFX740Z-15 CLOCK A.C. CHARACTERISTICS

($T_A = 0°C$ to $+70°C$, $V_{CC} = 5.0V \pm 5\%$)

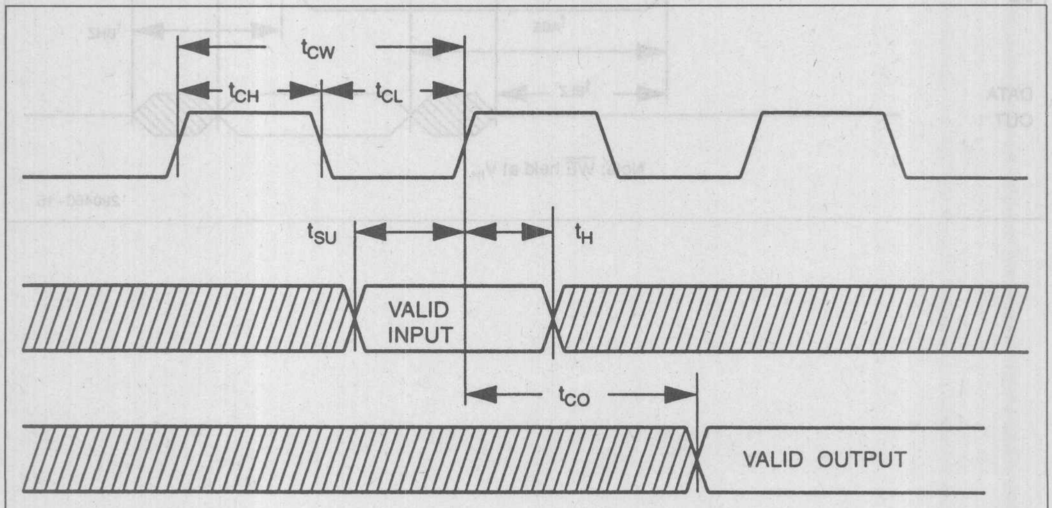
Symbol	Parameter	Synchronous		Delayed Sync		Async		Units
		Min	Max	Min	Max	Min	Max	
f_{CNT1}	Max Counter Frequency $1/(t_{SU} + t_{CO1})$ - External Feedback	50		50		50		MHz
f_{CNT2}	Max Counter Frequency $1/(t_{CNT})$ - Internal Feedback	50		50		50		MHz
f_{MAX}	Max Frequency (Pipelined) $1/(t_{CP})$ - No Feedback	66.7		62.5		62.5		MHz
t_{SU}	Input or I/O Setup Time to CLK	11		8		3		ns
t_H	Input or I/O Hold Time from CLK	0		2		6		ns
t_{CO1}	CLK to Output Valid		9		12		17	ns
t_{CO2}	CLK to Output Valid Fed Through Combinatorial Macrocell		24		27		32	ns
t_{CNT}	Register Output Feedback to Register Input—Internal Path		20		20		20	ns
t_{CL}	CLK Low Time	7		7		7		ns
t_{CH}	CLK High Time	7		7		7		ns
t_{CP}	CLK Period	15		15		15		ns

COMBINATORIAL MODE WAVEFORMS



290460-13

REGISTERED MODE WAVEFORMS

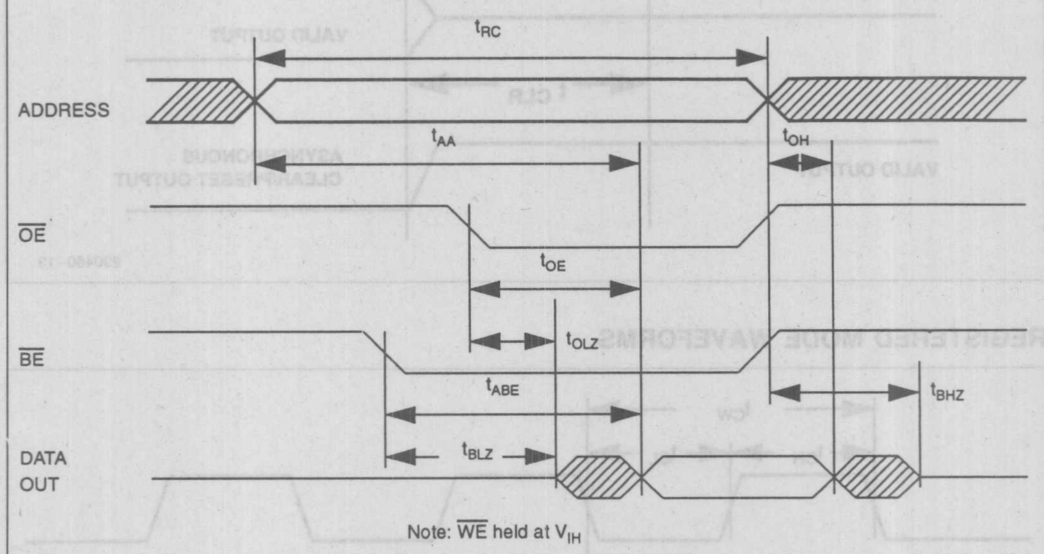


290460-14

SRAM READ—A.C. CHARACTERISTICS ($T_A = 0°C$ to $+70°C$, $V_{CC} = 5.0V \pm 5\%$)

Symbol	Parameter	-10		-15		Units
		Min	Max	Min	Max	
t_{RC}	Read Cycle Time	15		20		ns
t_{AA}	Address Access Time		15		20	ns
t_{ABE}	Block Enable Access Time		15		20	ns
t_{OE}(1)	Output Enable to Output Valid		12		15	ns
t_{OH}	Output Hold from Address Change	2		3		ns
t_{BLZ}(1)	Block Enable to Output in Low Z	3		5		ns
t_{BHZ}(1, 2)	Block Disable to Output in High Z		10		15	ns
t_{OLZ}(1)	Output Enable to Output in Low Z	3		5		ns

TIMING WAVEFORM OF READ CYCLE



290460–15

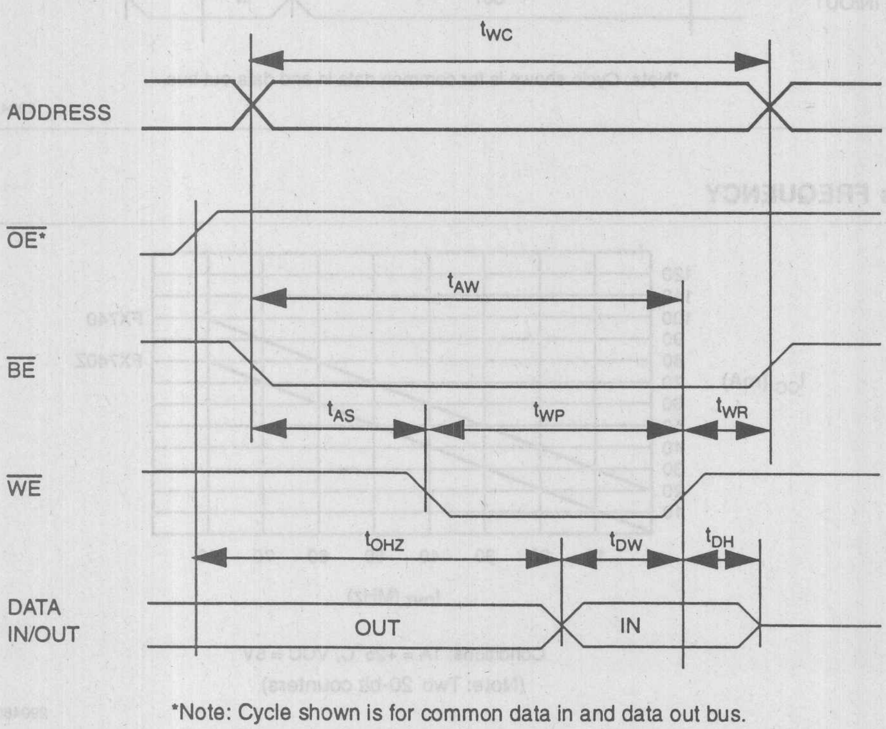
SRAM WRITE—A.C. CHARACTERISTICS ($T_A = 0°C$ to $+70°C$, $V_{CC} = 5.0V \pm 5\%$)

Symbol	Parameter	-10		-15		Units
		Min	Max	Min	Max	
t_{WC}	Write Cycle Time	15		20		ns
t_{BW}	Block Enable to End of Write	10		13		ns
t_{AW}	Address Valid to End of Write	13		17		ns
t_{AS}	Address Set-up Time	3		4		ns
t_{WP}	Write Pulse Width	10		13		ns
t_{WR}	Write Recovery Time	2		3		ns
t_{DW}	Data Valid to End of Write	10		13		ns
t_{DH}	Data Hold Time	2		3		ns
t_{OHZ}(1, 2, 3)	Output Disable to Valid Data In	10		13		ns

NOTES:
1. These signals are measured at ±0.5V from steady state voltage as driven by specified output load. Z → H and Z → L are measured at 1.5V on output.
2. These signals are measured with $C_L = 5$ pF.
3. Does not apply for separate data in and data out buses.

2

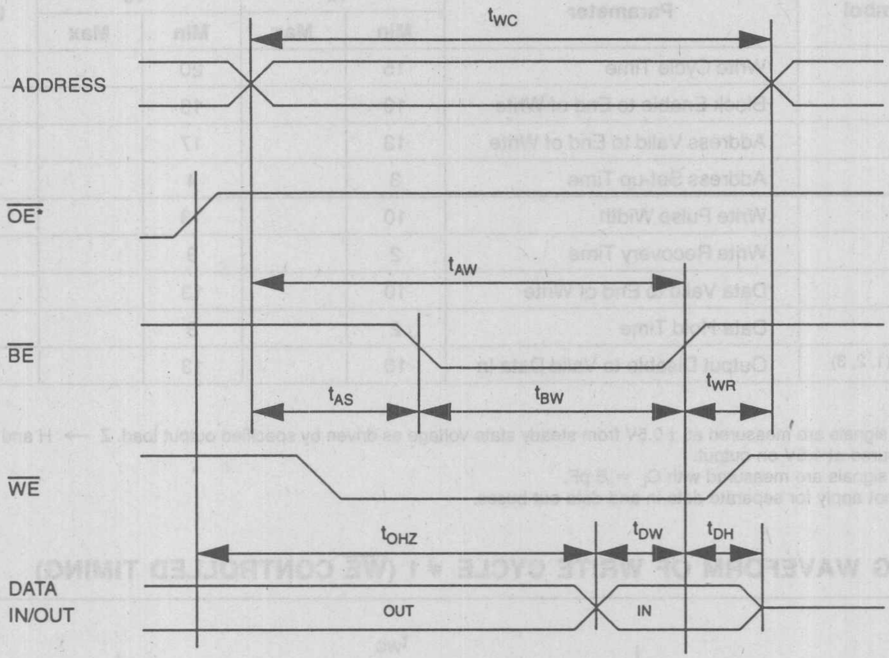
TIMING WAVEFORM OF WRITE CYCLE #1 ($\overline{WE}$ CONTROLLED TIMING)



*Note: Cycle shown is for common data in and data out bus.

290460–16

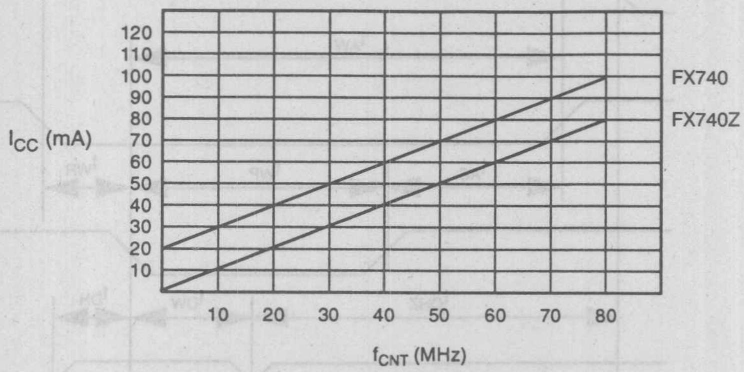
TIMING WAVEFORM OF WRITE CYCLE #2 ($\overline{BE}$ CONTROLLED TIMING)



*Note: Cycle shown is for common data in and data out bus.

290460–17

I_{CC} vs FREQUENCY



Conditions: TA = +25°C, VCC = 5V

(Note: Two 20-bit counters)

290460–18

POWER-UP RESET

Because V_{CC} rise can vary significantly from one application to another, V_{CC} rise must be monotonic. The power-up cycle is complete within a delay of t_{PR} after V_{CC} reaches the V_{ON} value.

Internal power-up reset circuits ensure that all flip-flops will be reset to a logic 0 after the device has powered-up. Also, the JTAG TAP controller will be put into the *Test-Logic-Reset* state. The outputs on an unprogrammed device will power-up in a high impedance state.

POWER-UP RESET CHARACTERISTICS

Symbol	Parameter	Value
t_{PR}	Power-Up Reset Time	100 μs Max
V_{ON}	Turn-On Voltage	4.75V Min

PIN DESCRIPTIONS

Table 4 lists the dedicated pin names and descriptions.

Table 4. Dedicated Pins

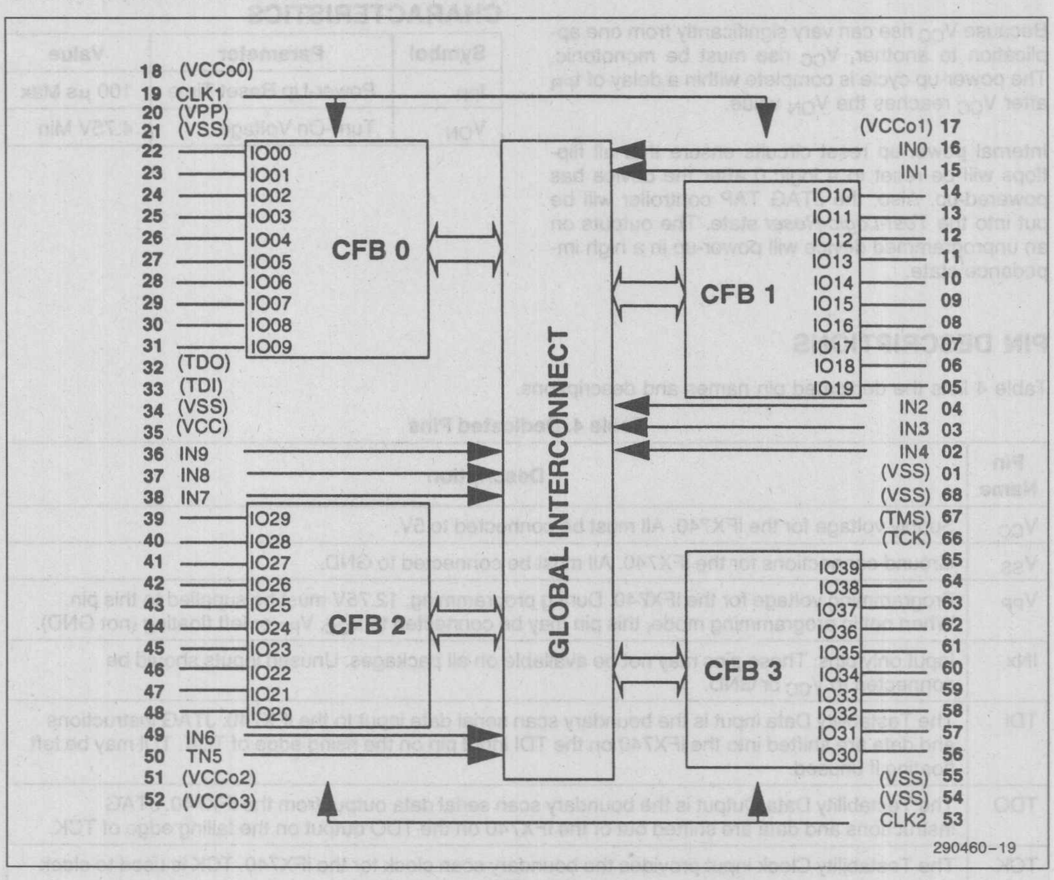
Pin Name	Description
V_{CC}	Supply voltage for the iFX740. All must be connected to 5V.
V_{SS}	Ground connections for the iFX740. All must be connected to GND.
V_{PP}	Programming voltage for the iFX740. During programming, 12.75V must be supplied to this pin. When not in programming mode, this pin may be connected to V_{CC}, V_{PP} or left floating (not GND).
INx	Input only pins. These pins may not be available on all packages. Unused inputs should be connected to V_{CC} or GND.
TDI	The Testability Data input is the boundary scan serial data input to the iFX740. JTAG instructions and data are shifted into the iFX740 on the TDI input pin on the rising edge of TCK. TDI may be left floating if unused.
TDO	The Testability Data Output is the boundary scan serial data output from the iFX740. JTAG instructions and data are shifted out of the iFX740 on the TDO output on the failing edge of TCK.
TCK	The Testability Clock input provides the boundary scan clock for the iFX740. TCK is used to clock state information and data into and out of the iFX740 during boundary scan or programming modes. The maximum operating frequency of the boundary scan test clock is 8 MHz. TCK may be left floating if unused.
TMS	The Testability Control input is the boundary scan test mode select for the iFX740. TMS may be left floating if unused.

Table 5 lists the user-defined pin names and descriptions.

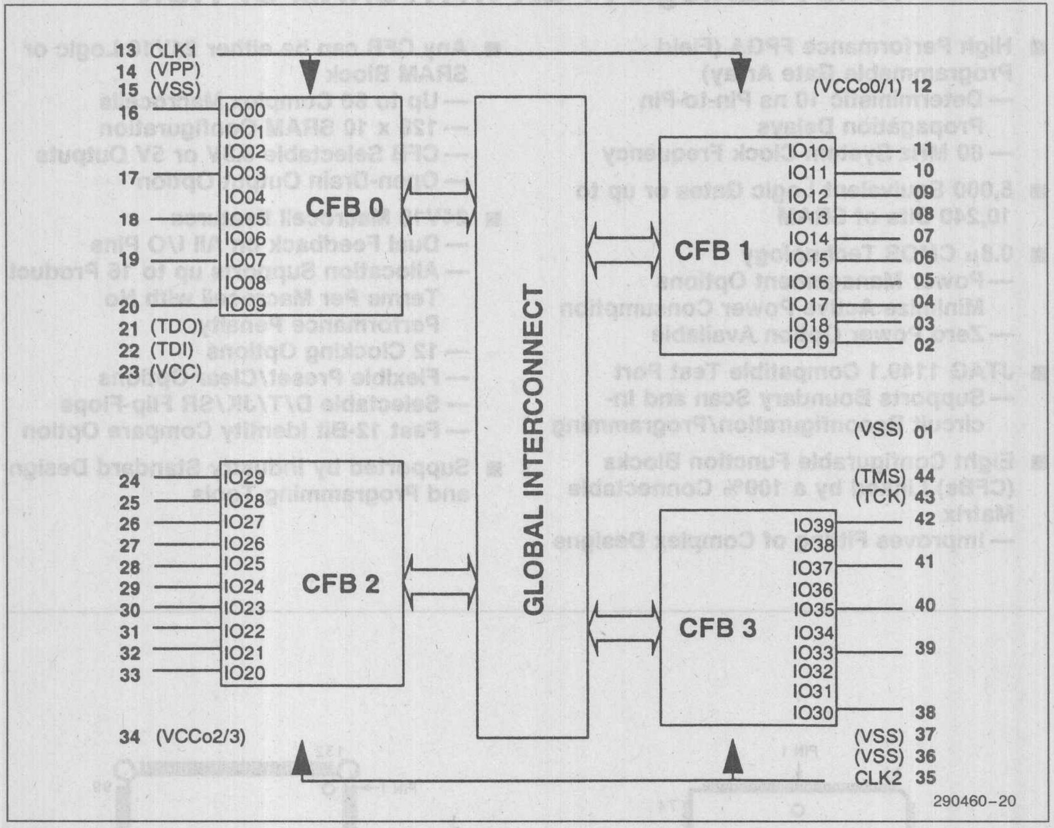
Table 5. User-defined Pins

Pin Name	Description
V_{CCOx}	Supply voltage for the outputs of the CFBs. Connecting these pins to +5V causes the CFB to output 5V signals. Connecting these pins to +3.3V causes the CFB to output 3.3V signals. These pins must always be connected to the desired output drive voltage.
CLKx	Global clocks.
I/Oxx	Pins that can be configured either as an input or an output. Unused I/O pins should be connected to V_{CC} or GND.

68-PIN PLCC PACKAGE



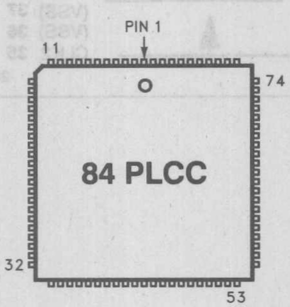
44-PIN PLCC PACKAGE



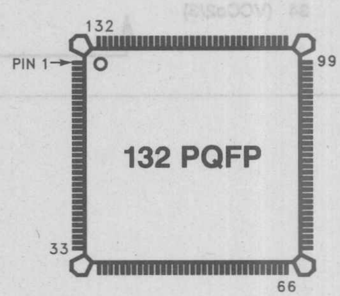
290460–20

iFX780
10 ns FLEXlogic FPGA WITH SRAM OPTION

- High Performance FPGA (Field Programmable Gate Array)
  - Deterministic 10 ns Pin-to-Pin Propagation Delays
  - 80 MHz System Clock Frequency
- 5,000 Equivalent Logic Gates or up to 10,240 Bits of SRAM
- 0.8μ CMOS Technology
  - Power Management Options Minimize Active Power Consumption
  - Zero Power Option Available
- JTAG 1149.1 Compatible Test Port
  - Supports Boundary Scan and In-circuit Reconfiguration/Programming
- Eight Configurable Function Blocks (CFBs) Linked by a 100% Connectable Matrix
  - Improves Fitting of Complex Designs
- Any CFB can be either 24V10 Logic or SRAM Block
  - Up to 80 Complex Macrocells
  - 128 x 10 SRAM Configuration
  - CFB Selectable 3.3V or 5V Outputs
  - Open-Drain Output Option
- 24V10 Macrocell Features
  - Dual Feedback on All I/O Pins
  - Allocation Supports up to 16 Product Terms Per Macrocell with No Performance Penalty
  - 12 Clocking Options
  - Flexible Preset/Clear Options
  - Selectable D/T/JK/SR Flip-Flops
  - Fast 12-Bit Identity Compare Option
- Supported by Industry Standard Design and Programming Tools



290459–1



290459–2

Package Options

Pins	Package	Macrocells	I/O	Inputs	Clock	JTAG/V_{PP}	V_{CC}	GND
84	PLCC	80	60	0	2	5	8	9
132	PQFP	80	80	22	2	5	10	13

November 1993
Order Number: 290459-004

INTRODUCTION

The iFX780 is the first member of the Intel FLEXlogic FPGA (Field Programmable Gate Array) family. The iFX780 consists of eight configurable function blocks (CFBs) linked by a 100% connectable matrix. Each CFB can be defined either as a 24V10 logic block or as a block of 128 x 10 SRAM. This combination will provide approximately 5,000 gates of logic in either PLCC or PQFP packages.

Flexible Performance

The iFX780 uses Intel's 0.8μ CHMOS EPROM technology to provide an 80 MHz external clock frequency with predictable 10 ns pin-to-pin delays. This advanced process technology combined with power management options enables very low active and standby power consumption.

Flexible Features

The unique combination of features available in the iFX780 make it ideal for a wide variety of applications. For example, the high pertormance and flexible clock options provided are designed to support functions such as bus control, custom cache control, and DRAM control for the current and next generation of Intel microprocessors. The very low power consumption and user selectable 5V/3.3V outputs allow the iFX780 to be used in mixed voltage applications such as portable or embedded systems where CPUs operating at 3.3V still need to communicate to 5V peripherals. The combination of SRAM and logic in a single device becomes a big advantage when designing communication controllers or bus interface controllers where memory is required for buffering data in addition to the logic for the controller design itself.

Flexible Testing and Programming

The iFX780 also provides dedicated JTAG 1149.1 compatible pins to support boundary scan, in-circuit reconfiguration, and programming modes. In-circuit reconfiguration not only allows the designer ultimate flexibility in prototyping new designs, but also supports applications where the final configuration is not fixed. New configurations may be downloaded to the iFX780 upon power-up to reflect changes in system organization or design requirements that cannot be determined at production time.

Flexible Tools Support

The FLEXlogic FPGA family is supported by industry standard design entry/programming environments including Intel's PLDshell Plus™ software. This software runs on Intel 386 or higher PC-compatible platforms.

INTERCONNECT

The Global Interconnect Matrix that connects each of the CFB blocks is 100% connectable. Any combination of signals in the matrix can be routed into any CFB block, up to the maximum fan-in of the block (24).

This high degree of connectivity between CFB blocks eliminates routing problems during rework of a complex design.

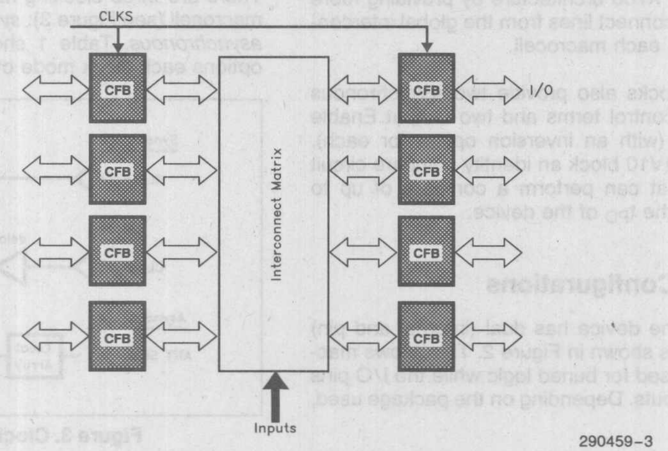


Figure 1. Interconnect Matrix

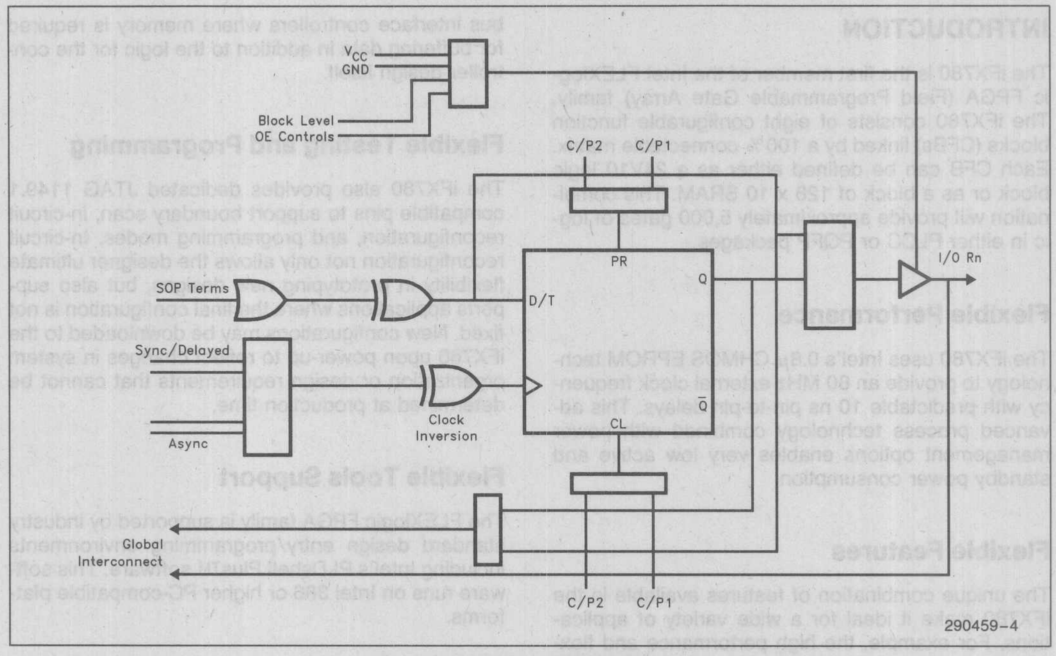


Figure 2. CFB as 24V10 Block

CONFIGURABLE FUNCTION BLOCKS

24V10 Mode

Each 24V10 block contains a product term array, a P-Term Allocation circuit, 10 macrocells, clocks and I/O logic in the familiar architecture of a simple PLD.

The 24V10 CFB blocks have a superior fan-in to macrocell ratio (2.4:1). This improves the fitting capacity of the iFX780 architecture by providing more available interconnect lines from the global interconnect matrix for each macrocell.

The 24V10 blocks also provide two asynchronous Clear/Preset control terms and two Output Enable control terms (with an inversion option for each). Within each 24V10 block an identity compare circuit is available that can perform a compare of up to 12 bits within the t_{PD} of the device.

Macrocell Configurations

Each I/O of the device has dual (internal and pin) feedback paths shown in Figure 2. This allows macrocells to be used for buried logic while the I/O pins are used as inputs. Depending on the package used, some macrocell outputs may not be brought outside the package. These I/Os may still be used to provide buried logic since internal feedback is available. The macrocells can be configured either as a fast combinatorial block, a D-register, or a T-register. J/K and S/R registers are available as software emulations.

Clocking Modes

There are three clocking modes available for every macrocell (see Figure 3): *synchronous, delayed, and asynchronous*. Table 1 shows the different timing options each clock mode offers.

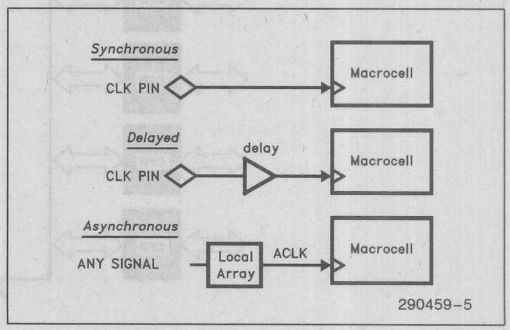


Figure 3. Clocking Modes

Synchronous is the standard clock mode where the register clock is driven directly from one of the two global clock pins.

Delayed clock is similar to *synchronous*, but there is a local delay added (within the CFB) to either of the two synchronous clock signals.

Asynchronous mode is where the register clock uses one of the two local CFB ACLK product terms.

Table 1. Clock Mode Timings for iFX780Z

Mode	T_{SU}	T_{HOLD}	T_{CO}
Synchronous	6	0	6
Delayed	4.5	2	8
Asynchronous	2	5	12

Clock Mode Timings for iFX780

Mode	T_{SU}	T_{HOLD}	T_{CO}
Synchronous	6	0	6.5
Delayed	4.5	2	8.5
Asynchronous	2	5	12

In addition, each clocking mode may be inverted to allow the macrocell register to be clocked either on the rising or falling edge of the clock signal. This combination provides up to twelve different clock options for each macrocell.

Control Signals

There are 4 control signals in each CFB in addition to the clocks (see Figure 4). These include two Output Enable (OE) signals, and two asynchronous Clear/Preset signals. Each control signal is generated by a single product term from the local 24V10 AND array with an inversion option. This allows multiple product term control equations to be implemented.

Comparator Logic

Each 24V10 block provides a comparator circuit (see Figure 5). This circuit can do an identity compare of up to 12 signals, within the T_{PD} of the device.

2

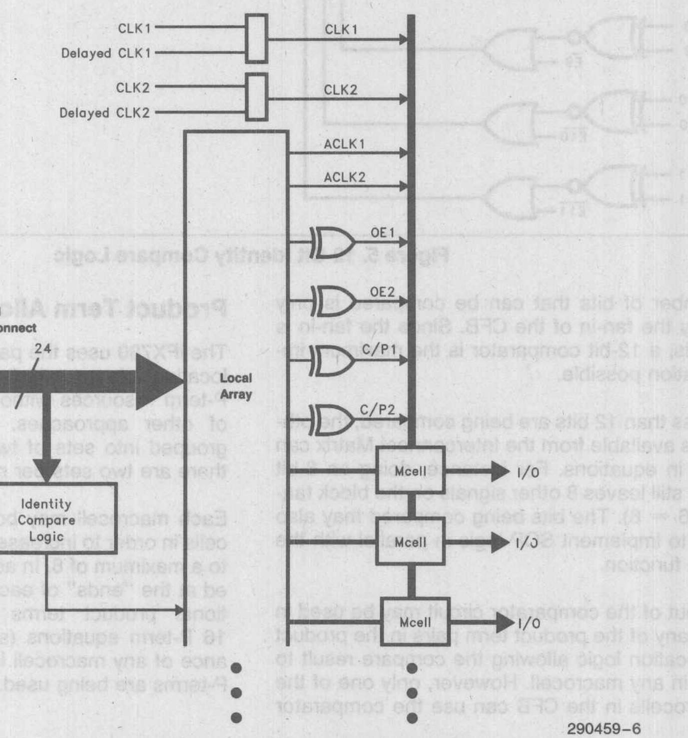


Figure 4. Control Signals

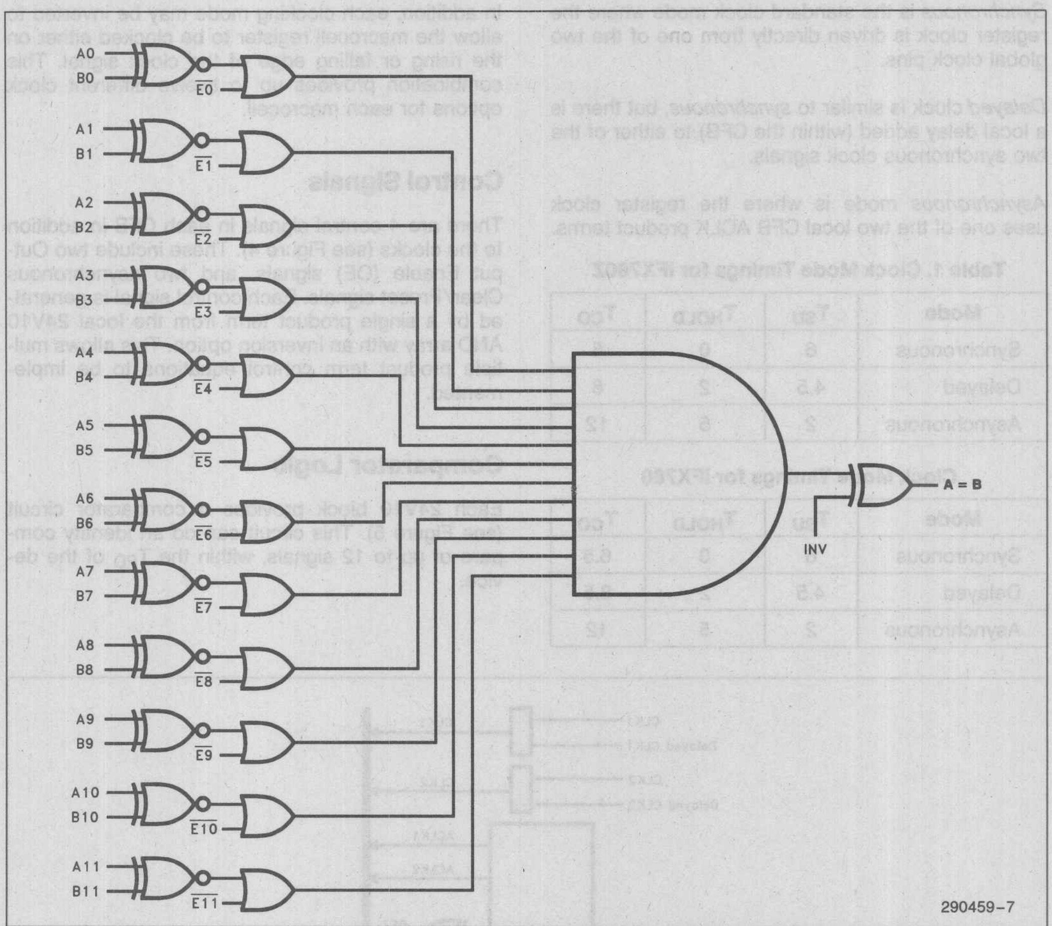


Figure 5. 12-Bit Identity Compare Logic

The number of bits that can be compared is only limited by the fan-in of the CFB. Since the fan-in is 24 signals, a 12-bit comparator is the maximum implementation possible.

When less than 12 bits are being compared, the other signals available from the Interconnect Matrix can be used in equations. For instance, doing an 8-bit compare still leaves 8 other signals on the block fan-in (24−16 = 8). The bits being compared may also be used to implement SOP logic in parallel with the compare function.

The output of the comparator circuit may be used in place of any of the product term pairs in the product term allocation logic allowing the compare result to be used in any macrocell. However, only one of the ten macrocells in the CFB can use the comparator output.

Product Term Allocation

The iFX780 uses the patented Intel product term allocation scheme, which gives better utilization of the P-term resources without the performance penalty of other approaches. The P-terms are typically grouped into sets of two product terms each, and there are two sets per macrocell.

Each macrocell may borrow from adjacent macrocells in order to increase the total number of P-terms to a maximum of 8. In addition, the macrocells located at the "ends" of each CFB have access to additional product terms and can support up to 16 P-term equations (see Figure 6). The performance of any macrocell is the same whether 2 or 16 P-terms are being used.

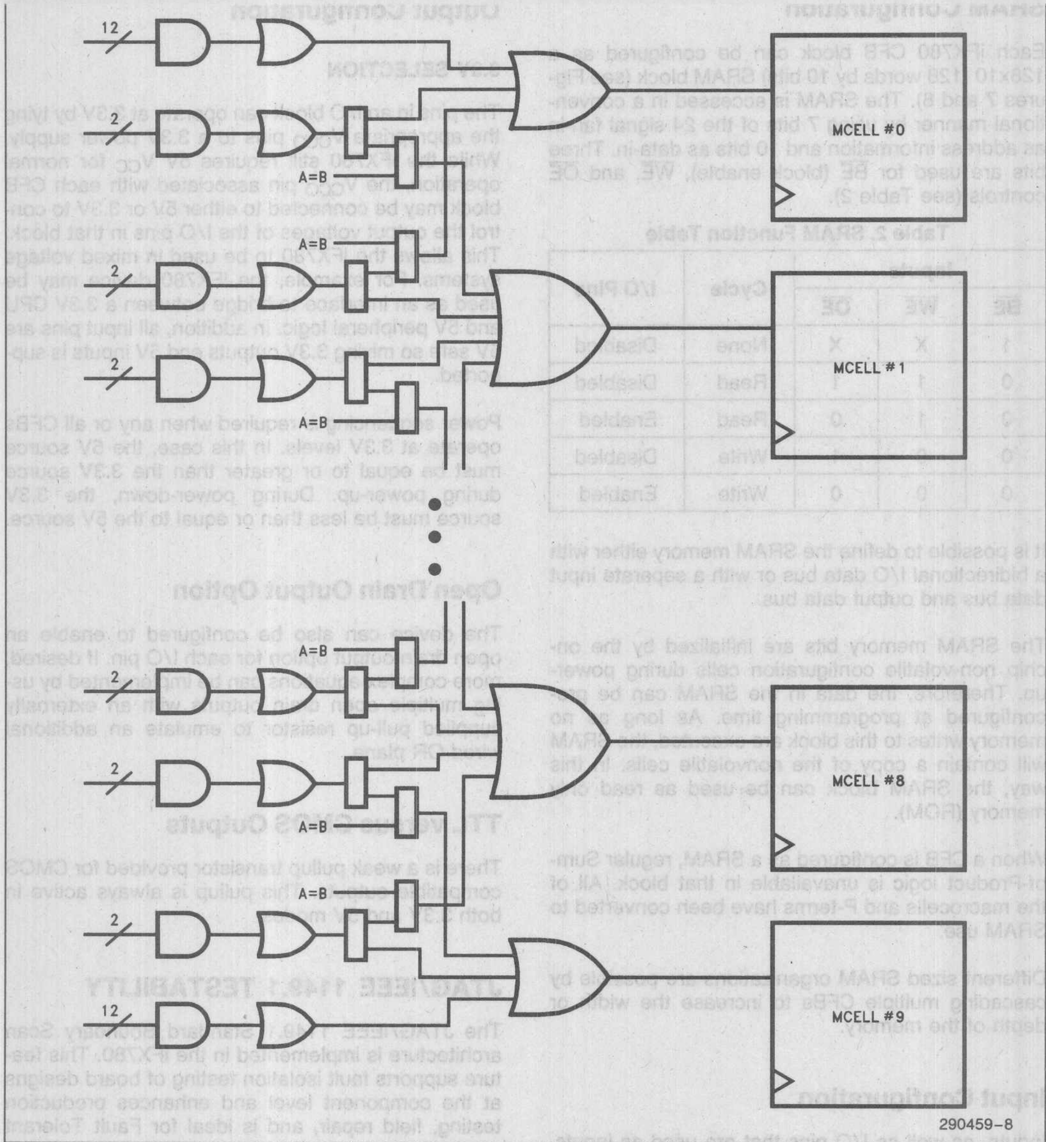


Figure 6. CFB Product Terms

2

SRAM Configuration

Each iFX780 CFB block can be configured as a 128x10 (128 words by 10 bits) SRAM block (see Figures 7 and 8). The SRAM is accessed in a conventional manner by using 7 bits of the 24 signal fan-in as address information and 10 bits as data-in. Three bits are used for $\overline{BE}$ (block enable), $\overline{WE}$, and $\overline{OE}$ controls (see Table 2).

Table 2. SRAM Function Table

Inputs			Cycle	I/O Pins
$\overline{BE}$	$\overline{WE}$	$\overline{OE}$		
1	X	X	None	Disabled
0	1	1	Read	Disabled
0	1	0	Read	Enabled
0	0	1	Write	Disabled
0	0	0	Write	Enabled

It is possible to define the SRAM memory either with a bidirectional I/O data bus or with a separate input data bus and output data bus.

The SRAM memory bits are initialized by the on-chip non-volatile configuration cells during power-up. Therefore, the data in the SRAM can be pre-configured at programming time. As long as no memory writes to this block are executed, the SRAM will contain a copy of the nonvolatile cells. In this way, the SRAM block can be used as read only memory (ROM).

When a CFB is configured as a SRAM, regular Sum-of-Product logic is unavailable in that block. All of the macrocells and P-terms have been converted to SRAM use.

Different sized SRAM organizations are possible by cascading multiple CFBs to increase the width or depth of the memory.

Input Configuration

Inputs, as well as I/O pins that are used as inputs, can be optimized for minimum standby current during either CMOS or TTL operation by using the "CMOS_LEVEL" and "TTL_LEVEL" keywords available in the PLDasm design language of PLDshell Plus. For 5V CMOS inputs the "CMOS_LEVEL" keyword should be used to reduce standby power consumption. For TTL or 3V CMOS inputs, the "TTL_LEVEL" keyword (the default condition for PLDasm) should be used. For additional information refer to Application Brief AB-27, Order Number 292107-001.

Output Configuration

3.3V SELECTION

The pins in an I/O block can operate at 3.3V by tying the appropriate V_{CCO} pins to a 3.3V power supply. While the iFX780 still requires 5V V_{CC} for normal operation, the V_{CCO} pin associated with each CFB block may be connected to either 5V or 3.3V to control the output voltages of the I/O pins in that block. This allows the iFX780 to be used in mixed voltage systems. For example, the iFX780 device may be used as an interface to bridge between a 3.3V CPU and 5V peripheral logic. In addition, all input pins are 5V safe so mixing 3.3V outputs and 5V inputs is supported.

Power sequencing *is* required when any or all CFBs operate at 3.3V levels. In this case, the 5V source must be equal to or greater than the 3.3V source during power-up. During power-down, the 3.3V source must be less than or equal to the 5V source.

Open Drain Output Option

The device can also be configured to enable an open drain output option for each I/O pin. If desired, more complex equations can be implemented by using multiple open drain outputs with an externally supplied pull-up resistor to emulate an additional wired OR plane.

TTL versus CMOS Outputs

There is a weak pullup transistor provided for CMOS compatible outputs. This pullup is always active in both 3.3V and 5V modes.

JTAG/IEEE 1149.1 TESTABILITY

The JTAG/IEEE 1149.1 Standard Boundary Scan architecture is implemented in the iFX780. This feature supports fault isolation testing of board designs at the component level and enhances production testing, field repair, and is ideal for Fault Tolerant applications.

The iFX780 boundary scan support consists of an Instruction Register, a Data Register, scan cells, and associated logic which are accessed through the Test Access Port (TAP). The TAP interface consists of three inputs: Test Mode Select (TMS), Test Data In (TDI) and Test Clock (TCK), and one output: Test Data Out (TDO).

The boundary scan cells of the iFX780 external signals are linked to form a shift register chain for all active pins. This chain provides a path which can be used to shift in test stimulus as well as shift out test response data for inspection.

For example, a continuity test may be performed between two JTAG devices on a circuit board by placing a known value on the output buffers of one device while observing the input buffers of the other device. This same technique may be used to perform simple in-circuit functional testing of the iFX780 for prototyping new system designs.

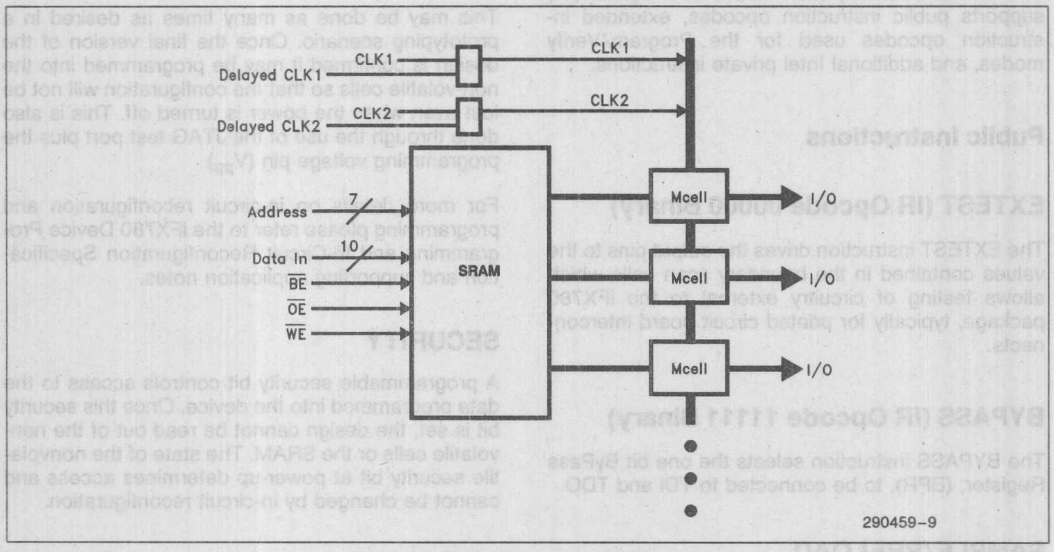


Figure 7. SRAM Overall Block Diagram

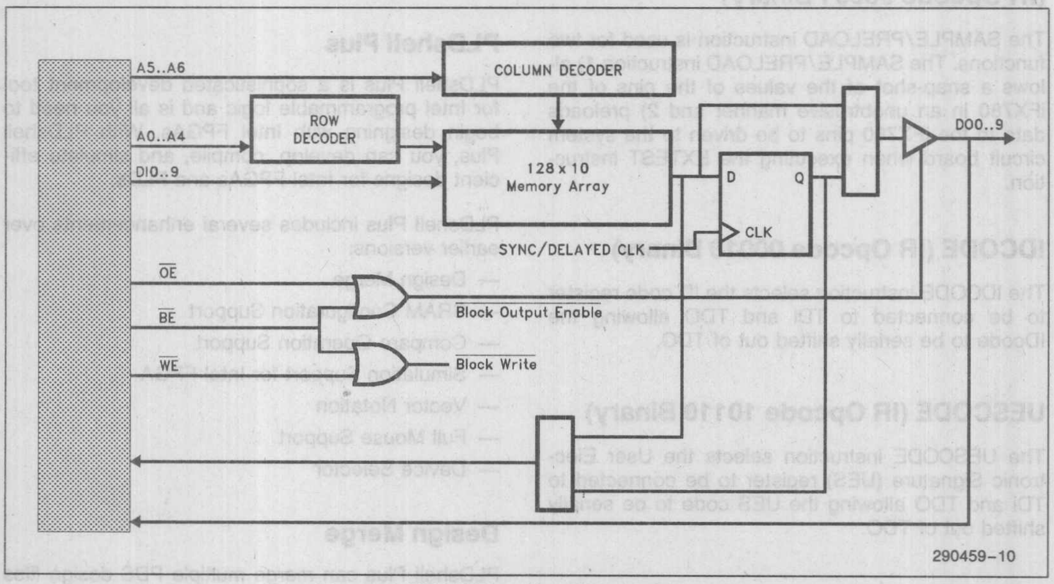


Figure 8. SRAM Functional Block Diagram

The 4-pin JTAG test interface is also used for standard programming, in-circuit reconfiguration, and in-circuit programming.

Boundary Scan Instructions

The iFX780 boundary scan Instruction Register (IR) supports public instruction opcodes, extended instruction opcodes used for the Program/Verify modes, and additional Intel private instructions.

Public Instructions

EXTEST (IR Opcode 00000 Binary)

The EXTEST instruction drives the output pins to the values contained in the boundary scan cells which allows testing of circuitry external to the iFX780 package, typically for printed circuit board interconnects.

BYPASS (IR Opcode 11111 Binary)

The BYPASS instruction selects the one bit ByPass Register, (BPR), to be connected to TDI and TDO.

SAMPLE/PRELOAD (IR Opcode 00001 Binary)

The SAMPLE/PRELOAD instruction is used for two functions. The SAMPLE/PRELOAD instruction 1) allows a snap-shot of the values of the pins of the iFX780 in an unobtrusive manner and 2) preloads data to the iFX780 pins to be driven to the system circuit board when executing the EXTEST instruction.

IDCODE (IR Opcode 00010 Binary)

The IDCODE instruction selects the ID code register to be connected to TDI and TDO allowing the IDcode to be serially shifted out of TDO.

UESCODE (IR Opcode 10110 Binary)

The UESCODE instruction selects the User Electronic Signature (UES) register to be connected to TDI and TDO allowing the UES code to be serially shifted out of TDO.

HIZ (IR Opcode 01000 Binary)

The HIZ instruction sets all I/Os to a high impedance state.

IN-CIRCUIT RECONFIGURATION

The iFX780 supports in-circuit reconfiguration and in-circuit programming through the use of the 4-pin JTAG test port. Downloading a new configuration can be accomplished by simply shifting the new data into the device.

This may be done as many times as desired in a prototyping scenario. Once the final version of the design is confirmed it may be programmed into the non-volatile cells so that the configuration will not be lost even when the power is turned off. This is also done through the use of the JTAG test port plus the programming voltage pin (V_{PP}).

For more details on in-circuit reconfiguration and programming please refer to the iFX780 Device Programming and In-Circuit Reconfiguration Specification and supporting application notes.

SECURITY

A programmable security bit controls access to the data programmed into the device. Once this security bit is set, the design cannot be read out of the non-volatile cells or the SRAM. The state of the nonvolatile security bit at power-up determines access and cannot be changed by in-circuit reconfiguration.

SOFTWARE SUPPORT

PLDshell Plus

PLDshell Plus is a sophisticated development tool for Intel programmable logic and is all you need to begin designing with Intel FPGAs. With PLDshell Plus, you can develop, compile, and simulate efficient designs for Intel FPGAs and PLDs.

PLDshell Plus includes several enhancements over earlier versions:

- Design Merge
- SRAM Configuration Support
- Compare Operation Support
- Simulation Support for Intel FPGA
- Vector Notation
- Full Mouse Support
- Device Selector

Design Merge

PLDshell Plus can merge multiple PDS design files into any Intel PLD, including the Intel iFX780. The Merge function makes it easy for designers to consolidate multiple PLDs into a single, high-performance FPGA or PLD.

FPGA Architectural Feature Support

PLDshell Plus supports all of the innovative architectural features of the iFX780 through the implementation of new language syntax such as:

— SRAM configuration

— Compare operation

— Buried macrocells

— Clocking options

— 3.3V and 5V options

Functional Simulation

PLDshell Plus allows the designer to simulate the internal function of any Intel FPGA or PLD for rapid design verification.

PLDshell Plus provides the following simulation capabilities:

— Event-driven simulation of combinatorial, registered, and state machine designs

— Ability to set any input, preload any register, and compare any output against an expected value

— Ability to group signals together (form a vector) to simulate a bus

— Generation of test vectors from simulation results for inclusion in the JEDEC file

— Simulation history file with ability to output a subset of signals to a secondary trace file

Device Selector

The designer can develop the logic design first, and then use the PLDshell Plus device selector to pick a list of appropriate devices. After a design is compiled or estimated through PLDshell Plus a report file is generated. Contained in the report file is a listing of suggested devices appropriate for the target design.

System Requirements

Listed below are the minimum requirements for a system in order to use PLDshell Plus:

— Intel 386 based PC compatible (or better)

— 4MB RAM (minimum)

— VGA monitor/adaptor

— DOS 3.1 (or later)

THIRD-PARTY SUPPORT DESIGN SOFTWARE

Third party tools support will be provided by the following vendors:

- Cadence
  — Composer*: Comprehensive suite of design entry, debug and documentation capabilities.
  — Verilog-XL*: Digital logic simulators and interactive debug environment.
- Data I/O
  — ABEL*: Design software allowing you to describe and implement logic designs.
- Logical Devices
  — CUPL*: High level, universal design software package.
- Mentor Graphics
  — Design Architect*: Integrated system of schematic, symbol, and text editors for capturing designs.
  — QuickSim*: High performance logic simulator for function and performance verification.
- Minc
  — PLDesigner-XL*: Powerful design tool that can be used for all types of programmable logic with automatic device selection, automatic partitioning and functional simulation.
- OrCAD
  — PLD Tools & Schematic Design Tool*: Software tool environment including schematic entry, test vector generation and multiple forms of input.
  — Verification/Simulation Tool*: Series of software tools for performing timing-based simulation of designs.

2

- Viewlogic
  - — ViewPLD & Powerview™: Integrated schematic capture and simulation environment.

PROGRAMMING SUPPORT

Programming Support will be provided by a number of leading vendors, such as:

- Advin Systems, Inc.
  - — PILOT-U84
  - — PILOT-U40
- B & C Microsystems, Inc.
  - — PROTEUS-UPLC88
- BP Microsystems
  - — PLD 1100
- Data I/O
  - — Unisite
  - — Unisite 2900/3900
- Products in Motion
  - — FLEXlogic Programmer
- Elan
  - — Model 6000
- Logical Devices
  - — ALLPRO
- SMS
  - — Sprint Plus

DEVICE MODELS

Simulation models will be provided by the following vendors:

- Logic Modeling Corporation
  - — Smart Model: Device model support for behavioral simulation through a variety of simulators.
- Viewlogic

ORDERING INFORMATION

f_{CNT1} (MHz)	F_{MAX} (MHz)	t_{PD} (ns)	I_{SB} (mA)	I_{CC} (mA/MHz)	Order Code	Package
80	100	10	20	1.5	KUFX780-10	132-Pin PQFP
					NFX780-10	84-Pin PLCC
50	66.7	15	20	1.5	KUFX780-15	132-Pin PQFP
					NFX780-15	84-Pin PLCC
80	100	10	1	1.5	KUFX780Z-10	132-Pin PQFP
					NFX780Z-10	84-Pin PLCC
50	66.7	15	1	1.5	KUFX780Z-15	132-Pin PQFP
					NFX780Z-15	84-Pin PLCC

ABSOLUTE MAXIMUM RATINGS*

Symbol	Parameter	Min	Max	Units
V_{CC}	Supply Voltage(1)	−2.0	+7.0	V
V_{PP}	Programming Supply Voltage(1)	−2.0	+13.5	V
V_I	DC Input Voltage(1, 2)	−0.5	V_{CC} + 0.5	V
t_{STG}	Storage Temperature	−65	+150	°C
t_{AMB}	Ambient Temperature(3)	−10	+85	°C

NOTICE: This data sheet contains preliminary information on new products in production. The specifications are subject to change without notice. Verify with your local Intel Sales office that you have the latest data sheet before finalizing a design.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

NOTES:
1. Voltages with respect to ground.
2. Minimum DC input is −0.5V. During transitions, the inputs may undershoot to −2.0V or overshoot to +7.0V for periods less than 20 ns under no load conditions.
3. Under bias. Extended temperature versions are also available.

2

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Units
V_{CC}/V_{CCO}	Supply/Output Supply Voltage - 5V	4.75	5.25	V
V_{CCO}	Output Supply Voltage - 3.3V	3.0	3.6	V
V_{IN}	Input Voltage	0	V_{CC}	V
V_O	Output Voltage	0	V_{CCO}	V
T_A	Operating Temperature	0	+70	°C
t_r	Input Rise Time		500	ns
t_f	Input Fall Time		500	ns

D.C. CHARACTERISTICS (T_A = 0°C to +70°C, V_{CC} = 5.0V ±5%)(4)

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
V_{IH}(5)	High Level Input Voltage	2.0		V_{CC} + 0.3	V	
V_{IL}(5)	Low Level Input Voltage	−0.3		0.8	V	
V_{OH}	5V TTL High Level Output	2.4			V	I_{OH} = −4.0 mA D.C., V_{CC} = Min
	5V CMOS High Level Output	V_{CCO} −0.2			V	I_{OH} = −20 μA D.C., V_{CC} = Min
	3V High Level Output Voltage	V_{CCO} −0.2			V	I_{OH} = −20 μA D.C., V_{CC} = Min
V_{OL}	5V Low Level Output Voltage			0.45	V	I_{OL} = 12.0 mA D.C., V_{CC} = Min
	3V Low Level Output Voltage			0.2	V	I_{OL} = 20 μA D.C., V_{CC} = Min
I_I(6)	Input Leakage Current			±10	μA	V_{CC} = Max, V_{IN} = GND or V_{CC}

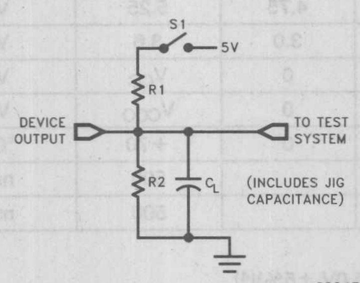
NOTES:
4. Typical values are at T_A = 25°C, V_{CC} = 5V.
5. Absolute values with respect to device GND; all over and undershoots due to system and tester noise are included. Do not attempt to test these values without suitable equipment.
6. Input leakage current on JTAG pins: ±20 μA. Input leakage current on clock pins tested at V_{IN} = GND or 4V.

D.C. CHARACTERISTICS ($T_A = 0°C$ to $+70°C$, $V_{CC} = 5.0V \pm 5\%$)(4) (Continued)

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
I_{OZ}	Output Leakage Current			±50	μA	V_{CC} = Max, V_{OUT} = GND or V_{CC}
I_{SC}(7)	Output Short Circuit Current	−30		−120	mA	V_{CC} = Max, V_{OUT} = 0.5V
I_{SB}	Standby Power Supply Current FX780		20		mA	V_{IN} = V_{CC} or GND, Outputs Open
	Standby Power Supply Current FX780Z		1		mA	
I_{CC} Active	Power Supply Current FX780		1.5		mA per MHz	V_{IN} = V_{CC} or GND, Outputs Open, Device Programmed as Four 20-Bit Counters
	Power Supply Current FX780Z		1.5		mA per MHz	

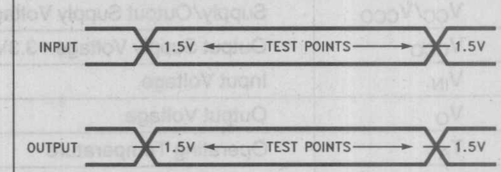
NOTE:
7. Not more than 1 output should be tested at a time. Duration of that test should not exceed 1 second.

A.C. TESTING LOAD CIRCUIT



290459–11

A.C. TESTING INPUT, OUTPUT WAVEFORM



290459–12

AC Testing: Inputs are driven at 3.0V for a logic "1" and 0V for a logic "0." Timing measurements are made at 1.5V. Outputs are measured at 1.5V. Device input rise and fall times <3 ns.

SWITCHING TEST CIRCUIT

Specification	S1	C_L	Commercial		Measured Output Value
			R1	R2	
t_{PD}	Closed	35 pF	330Ω	200Ω	1.5V
t_{PZX}	Z → H: Open Z → L: Closed				1.5V
t_{PXZ}	H → Z: Open L → Z: Closed	5 pF			H → Z: V_{OH} − 0.5V L → Z: V_{OL} + 0.5V

PIN CAPACITANCE ($T_A = 0°C$ to $+70°C$, $V_{CC} = 5.0V \pm 5\%$)(8)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 2V, f = 1.0 MHz		10	12	pF
C_{IO}	I/O Capacitance	V_{OUT} = 2V, f = 1.0 MHz		12	15	pF
C_{CLK}	Clock Pin Capacitance	V_{OUT} = 2V, f = 1.0 MHz		15	18	pF
C_{VPP}	V_{PP} Pin Capacitance	f = 1.0 MHz		12	15	pF

NOTE:
8. These values are evaluated at initial characterization and whenever design modifications occur that may affect capacitance.

COMBINATORIAL MODE A.C. CHARACTERISTICS

(T_A = 0°C to +70°C, V_{CC} = 5.0V ±5%)

Symbol	Parameter	-10 Min	-10 Typ	-10 Max	-15 Min	-15 Typ	-15 Max	Units
t_{PD}	Input or I/O to Output Valid			10			15	ns
t_{PZX}(9)	Input or I/O to Output Enable			12			18	ns
t_{PXZ}(9)	Input or I/O to Output Disable			12			18	ns
t_{CLR}	Input or I/O to Asynchronous Clear/Preset			15			20	ns
t_{COMP}	Comparator Input or I/O Feedback to Output Valid			10			15	ns

REGISTER MODE—iFX780Z-10 CLOCK A.C. CHARACTERISTICS

(T_A = 0°C to +70°C, V_{CC} = 5.0V ±5%)

Symbol	Parameter	Synchronous Min	Synchronous Max	Delayed Sync Min	Delayed Sync Max	Async Min	Async Max	Units
f_{CNT1}	Max Counter Frequency $1/(t_{SU} + t_{CO1})$—External Feedback	83.3		80		71.4		MHz
f_{CNT2}	Max Counter Frequency $1/(t_{CNT})$—Internal Feedback	83.3		80		74.1		MHz
f_{MAX}	Max Frequency (Pipelined) $1/(t_{CP})$—No Feedback	100		92.9		80		MHz
t_{SU}	Input or I/O Setup Time to CLK	6		4.5		2		ns
t_H	Input or I/O Hold Time from CLK	0		2		5		ns
t_{CO1}	CLK to Output Valid		6		8		12	ns
t_{CO2}	CLK to Output Valid Fed Through Combinatorial Macrocell		16		18		22	ns
t_{CNT}	Register Output Feedback to Register Input—Internal Path		12		12.5		13.5	ns
t_{CL}	CLK Low Time	4.5		4.5		5		ns
t_{CH}	CLK High Time	4.5		4.5		5		ns
t_{CP}	CLK Period	10		10.5		12.5		ns

NOTES:

9. t_{PZX} and t_{PXZ} are measured at ±0.5V from steady state voltage as driven by specified output load. t_{PXZ} is measured with C_L = 5 pF. Z → H and Z → L are measured at 1.5V on output.
10. Three outputs switching per block, three blocks tested simultaneously.

REGISTER MODE—iFX780-10 CLOCK A.C. CHARACTERISTICS

(T_A = 0°C to +70°C, V_{CC} = 5.0V ±5%)

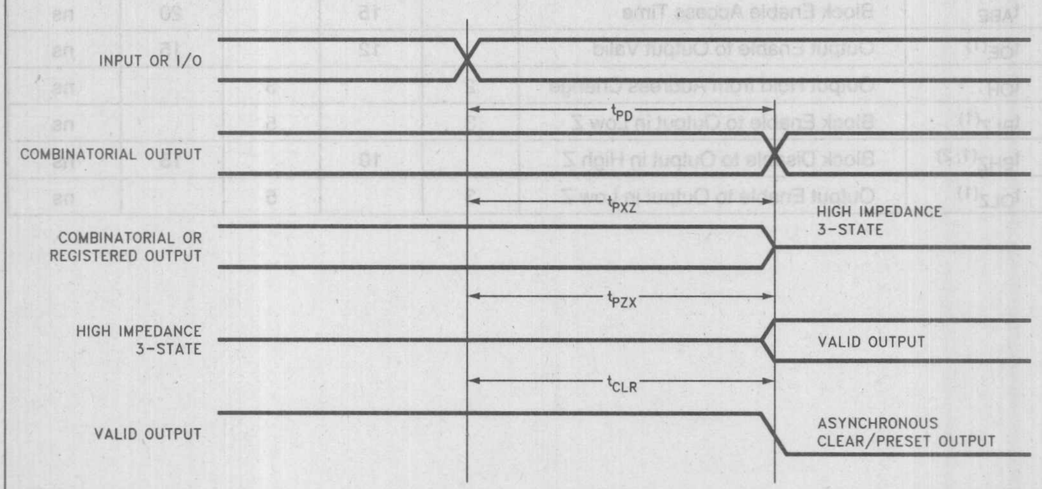
Symbol	Parameter	Synchronous		Delayed Sync		Async		Units
		Min	Max	Min	Max	Min	Max	
f_{CNT1}	Max Counter Frequency $1/(t_{SU} + t_{CO1})$—External Feedback	80		76.9		71.4		MHz
f_{CNT2}	Max Counter Frequency $1/(t_{CNT})$—Internal Feedback	80		76.9		71.4		MHz
f_{MAX}	Max Frequency (Pipelined) $1/(t_{CP})$—No Feedback	100		92.9		80		MHz
t_{SU}	Input or I/O Setup Time to CLK	6		4.5		2		ns
t_H	Input or I/O Hold Time from CLK	0		2		5		ns
t_{CO1}	CLK to Output Valid		6.5		8.5		12	ns
t_{CO2}	CLK to Output Valid Fed Through Combinatorial Macrocell		16.5		18.5		22.5	ns
t_{CNT}	Register Output Feedback to Register Input—Internal Path		12.5		13		14	ns
t_{CL}	CLK Low Time	4.5		4.5		5		ns
t_{CH}	CLK High Time	4.5		4.5		5		ns
t_{CP}	CLK Period	10		10.5		12.5		ns

REGISTER MODE—iFX780-15/iFX780Z-15 CLOCK A.C. CHARACTERISTICS

(T_A = 0°C to +70°C, V_{CC} = 5.0V ±5%)

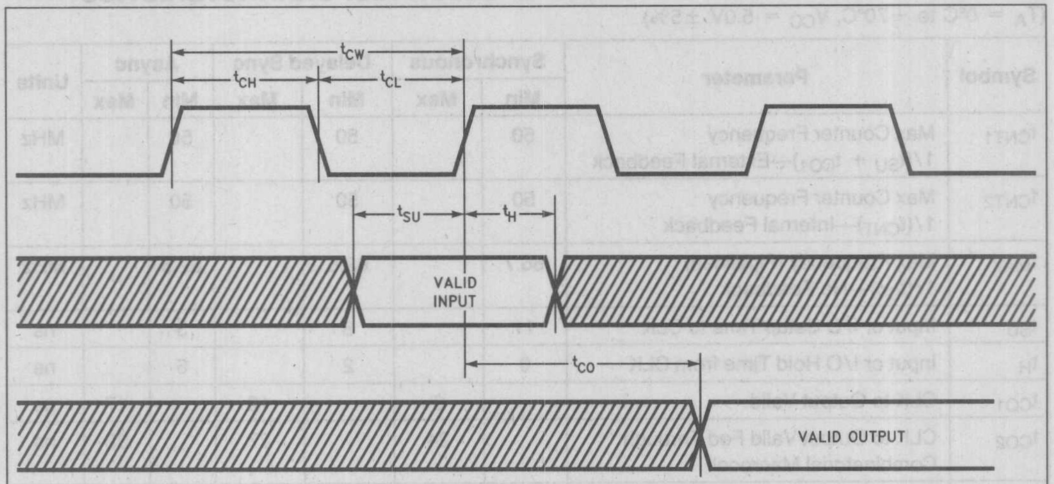
Symbol	Parameter	Synchronous Min	Synchronous Max	Delayed Sync Min	Delayed Sync Max	Async Min	Async Max	Units
f_{CNT1}	Max Counter Frequency 1/(t_{SU} + t_{CO1})—External Feedback	50		50		50		MHz
f_{CNT2}	Max Counter Frequency 1/(t_{CNT})—Internal Feedback	50		50		50		MHz
f_{MAX}	Max Frequency (Pipelined) 1/(t_{CP})—No Feedback	66.7		62.5		62.5		MHz
t_{SU}	Input or I/O Setup Time to CLK	11		8		3		ns
t_H	Input or I/O Hold Time from CLK	0		2		6		ns
t_{CO1}	CLK to Output Valid		9		12		17	ns
t_{CO2}	CLK to Output Valid Fed Through Combinatorial Macrocell		24		27		32	ns
t_{CNT}	Register Output Feedback to Register Input—Internal Path		20		20		20	ns
t_{CL}	CLK Low Time	7		7		7		ns
t_{CH}	CLK High Time	7		7		7		ns
t_{CP}	CLK Period	15		15		15		ns

COMBINATORIAL MODE WAVEFORMS



290459-13

REGISTERED MODE WAVEFORMS

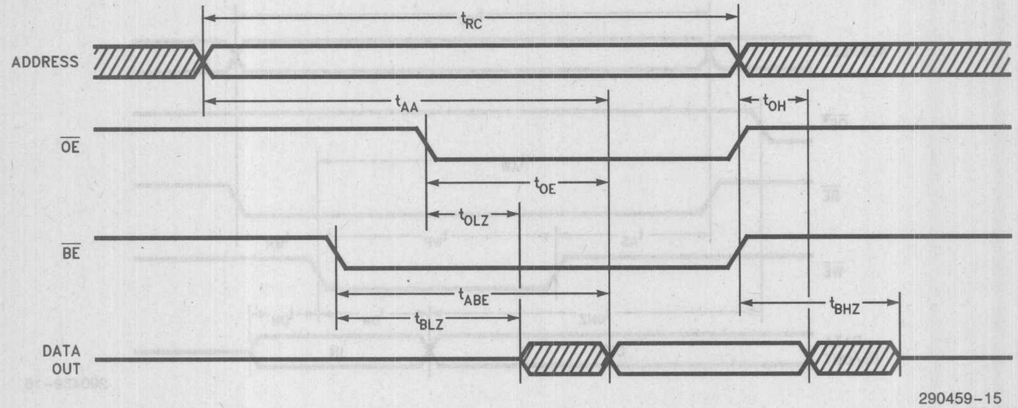


290459–14

SRAM READ—A.C. CHARACTERISTICS (T_A = 0°C to +70°C, V_{CC} = 5.0V ±5%)

Symbol	Parameter	-10		-15		Units
		Min	Max	Min	Max	
t_{RC}	Read Cycle Time	15		20		ns
t_{AA}	Address Access Time		15		20	ns
t_{ABE}	Block Enable Access Time		15		20	ns
$t_{OE}^{(1)}$	Output Enable to Output Valid		12		15	ns
t_{OH}	Output Hold from Address Change	2		3		ns
$t_{BLZ}^{(1)}$	Block Enable to Output in Low Z	3		5		ns
$t_{BHZ}^{(1, 2)}$	Block Disable to Output in High Z		10		15	ns
$t_{OLZ}^{(1)}$	Output Enable to Output in Low Z	3		5		ns

TIMING WAVEFORM OF READ CYCLE



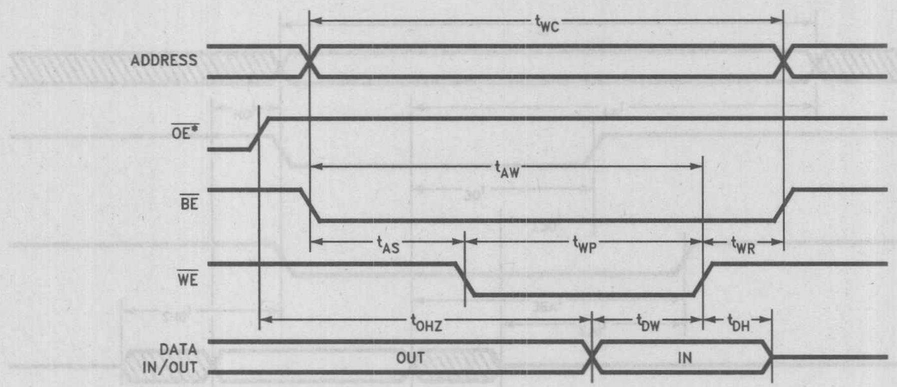
NOTE:
$\overline{WE}$ held at V_{IH}.

SRAM WRITE—A.C. CHARACTERISTICS (T_A = 0°C to +70°C, V_{CC} = 5.0V ±5%)

Symbol	Parameter	-10		-15		Units
		Min	Max	Min	Max	
t_{WC}	Write Cycle Time	15		20		ns
t_{BW}	Block Enable to End of Write	10		13		ns
t_{AW}	Address Valid to End of Write	13		17		ns
t_{AS}	Address Set-up Time	3		4		ns
t_{WP}	Write Pulse Width	10		13		ns
t_{WR}	Write Recovery Time	2		3		ns
t_{DW}	Data Valid to End of Write	10		13		ns
t_{DH}	Data Hold Time	2		3		ns
t_{OHZ}(1, 2, 3)	Output Disable to Valid Data In	10		13		ns

NOTES:
1. These signals are measured at ±0.5V from steady state voltage as driven by specified output load. Z → H and Z → L are measured at 1.5V on output.
2. These signals are measured with C_L = 5 pF.
3. Does not apply for separate data in and data out buses.

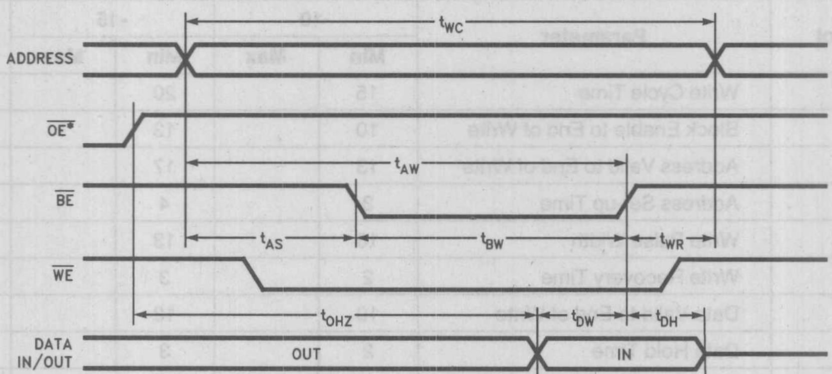
TIMING WAVEFORM OF WRITE CYCLE ($\overline{WE}$ Controlled Timing)



290459-16

NOTE:
Cycle shown is for common data in and data out bus.

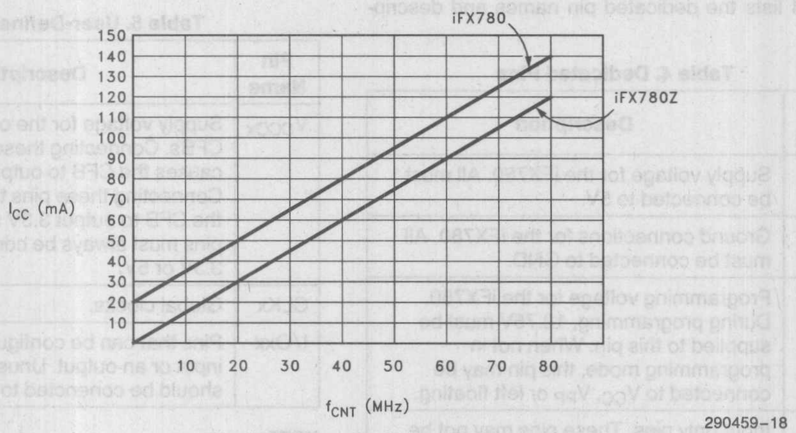
TIMING WAVEFORM OF WRITE CYCLE #2 ($\overline{BE}$ Controlled Timing)



290459-17

NOTE:
Cycle shown is for common data in and data out bus.

I_{CC} vs FREQUENCY



Conditions: $T_A = +25°C$, $V_{CC} = 5V$

NOTE: Four 20-bit counters

POWER-UP RESET

Because V_{CC} rise can vary significantly from one application to another, V_{CC} rise must be monotonic. The power-up cycle is complete within a delay of t_{PR} after V_{CC} reaches the V_{ON} value. During power sequencing, V_{CC} must always be greater than or equal to V_{CCO}.

Internal power-up reset circuits ensure that all flip-flops will be reset to a logic 0 after the device has powered-up. Also, the JTAG TAP controller will be put into the *Test-Logic-Reset* state. The outputs on an unprogrammed device will power-up in a high impedance state.

POWER-UP RESET CHARACTERISTICS

Symbol	Parameter	Value
t_{PR}	Power-Up Reset Time	100 μs Max
V_{ON}	Turn-On Voltage	4.75V Min

PIN DESCRIPTIONS

Table 4 lists the dedicated pin names and descriptions.

Table 4. Dedicated Pins

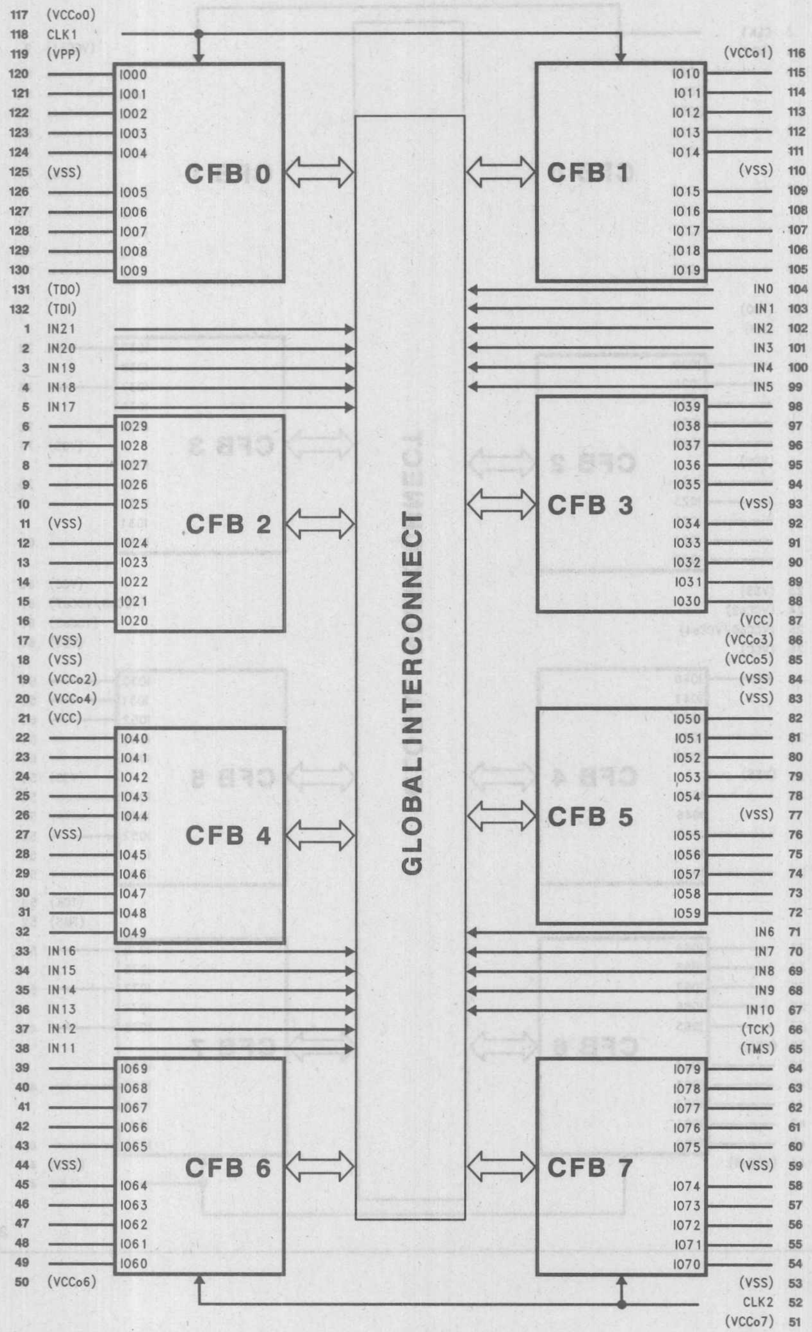
Pin Name	Description
V_{CC}	Supply voltage for the iFX780. All must be connected to 5V.
V_{SS}	Ground connections for the iFX780. All must be connected to GND.
V_{PP}	Programming voltage for the iFX780. During programming, 12.75V must be supplied to this pin. When not in programming mode, this pin may be connected to V_{CC}, V_{PP} or left floating.
INx	Input only pins. These pins may not be available on all packages. Unused inputs should be connected to V_{CC} or GND.
TDI	The Testability Data Input is the boundary scan serial data input to the iFX780. JTAG instructions and data are shifted into the iFX780 on the TDI input pin on the rising edge of TCK. TDI may be left floating if unused.
TDO	The Testability Data Output is the boundary scan serial data output from the iFX780. JTAG instructions and data are shifted out of the iFX780 on the TDO output on the falling edge of TCK. The TDO output driver is supplied through V_{CCO}.
TCK	The Testability Clock input provides the boundary scan clock for the iFX780. TCK is used to clock state information and data into and out of the iFX780 during boundary scan or programming modes. The maximum operating frequency of the boundary scan test clock is 8 MHz. TCK may be left floating if unused.
TMS	The Testability Control input is the boundary scan test mode select for the iFX780. TMS may be left floating if unused.

Table 5 lists the user defined pin names and descriptions.

Table 5. User-Defined Pins

Pin Name	Description
V_{CCOx}	Supply voltage for the outputs of the CFBs. Connecting these pins to +5V causes the CFB to output 5V signals. Connecting these pins to +3.3V causes the CFB to output 3.3V signals. These pins must always be connected to either 3.3V or 5V.
CLKx	Global clocks.
I/Oxx	Pins that can be configured either as an input or an output. Unused I/O pins should be conencted to V_{CC} or GND.

NOTE:
V_{CC}, V_{CCOX} and V_{PP} pins should be decoupled with a 0.1 μF ceramic capacitor at the device pin.


CFB 0
CFB 1
CFB 2
CFB 3
CFB 4
CFB 5
CFB 6
CFB 7
GLOBAL INTERCONNECT
117 (VCCo0)
118 CLK1
119 (VPP)
120 IO00
121 IO01
122 IO02
123 IO03
124 IO04
125 (VSS)
126 IO05
127 IO06
128 IO07
129 IO08
130 IO09
131 (TDO)
132 (TDI)
1 IN21
2 IN20
3 IN19
4 IN18
5 IN17
6 IO29
7 IO28
8 IO27
9 IO26
10 IO25
11 (VSS)
12 IO24
13 IO23
14 IO22
15 IO21
16 IO20
17 (VSS)
18 (VSS)
19 (VCCo2)
20 (VCCo4)
21 (VCC)
22 IO40
23 IO41
24 IO42
25 IO43
26 IO44
27 (VSS)
28 IO45
29 IO46
30 IO47
31 IO48
32 IO49
33 IN16
34 IN15
35 IN14
36 IN13
37 IN12
38 IN11
39 IO69
40 IO68
41 IO67
42 IO66
43 IO65
44 (VSS)
45 IO64
46 IO63
47 IO62
48 IO61
49 IO60
50 (VCCo6)
(VCCo1) 116
IO10 115
IO11 114
IO12 113
IO13 112
IO14 111
(VSS) 110
IO15 109
IO16 108
IO17 107
IO18 106
IO19 105
IN0 104
IN1 103
IN2 102
IN3 101
IN4 100
IN5 99
IO39 98
IO38 97
IO37 96
IO36 95
IO35 94
(VSS) 93
IO34 92
IO33 91
IO32 90
IO31 89
IO30 88
(VCC) 87
(VCCo3) 86
(VCCo5) 85
(VSS) 84
(VSS) 83
IO50 82
IO51 81
IO52 80
IO53 79
IO54 78
(VSS) 77
IO55 76
IO56 75
IO57 74
IO58 73
IO59 72
IN6 71
IN7 70
IN8 69
IN9 68
IN10 67
(TCK) 66
(TMS) 65
IO79 64
IO78 63
IO77 62
IO76 61
IO75 60
(VSS) 59
IO74 58
IO73 57
IO72 56
IO71 55
IO70 54
(VSS) 53
CLK2 52
(VCCo7) 51

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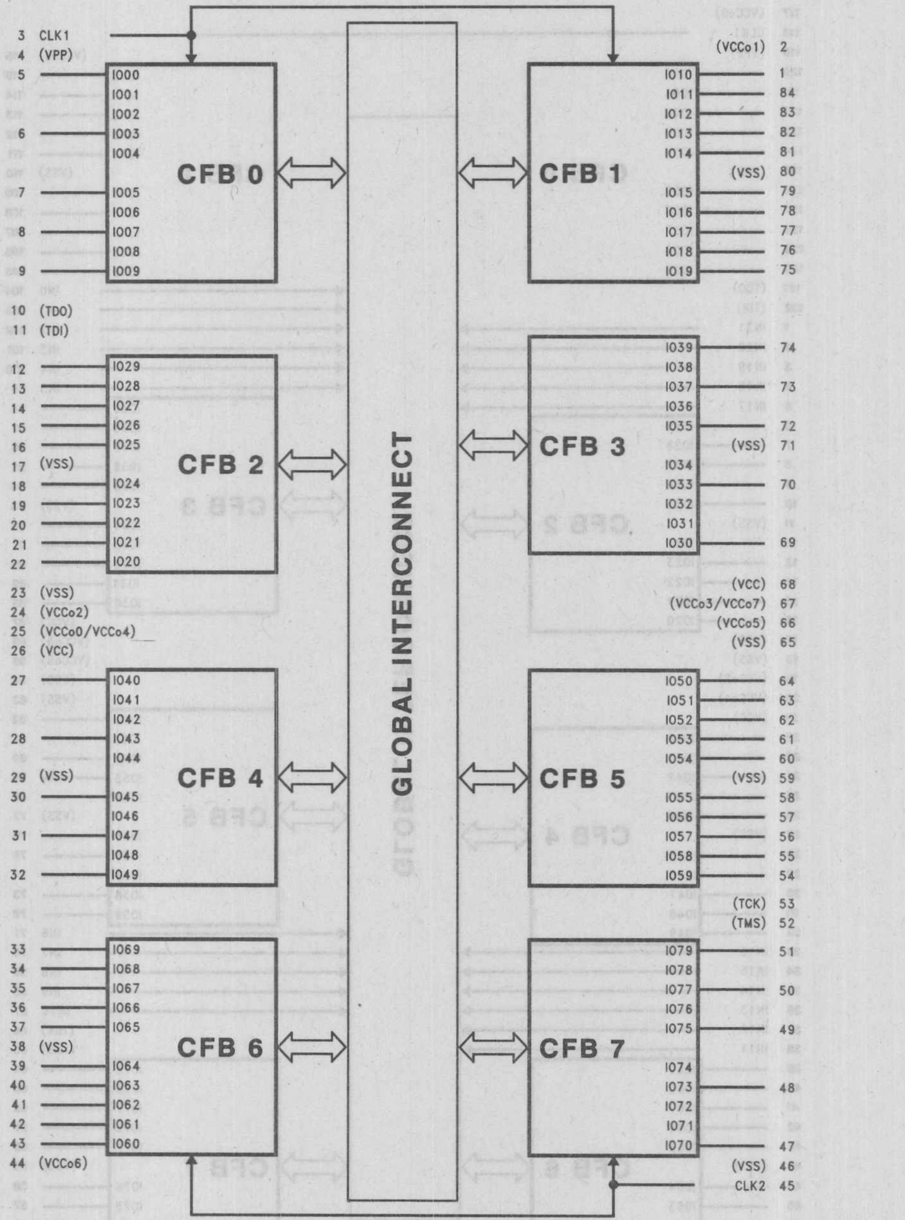
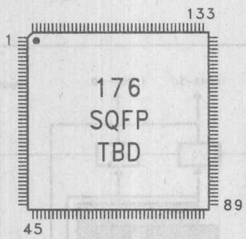

CFB 0
CFB 1
CFB 2
CFB 3
CFB 4
CFB 5
CFB 6
CFB 7
GLOBAL INTERCONNECT
3 CLK1
4 (VPP)
5 IO00
IO01
IO02
6 IO03
IO04
7 IO05
IO06
8 IO07
IO08
9 IO09
10 (TDO)
11 (TDI)
12 IO29
13 IO28
14 IO27
15 IO26
16 IO25
17 (VSS)
18 IO24
19 IO23
20 IO22
21 IO21
22 IO20
23 (VSS)
24 (VCCo2)
25 (VCCo0/VCCo4)
26 (VCC)
27 IO40
IO41
IO42
28 IO43
IO44
29 (VSS)
30 IO45
IO46
31 IO47
IO48
32 IO49
33 IO69
34 IO68
35 IO67
36 IO66
37 IO65
38 (VSS)
39 IO64
40 IO63
41 IO62
42 IO61
43 IO60
44 (VCCo6)
(VCCo1) 2
IO10 1
IO11 84
IO12 83
IO13 82
IO14 81
(VSS) 80
IO15 79
IO16 78
IO17 77
IO18 76
IO19 75
IO39 74
IO38
IO37 73
IO36
IO35 72
(VSS) 71
IO34
IO33 70
IO32
IO31
IO30 69
(VCC) 68
(VCCo3/VCCo7) 67
(VCCo5) 66
(VSS) 65
IO50 64
IO51 63
IO52 62
IO53 61
IO54 60
(VSS) 59
IO55 58
IO56 57
IO57 56
IO58 55
IO59 54
(TCK) 53
(TMS) 52
IO79 51
IO78
IO77 50
IO76
IO75 49
IO74
IO73 48
IO72
IO71
IO70 47
(VSS) 46
CLK2 45

290459-20

iFX8160
10 ns FLEXlogic FPGA WITH SRAM OPTION

- **High Performance FPGA (Field Programmable Gate Array)**
  - **— Deterministic 10 ns Pin-to-Pin Propagation Delays**
  - **— 80 MHz System Clock Frequency**
- **160 Complex Macrocells (7,000 Maximum Logic Gates) or up to 20,480 Bits of SRAM**
- **Any CFB can be either 24V10 Logic or SRAM Block**
  - **— 128 x 10 SRAM Configuration**
  - **— CFB Selectable 3.3V or 5V Outputs**
  - **— Open-Drain Output Option**
- **Supports Partial Reconfigurability and Reprogrammability**
- **JTAG 1149.1 Compatible Test Port**
  - **— Supports Boundary Scan and In-Circuit Reconfiguration and Re-Programming**
- **Supported by Industry Standard Design and Programming Tools**
- **Electrically Erasable 0.6μ ETOX* IV CHMOS FLASH Technology**
  - **— Power Management Options Minimize Active Power Consumption (3 mA/MHz)**
  - **— 1 mA Standby**
- **High Drive I/O**
  - **— PCI Compliant**
- **24V10 Macrocell Features**
  - **— Dual Feedback on All I/O Pins**
  - **— Allocation Supports up to 16 Product Terms per Macrocell with No Performance Penalty**
  - **— 12 Clocking Options**
  - **— Flexible Preset/Clear Options**
  - **— Selectable D/T Flip-Flops**
  - **— Fast 12-Bit Identity Compare Option**
- **Sixteen Configurable Function Blocks (CFBs) Linked by a 100% Connectable Matrix**
  - **— Improves Fitting of Complex Designs**
- **TQFP Thin Package Available**



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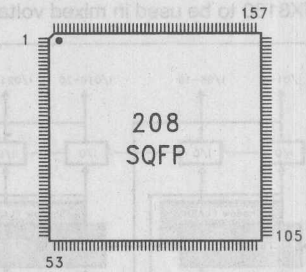

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Package Options

Pins	Package	Macrocells	I/O	Inputs	Clocks	JTAG/V_{PP}	V_{CC}	GND
176	TQFP	160	110	26	4	6	12	18
208	SQFP	160	120	48	4	6	12	18
225	BGA	160	120	54	4	6	17	24

*ETOX is a patented process of Intel Corporation.

October 1993
Order Number: 290461-002

INTRODUCTION

The iFX8160 is the third member of the Intel FLEXlogic FPGA (Field Programmable Gate Array) family. The iFX8160 consists of sixteen configurable function blocks (CFBs) linked by a 100% connectable matrix. Each CFB can be defined either as a 24V10 logic block or as a block of 128 x 10 SRAM. This combination will provide approximately 7,000 gates of logic in either SQFP or BGA packages.

FLEXIBLE PERFORMANCE

The iFX8160 uses Intel's 0.6μ ETOX FLASH technology to provide an 80 MHz external clock frequency with predictable 10 ns pin-to-pin delays. This advanced process technology combined with power management options enables very low active and standby power consumption.

FLEXIBLE FEATURES

The unique combination of features available in the iFX8160 make it ideal for a wide variety of applications. For example, the high performance and flexible clock options provided are designed to support functions such as bus control, custom cache control, and DRAM control for the current and next generation of Intel microprocessors. The very low power consumption and user selectable 5V/3.3V outputs allow the iFX8160 to be used in mixed voltage applications such as portable or embedded systems where CPUs operating at 3.3V still need to communicate to 5V peripherals. The combination of SRAM and logic in a single device becomes a big advantage when designing communication controllers or bus interface controllers where memory is required for buffering data in addition to the logic for the controller design itself.

FLEXIBLE TESTING AND PROGRAMMING

The iFX8160 also provides dedicated JTAG 1149.1 compatible pins to support boundary scan, in-circuit reconfiguration/reprogramming, and programming modes. In-circuit reconfiguration/reprogramming not only allows the designer ultimate flexibility in prototyping new designs but also supports applications where the final configuration is not fixed. New configurations may be downloaded to the iFX8160 upon power-up to reflect changes in system organization or design requirements that cannot be determined at production time. For more information on in-circuit reconfiguration and programming, refer to Application Brief AB-52.

FLEXIBLE TOOLS SUPPORT

The FLEXlogic FPGA family is supported by industry standard design entry/programming environments including Intel's PLDshell Plus software. This software runs on Intel386™ or higher PC-compatible platforms.

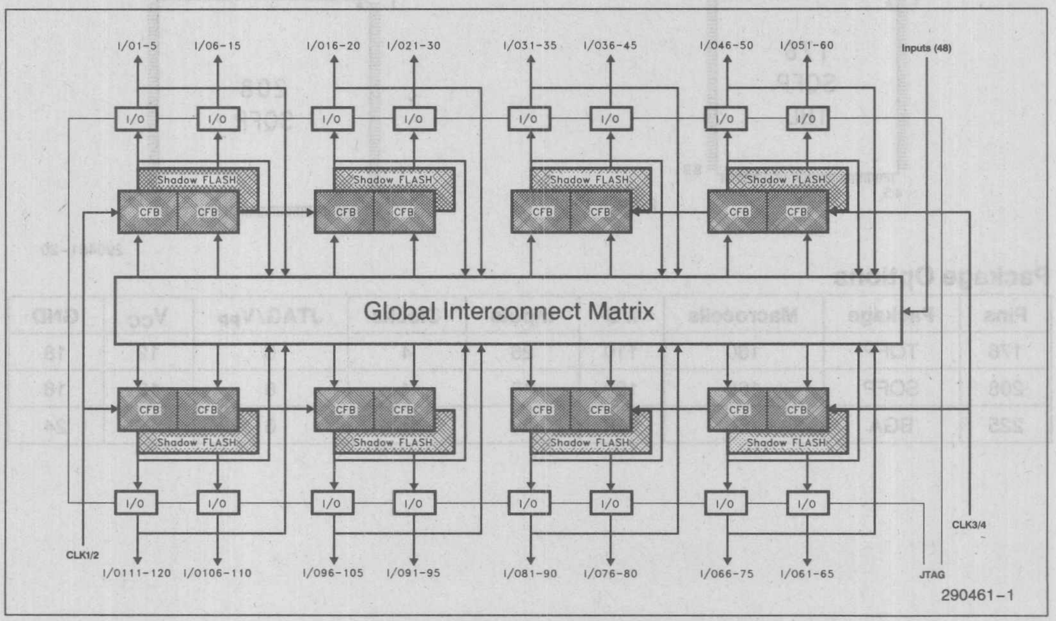


Figure 1. IFX8160 Architecture

INTERCONNECT

The Global Interconnect Matrix that connects each of the CFB blocks is 100% connectable. Any combination of signals in the matrix can be routed into any CFB block, up to the maximum fan-in of the block (24).

This high degree of connectivity between CFB blocks eliminates routing problems during rework of a complex design.

Configurable Function Blocks

24V10 MODE

Each 24V10 block contains a product term array, a P-Term Allocation circuit, 10 macrocells, clocks and I/O logic in the familiar architecture of a simple PLD.

The 24V10 CFB blocks have a generous fan-in to macrocell ratio (2.4:1). This improves the fitting capacity of the iFX8160 architecture by providing more available interconnect lines from the global interconnect matrix for each macrocell.

The 24V10 blocks also provide two asynchronous Clear/Preset control terms and two Output Enable control terms (with an inversion option for each). Within each 24V10 block an identity compare circuit is available that can perform a compare of up to 12 bits within the t_{PD} of the device.

MACROCELL CONFIGURATIONS

Each I/O of the device has dual (internal and pin) feedback paths (see Figure 2). This allows macrocells to be used for buried logic while the I/O pins are used as inputs. Depending on the package used, some macrocell outputs may not be brought outside the package. These I/Os may still be used to provide buried logic since internal feedback is available. The macrocells can be configured either as a fast combinatorial block, a D-register, or a T-register. J/K and S/R registers are available via software emulations.

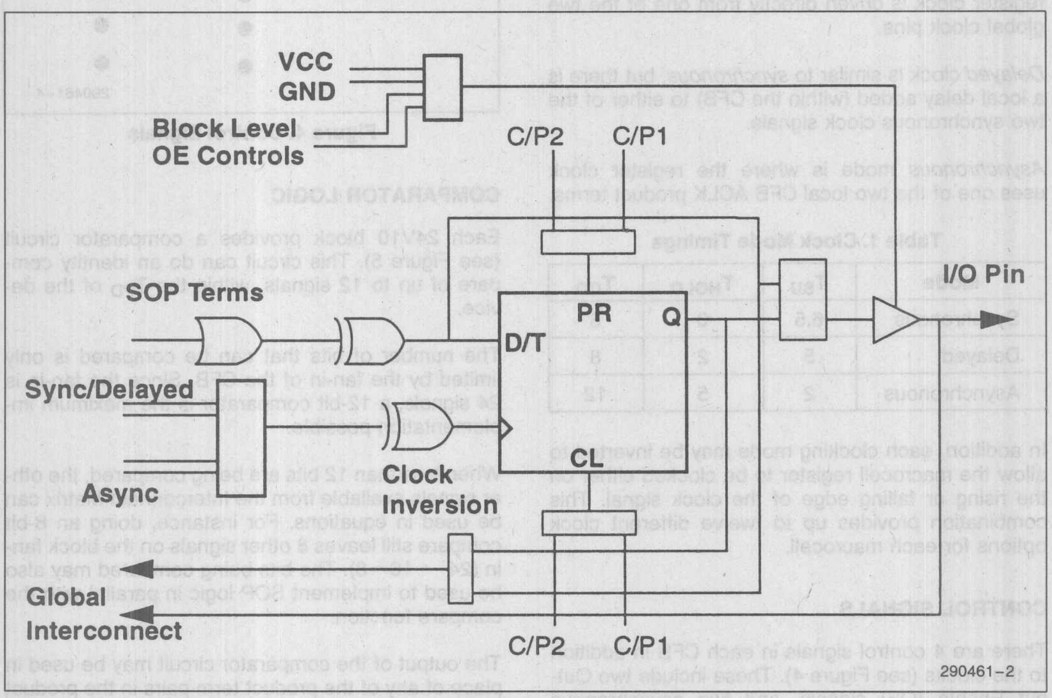


Figure 2. CFB as 24V10 Block

There are three clocking modes available for every macrocell (see Figure 3): *synchronous, delayed, asynchronous.* Table 1 shows the different timing options each clock mode offers.

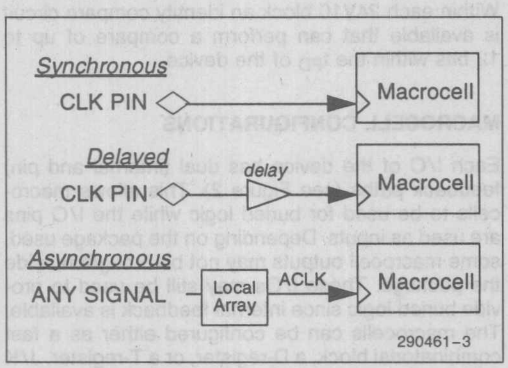


Figure 3. Clocking Modes

Synchronous is the standard clock mode where the register clock is driven directly from one of the two global clock pins.

Delayed clock is similar to *synchronous*, but there is a local delay added (within the CFB) to either of the two synchronous clock signals.

Asynchronous mode is where the register clock uses one of the two local CFB ACLK product terms.

Table 1. Clock Mode Timings

Mode	T_{SU}	T_{HOLD}	T_{CO}
Synchronous	6.5	0	6
Delayed	5	2	8
Asynchronous	2	5	12

In addition, each clocking mode may be inverted to allow the macrocell register to be clocked either on the rising or falling edge of the clock signal. This combination provides up to twelve different clock options for each macrocell.

CONTROL SIGNALS

There are 4 control signals in each CFB in addition to the clocks (see Figure 4). These include two Output Enable (OE) signals, and two asynchronous Clear/Preset signals. Each control signal is generated by a single product term from the local 24V10 AND array with an inversion option. This allows multiple product term control equations to be implemented.

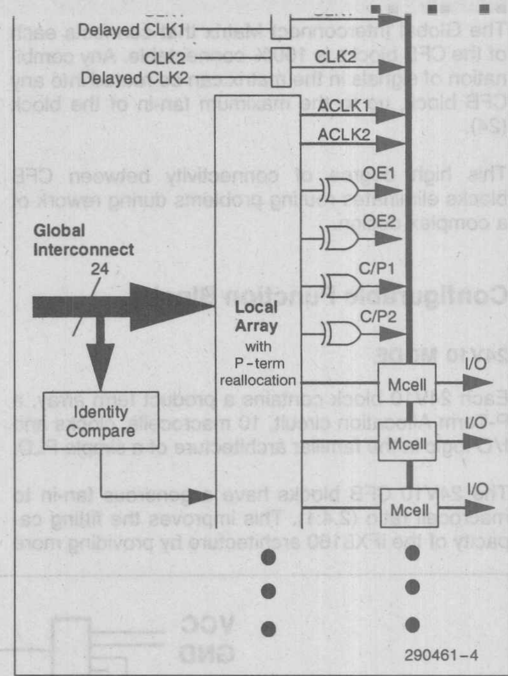


Figure 4. Control Signals

COMPARATOR LOGIC

Each 24V10 block provides a comparator circuit (see Figure 5). This circuit can do an identity compare of up to 12 signals, within the T_{PD} of the device.

The number of bits that can be compared is only limited by the fan-in of the CFB. Since the fan-in is 24 signals, a 12-bit comparator is the maximum implementation possible.

When less than 12 bits are being compared, the other signals available from the Interconnect Matrix can be used in equations. For instance, doing an 8-bit compare still leaves 8 other signals on the block fan-in (24 − 16 = 8). The bits being compared may also be used to implement SOP logic in parallel with the compare function.

The output of the comparator circuit may be used in place of any of the product term pairs in the product term allocation logic allowing the compare result to be used in any macrocell. However, only one of the ten macrocells in the CFB can use the comparator output.

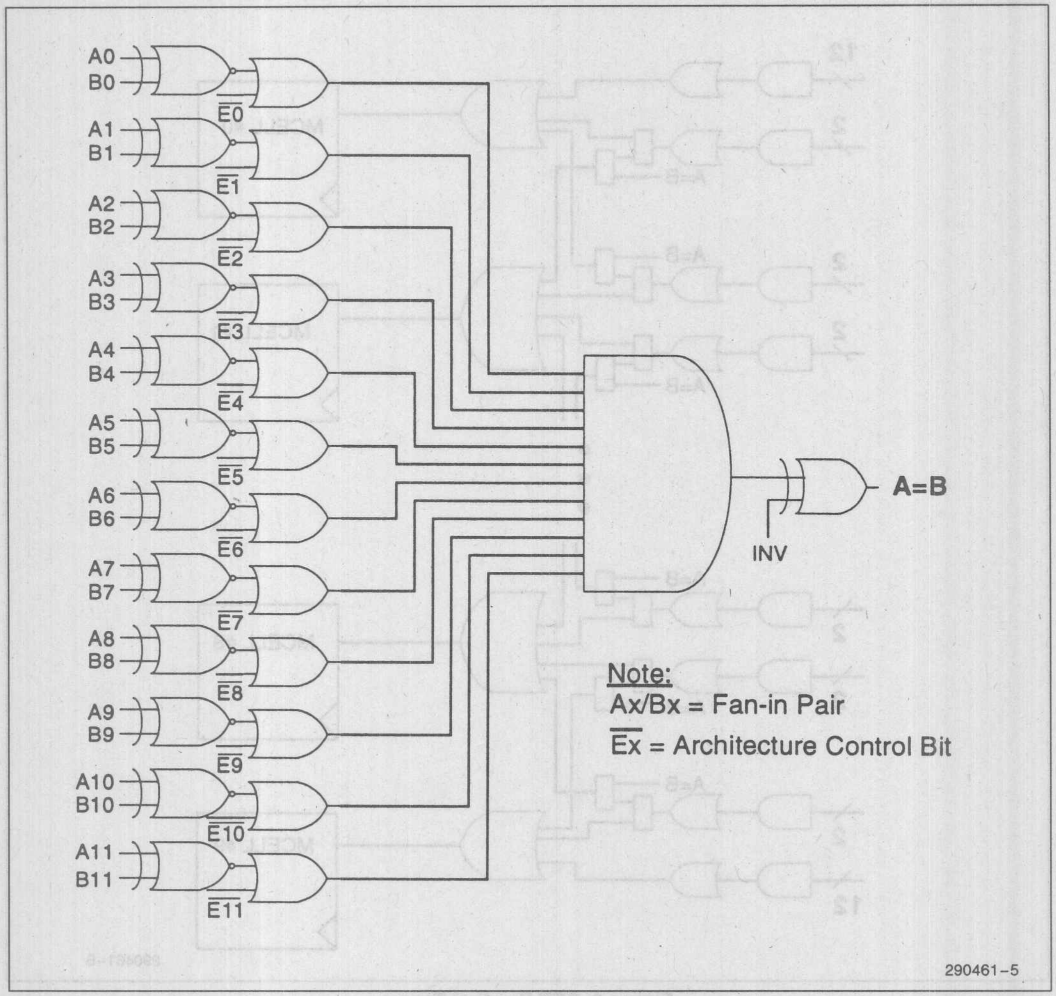


Figure 5. 12-Bit Identity Compare Logic

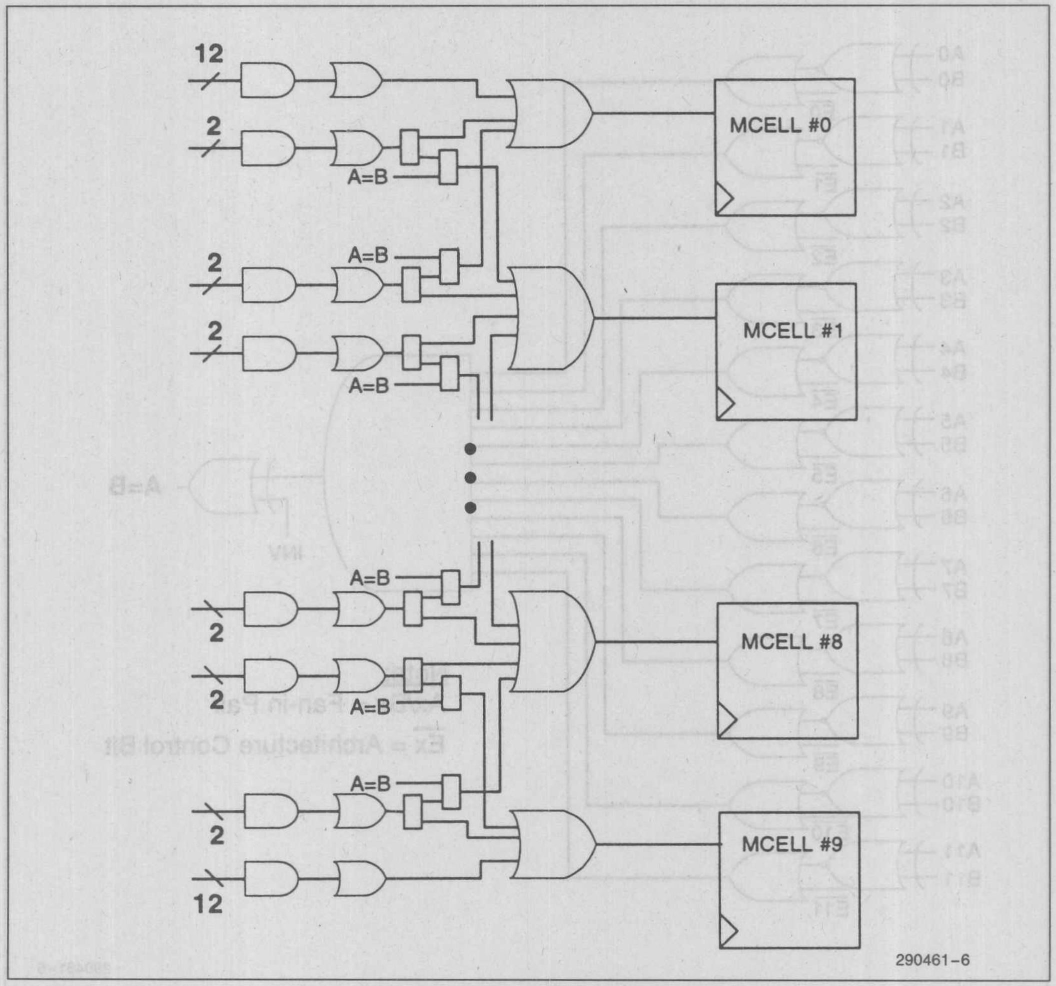


Figure 6. CFB Product Terms

PRODUCT TERM ALLOCATION

The iFX8160 uses the patented Intel product term allocation scheme, which gives better utilization of the P-term resources without the performance penalty of other approaches. The P-terms are typically grouped into sets of two product terms each, and there are two sets per macrocell.

Each macrocell may borrow from adjacent macrocells in order to increase the total number of P-terms to a maximum of 8. In addition, the macrocells located at the "ends" of each CFB have access to additional product terms and can support up to 16 P-term equations (see Figure 6). The performance of any macrocell is the same whether 2 P-terms or 16 P-terms are being used.

SRAM Configuration

Each iFX8160 CFB block can be configured as a 128 x 10 (128 words by 10 bits) SRAM block (see Figures 7 and 8). The SRAM is accessed in a conventional manner by using 7 bits of the 24 signal fan-in as address information and 10 bits as data-in. Three bits are used for $\overline{BE}$ (Block Enable), $\overline{WE}$, and $\overline{OE}$ controls (see Table 2). SRAM control signals on the iFX8160 may be active-high or active low.

Table 2. SRAM Function Table

Inputs			Cycle	I/O Pins
$\overline{BE}$	$\overline{WE}$	$\overline{OE}$		
1	X	X	None	Disabled
0	1	1	Read	Disabled
0	1	0	Read	Enabled
0	0	1	write	Disabled
0	0	0	write	Enabled

It is possible to define the SRAM memory either with a bidirectional I/O data bus or with a separate input data bus and output data bus.

The SRAM memory bits are initialized by the on-chip FLASH cells during power-up. Therefore, the data in the SRAM can be pre-configured at programming time. As long as no memory writes to this block are executed, the SRAM will contain a copy of the nonvolatile cells. In this way, the SRAM block can be used as read only memory (ROM).

When a CFB is configured as a SRAM, regular Sum-of-Product logic is unavailable in that block. All of the macrocells and p-terms have been converted to SRAM use.

Different sized SRAM organizations are possible by cascading multiple CFBs to increase the width or depth of the memory.

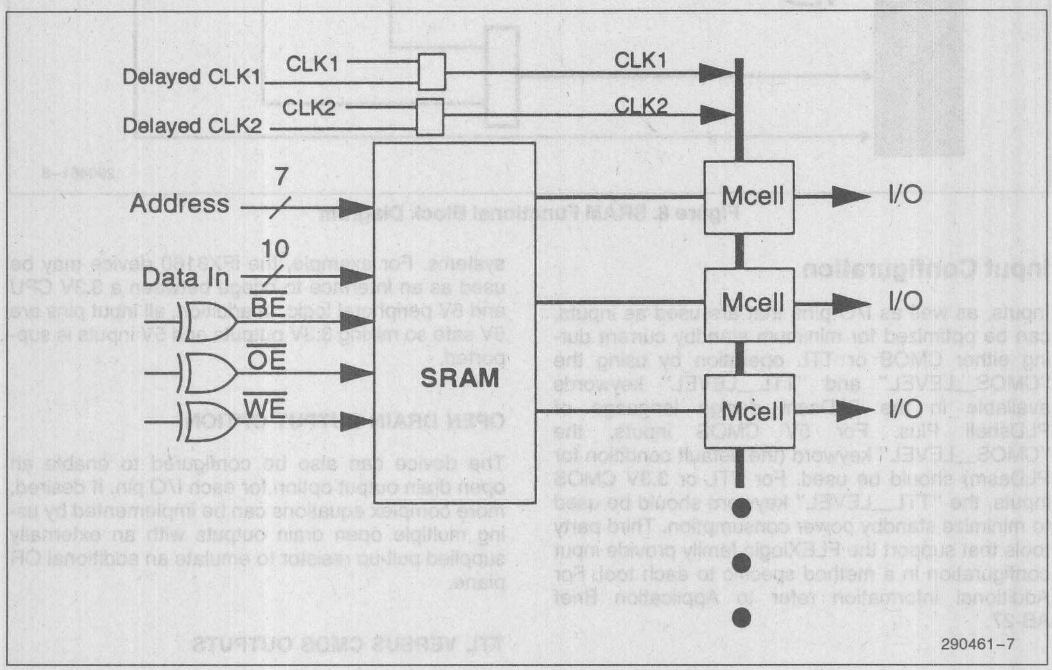


Figure 7. SRAM Overall Block Diagram

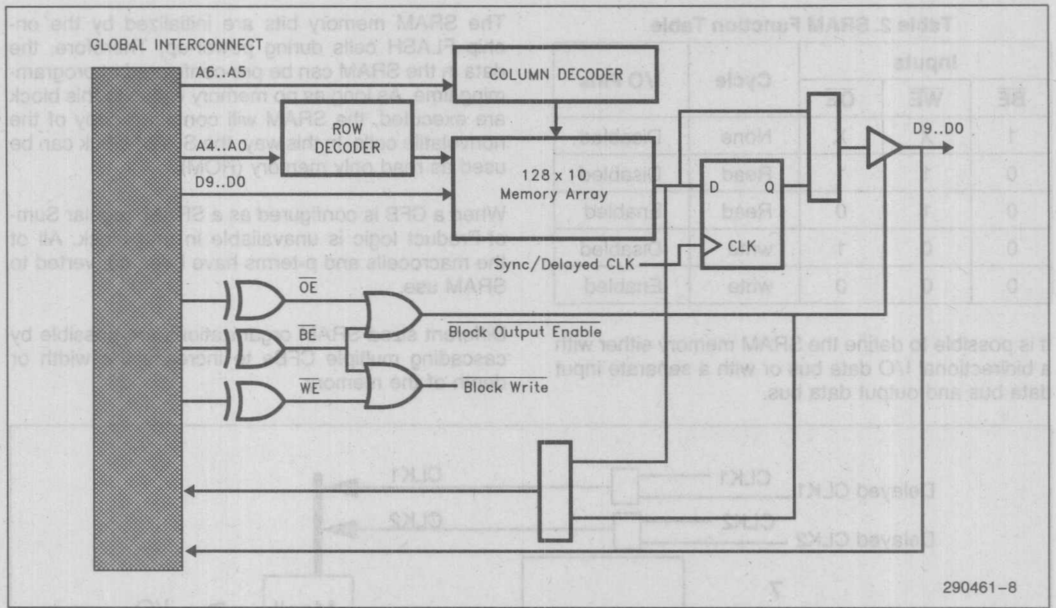


Figure 8. SRAM Functional Block Diagram

Input Configuration

Inputs, as well as I/O pins that are used as inputs, can be optimized for minimum standby current during either CMOS or TTL operation by using the "CMOS_LEVEL" and "TTL_LEVEL" keywords available in the PLDasm design language of PLDshell Plus. For 5V CMOS inputs, the "CMOS_LEVEL" keyword (the default condition for PLDasm) should be used. For TTL or 3.3V CMOS inputs, the "TTL_LEVEL" keyword should be used to minimize standby power consumption. Third party tools that support the FLEXlogic family provide input configuration in a method specific to each tool. For Additional information refer to Application Brief AB-27.

Output Configuration

3.3V SELECTION

The pins in an I/O block can operate at 3.3V by tying the appropriate V_{CCO} pins to a 3.3V power supply. While the iFX8160 still requires 5V V_{CC} for normal operation, the V_{CCO} pin associated with each CFB block may be connected to either 5V or 3.3V to control the output voltages of the I/O pins in that block. This allows the iFX8160 to be used in mixed voltage systems. For example, the iFX8160 device may be used as an interface to bridge between a 3.3V CPU and 5V peripheral logic. In addition, all input pins are 5V safe so mixing 3.3V outputs and 5V inputs is supported.

OPEN DRAIN OUTPUT OPTION

The device can also be configured to enable an open drain output option for each I/O pin. If desired, more complex equations can be implemented by using multiple open drain outputs with an externally supplied pull-up resistor to emulate an additional OR plane.

TTL VERSUS CMOS OUTPUTS

There is a weak pullup provided for CMOS-compatible outputs. This pullup is always active in both 3.3V and 5V modes.

HIGH DRIVE I/O

The iFX8160 output buffers are designed specifically for applications requiring high drive current. This allows the iFX8160 to drive a bus, like PCI, without the need for external buffers.

JTAG/IEEE 1149.1 TESTABILITY

The JTAG/IEEE 1149.1 Standard Boundary Scan architecture is implemented in the iFX8160. This feature supports fault isolation testing of board designs at the component level and enhances production testing, field repair, and is ideal for Fault Tolerant applications.

The iFX8160 boundary scan support consists of an Instruction Register, a Data Register, scan cells, and associated logic which are accessed through the Test Access Port (TAP). The TAP interface consists of three inputs: Test Mode Select (TMS), Test Data In (TDI) and Test Clock (TCK), and one output: Test Data Out (TDO).

The boundary scan cells of the iFX8160 external signals are linked to form a shift register chain for all active pins. This chain provides a path which can be used to shift in test stimulus as well as shift out test response data for inspection.

For example, a continuity test may be performed between two JTAG devices on a circuit board by placing a known value on the output buffers of one device while observing the input buffers of the other device. This same technique may be used to perform simple in-circuit functional testing of the iFX8160 for prototyping new system designs.

The 4-pin JTAG test interface is also used for standard programming, in-circuit reconfiguration, and in-circuit programming.

Boundary Scan Instructions

The iFX8160 boundary scan Instruction Register (IR) supports public instruction opcodes, extended instruction opcodes used for the Program/Verify modes, and additional Intel private instructions.

Public Instructions

EXTEST (IR OPCODE 00000 BINARY)

The EXTEST instruction drives the output pins to the values contained in the boundary scan cells which allows testing of circuitry external to the iFX8160 package, typically for printed circuit board interconnects.

BYPASS (IR OPCODE 11111 BINARY)

The BYPASS instruction selects the one bit ByPass Register, (BPR), to be connected to TDI and TDO.

SAMPLE/PRELOAD (IR OPCODE 00001 BINARY)

The SAMPLE/PRELOAD instruction is used for two functions. The SAMPLE/PRELOAD instruction 1) allows a snap-shot of the values of the pins of the iFX8160 in an unobtrusive manner and 2) preloads data to the iFX8160 pins to be driven to the system circuit board when executing the EXTEST instruction.

IDCODE (IR OPCODE 00010 BINARY)

The IDCODE instruction selects the ID code register to be connected to TDI and TDO allowing the ID-code to be serially shifted out of TDO.

UESCODE (IR OPCODE 10110 BINARY)

The UESCODE instruction selects the User Electronic Signature (UES) register to be connected to TDI and TDO allowing the UES code to be serially shifted out of TDO.

HIZ (IR OPCODE 01000 BINARY)

The HIZ instruction sets all I/Os to a high impedance state.

FERASE (IROPCODE TBD)

The FERASE instruction is used to erase the non-volatile shadow FLASH array beore re-programming.

IN-CIRCUIT RECONFIGURATION AND REPROGRAMMING

The iFX8160 supports in-circuit reconfiguration through the use of the 4-pin JTAG test port. Downloading a new configuration can be accomplished by simply shifting the new data into the device. This may be done as many times as desired in a prototyping scenario.

Once the final version of the design is confirmed it may be programmed into the FLASH cells so that the configuration will not be lost even when the power is turned off. This is also done through the use of the JTAG test port plus the programming voltage pins (V_{PP}).

The iFX8160 FLASH cells are also electrically erasable and may be reprogrammed.

Partial reconfiguration and reprogrammability is also supported in the iFX8160. New configurations may be downloaded to either half of the iFX8160 during operation to reflect changes in system design.

A programmable security bit controls access to the data programmed into the device. Once this security bit is set, the design cannot be read out of the nonvolatile cells or the SRAM. The state of the nonvolatile security bit at power-up determines access and cannot be changed by in-circuit reconfiguration.

SOFTWARE SUPPORT

PLDshell Plus

PLDshell Plus is a sophisticated development tool for Intel programmable logic and is all you need to begin designing with Intel FPGAs. With PLDshell Plus, you can develop, compile, and simulate efficient designs for Intel FPGAs and PLDs.

PLDshell Plus includes several enhancements over earlier versions:

— Design Merge

— SRAM Configuration Support

— Compare Operation Support

— Simulation Support for Intel FPGA

— Vector Notation

— Full Mouse Support

— Device Selector

DESIGN MERGE

PLDshell Plus can merge multiple PDS design files into any Intel PLD, including the Intel iFX8160. The Merge function makes it easy for designers to consolidate multiple PLDs into a single, high-performance FPGA or PLD.

FPGA ARCHITECTURAL FEATURE SUPPORT

PLDshell Plus supports all of the innovative architectural features of the iFX8160 through the implementation of new language syntax such as:

— SRAM configuration

— Compare operation

— Buried macrocells

— Clocking options

— 3.3V and 5V options

FUNCTIONAL SIMULATION

PLDshell Plus allows the designer to simulate the internal function of any Intel FPGA or PLD for rapid design verification.

pabilities:

— Event-driven simulation of combinatorial, registered, and state machine designs

— Ability to set any input, preload any register, and compare any output against an expected value

— Ability to group signals together (form a vector) to simulate a bus

— Generation of test vectors from simulation results for inclusion in the JEDEC file

— Simulation history file with ability to output a subset of signals to a secondary trace file

DEVICE SELECTOR

The designer can develop the logic design first, and then use the PLDshell Plus device selector to pick a list of appropriate devices. After a design is compiled or estimated through PLDshell Plus a report file is generated. Contained in the report file is a listing of suggested devices appropriate for the target design.

SYSTEM REQUIREMENTS

Listed below are the minimum requirements for a system in order to use PLDshell Plus:

— Intel 386 based PC compatible

— 4 MB RAM (minimum)

— VGA monitor/adaptor

— DOS 3.1 (or later)

THIRD-PARTY SUPPORT DESIGN SOFTWARE

Third party tools support is provided by the following vendors:

- Data I/O
  - — ABEL: Design software allowing you to describe and implement logic designs.
- Logical Devices
  - — CUPL: High level, universal design software package.
- Minc
  - — PLDesigner-XL(R): Powerful design tool that can be used for all types of programmable logic with automatic device selection, automatic partitioning and functional simulation.
- OrCAD
  - — PLD Tools and Schematic Design Tool: Software tool environment including schematic entry, test vector generation and multiple forms of input.

— Verification/Simulation Tool: Series of software tools for performing timing-based simulation of designs.

- Viewlogic
  — ViewPLD and Powerview: Integrated schematic capture and simulation environment.

DEVICE MODELS

Simulation models will be provided by the following vendors:

- Logic Modeling Corporation
  — Smart Model: Device model support for behavioral simulation through a variety of simulators.
- Viewlogic

PROGRAMMING SUPPORT

- Products in Motion (916) 363-5591
  — Flexlogic Programmer
- BP Microsystems
  — PLD 1100
- Data I/O
  — Unisite
  — 2900/3900
- Elan
  — Model 6000

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage (V_{CC})(1) .... −2.0V to +7.0V

Programming Supply Voltage (V_{PP})(1) .... −2.0V to +12.6V

DC Input Voltage (V_I)(1, 2) .... −0.5V to V_{CC} + 0.5V

Storage Temperature (T_{stg}) ..... −65°C to +150°C

Ambient Temperature (T_{amb})(3) ... −10°C to +85°C

NOTES:

1. Voltages with respect to ground.
2. Minimum DC input is −0.5V. During transitions, the inputs may undershoot to −2.0V or overshoot to +7.0V for periods less than 20 ns under no load conditions.
3. Under bias. Extended temperature versions are also available.

NOTICE: This data sheet contains information on products in the sampling and initial production phases of development. The specifications are subject to change without notice. Verify with your local Intel Sales office that you have the latest data sheet before finalizing a design.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

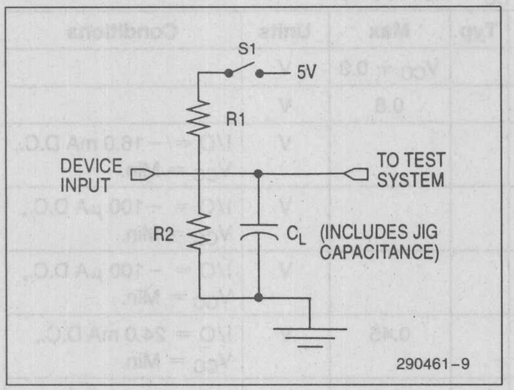
RECOMMENDED OPERATING CONDITIONS

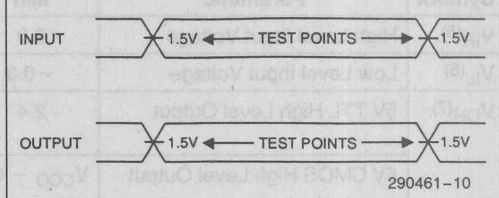
Symbol	Parameter	Min	Max	Units
V_{CC}/V_{CCO}	Supply Voltage—5.0V	4.75	5.25	V
V_{CCO}	Output Supply Voltage—3.3V	3.0	3.6	V
V_{IN}	Input Voltage	0	V_{CC}	V
V_O	Output Voltage	0	V_{CCO}	V
T_A	Operating Temperature	0	+70	°C
t_R	Input Rise Time		500	ns
t_F	Input Fall Time		500	ns

DC CHARACTERISTICS ($T_A = 0°C$ to $+70°C$, $V_{CC} = 5.0V \pm 5\%$)(4)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{IH}(5)	High Level Input Voltage	2.0		$V_{CC} + 0.3$	V	
V_{IL}(5)	Low Level Input Voltage	−0.3		0.8	V	
V_{OH}(7)	5V TTL High Level Output	2.4			V	I/O = −16.0 mA D.C., V_{CC} = Min.
	5V CMOS High Level Output	$V_{CCO} - 0.2$			V	I/O = −100 µA D.C., V_{CC} = Min.
	3V High Level Output Voltage	$V_{CCO} - 0.2$			V	I/O = −100 µA D.C., V_{CC} = Min.
V_{OL}(7)	5V Low Level Output Voltage			0.45	V	I/O = 24.0 mA D.C., V_{CC} = Min.
	3V Low Level Output Voltage			0.2	V	I/O = 12 mA D.C., V_{CC} = Min.
I_I(8)	Input Leakage Voltage			±10	µA	V_{CC} = Max., V_{IN} = GND or V_{CC}
I_{OZ}	Output Leakage Current			±50	µA	V_{CC} = Max., V_{OUT} = GND or V_{CC}
I_{SC}(6)	Output Short Circuit Current	−30		−120	mA	V_{CC} = Max., V_{OUT} = 0.5V
I_{SB}	Standby Power Supply Current		1		mA	V_{IN} = V_{CC} or GND, Outputs Open
I_{CC} Active	Power Supply Current		3		mA per MHz	V_{IN} = V_{CC} or GND, Outputs Open, Device Programmed as Eight 20-Bit Counters

NOTES:
4. Typical values are at T_A = 25°C, V_{CC} = 5V.
5. Absolute values with respect to device GND; all over and undershoots due to system and tester noise are included. Do not attempt to test these values without suitable equipment.
6. Not more than 1 output should be tested at a time. Duration of that test should not exceed 1 second.
7. When driving an I/O pin under JTAG boundary scan, I_{OH} = −4.0 mA and I_{OL} = 12 mA.
8. Input Leakage current on JTAG pins: ±20 µA





NOTE:
Inputs are driven at 3.0V for a LOGIC "1" and 0V for a Logic "0". Timing measurements are made at 1.5V. Outputs are measured at 1.5V. Device input rise and fall times < 3 ns.

SWITCHING TEST CIRCUIT

Specification	S1	C_L	Commercial		Measured Output Value
			R1	R2	
t_{PD}	Closed	35 pF	330Ω	200Ω	1.5V
t_{PZX}	Z → H: Open Z → L: Closed				1.5V
t_{PXZ}	H → Z: Open L → Z: Closed	5 pF			H → Z: V_{OH} − 0.5V L → Z: V_{OL} + 0.5V

PIN CAPACITANCE (T_A = 0°C to +70°C, V_{CC} = 5.0V ±5%)(7)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
C_{IN}	Input Capacitance	V_{IN} = 2V, f = 1.0 MHz				pF
C_{IO}	I/O Capacitance	V_{OUT} = 2V, f = 1.0 MHz				pF
C_{CLK}	Clock Pin Capacitance	V_{OUT} = 2V, f = 1.0 MHz				pF
C_{VPP}	V_{PP} Pin Capacitance	f = 1.0 MHz				pF

NOTE:
7. These values are evaluated at initial characterization and whenever design modifications occur that may affect capacitance.

COMBINATORIAL MODE AC CHARACTERISTICS (T_A = 0°C to +70°C, V_{CC} = 5.0V ±5%)

Symbol	Parameter	iFX8160-10			iFX8160-12			Units
		Min	Typ	Max	Min	Typ	Max	
t_{PD}	Input or I/O to Output Valid			10			10	ns
t_{PZX}(8)	Input or I/O to Output Enable			12			14	ns
t_{PXZ}(8)	Input or I/O to Output Disable			12			14	ns
t_{CLR}	Input or I/O to Asynchronous Clear/Preset			15			18	ns
t_{COMP}	Comparator Input or I/O Feedback to Output Valid			10			12	ns

REGISTER MODE—iFX8160-10 CLOCK AC CHARACTERISTICS

(T_A = 0°C to +70°C, V_{CC} = 5.0V ±5%)

Symbol	Parameter	Synchronous		Delayed Synchronous		Async		Units
		Min	Max	Min	Max	Min	Max	
f_{CNT1}	Max. Counter Frequency $1/(t_{SU} + t_{CO1})$—External Feedback	80		76.9		71.4		MHz
f_{CNT2}	Max. Counter Frequency $1/(t_{CNT})$—Internal Feedback	80		76.9		71.4		MHz
f_{MAX}	Max. Frequency (Pipelined) $1/(t_{CP})$—No Feedback	100		92.9		80		MHz
t_{SU}	Input or I/O Setup Time to CLK	6.5		5		2		ns
t_H	Input or I/O Hold Time from CLK	0		2		5		ns
t_{CO1}	CLK to Output Valid		6		8		12	ns
t_{CO2}	CLK to Output Valid Fed through Combinatorial Macrocell		16		18		22	ns
t_{CNT}	Register Output Feedback to Register Input—Internal Path		12.5		13		14	ns
t_{CL}	CLK Low Time	4.5		4.5		5		ns
t_{CH}	CLK High Time	4.5		4.5		5		ns
t_{CP}	CLK Period	10		10.5		12.5		ns

NOTE:

8. t_{PZX} and t_{PXZ} are measured at ±0.5V from steady state voltage as driven by specified output load. t_{PXZ} is measure with C_L = 5 pF. Z → H and Z → L are measured at 1.5V on output.

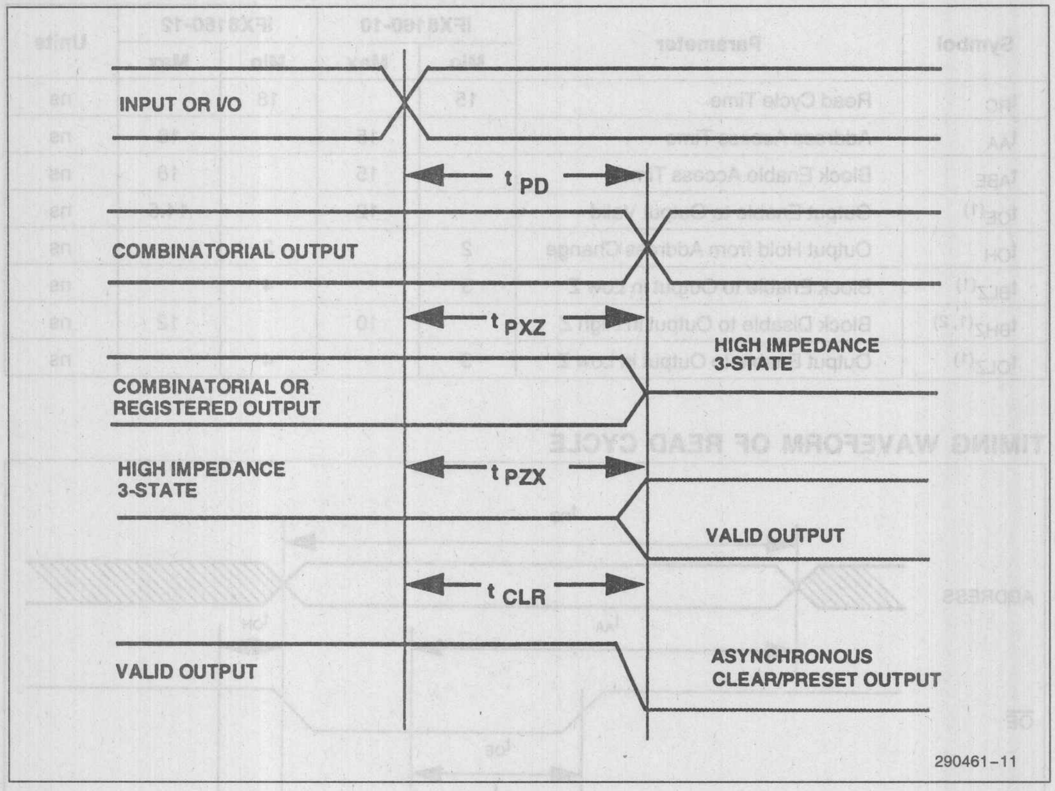
2

REGISTER MODE—iFX8160-12 CLOCK AC CHARACTERISTICS

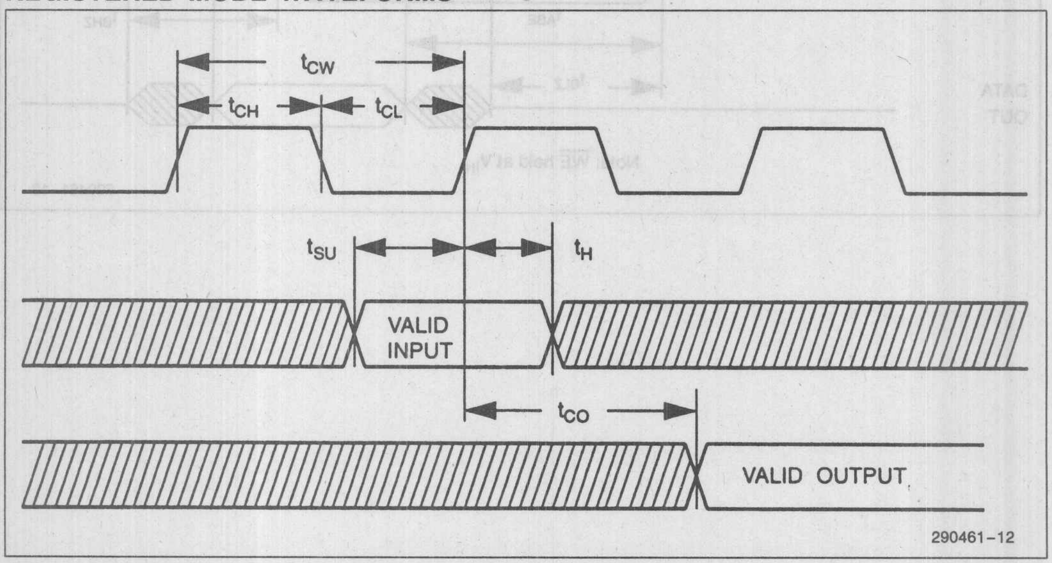
(T_A = 0°C to +70°C, V_{CC} = 5.0V ±5%)

Symbol	Parameter	Synchronous		Delayed Synchronous		Async		Units
		Min	Max	Min	Max	Min	Max	
f_{CNT1}	Max. Counter Frequency $1/(t_{SU} + t_{CO1})$—External Feedback	64.5		64.5		58.8		MHz
f_{CNT2}	Max. Counter Frequency $1/(t_{CNT})$—Internal Feedback	64.5		64.5		58.8		MHz
f_{MAX}	Max. Frequency (Pipelined) $1/(t_{CP})$—No Feedback	83.3		80		66.7		MHz
t_{SU}	Input or I/O Setup Time to CLK	8		6		2.5		ns
t_H	Input or I/O Hold Time from CLK	0		2		6		ns
t_{CO1}	CLK to Output Valid		7.5		9.5		14.5	ns
t_{CO2}	CLK to Output Valid Fed through Combinatorial Macrocell		19.5		21.5		26.5	ns
t_{CNT}	Register Output Feedback to Register Input—Internal Path		15.5		15.5		17	ns
t_{CL}	CLK Low Time	5.5		5.5		5.5		ns
t_{CH}	CLK High Time	5.5		5.5		5.5		ns
t_{CP}	CLK Period	12		12.5		15		ns

COMBINATORIAL MODE WAVEFORMS



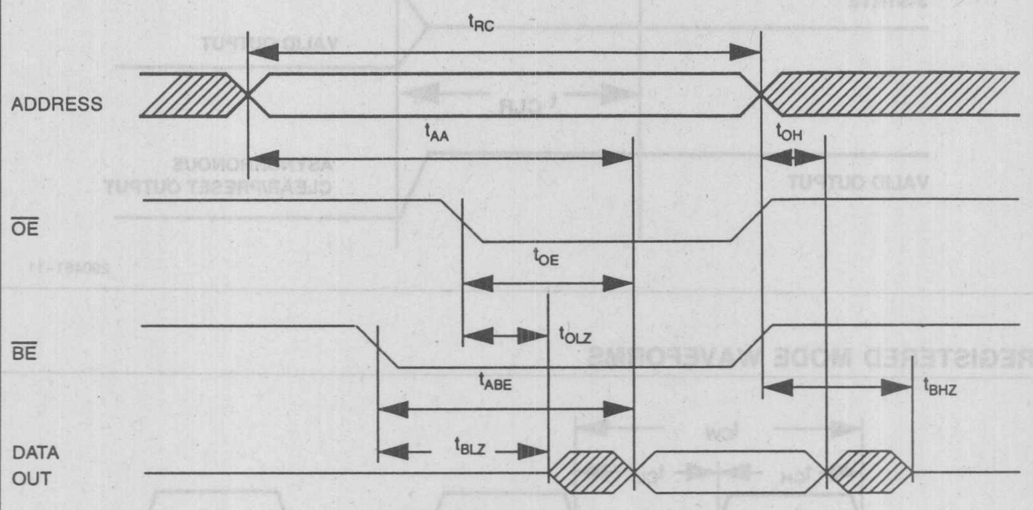
REGISTERED MODE WAVEFORMS



SRAM READ—AC CHARACTERISTICS (T_A = 0°C to +70°C, V_{CC} = 5.0V ±10%)

Symbol	Parameter	iFX8160-10		iFX8160-12		Units
		Min	Max	Min	Max	
t_{RC}	Read Cycle Time	15		18		ns
t_{AA}	Address Access Time		15		18	ns
t_{ABE}	Block Enable Access Time		15		18	ns
t_{OE}(1)	Output Enable to Output Valid		12		14.5	ns
t_{OH}	Output Hold from Address Change	2		3		ns
t_{BLZ}(1)	Block Enable to Output in Low Z	3		4		ns
t_{BHZ}(1, 2)	Block Disable to Output in High Z		10		12	ns
t_{OLZ}(1)	Output Enable to Output in Low Z	3		4		ns

TIMING WAVEFORM OF READ CYCLE



Note: $\overline{WE}$ held at V_{IH}

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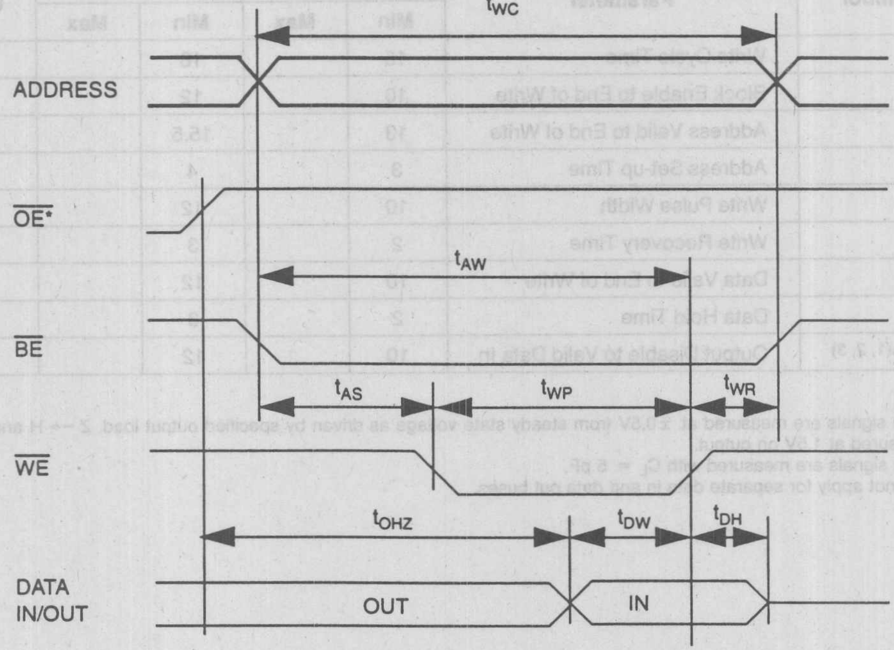
SRAM WRITE—AC CHARACTERISTICS ($T_A = 0°C$ to $+70°C$, $V_{CC} = 5.0V \pm 5\%$)

Symbol	Parameter	iFX8160-10		iFX8160-12		Units
		Min	Max	Min	Max	
t_{WC}	Write Cycle Time	15		18		ns
t_{BW}	Block Enable to End of Write	10		12		ns
t_{AW}	Address Valid to End of Write	13		15.5		ns
t_{AS}	Address Set-up Time	3		4		ns
t_{WP}	Write Pulse Width	10		12		ns
t_{WR}	Write Recovery Time	2		3		ns
t_{DW}	Data Valid to End of Write	10		12		ns
t_{DH}	Data Hold Time	2		3		ns
t_{OHZ}(1, 2, 3)	Output Disable to Valid Data In	10		12		ns

NOTES:
1. These signals are measured at ±0.5V from steady state voltage as driven by specified output load. Z → H and Z → L are measured at 1.5V on output.
2. These signals are measured with $C_L = 5$ pF.
3. Does not apply for separate data in and data out buses.

TIMING WAVEFORM OF WRITE CYCLE #1 ($\overline{\text{WE}}$ Controlled Timing)



*Note: Cycle shown is for common data in and data out bus.

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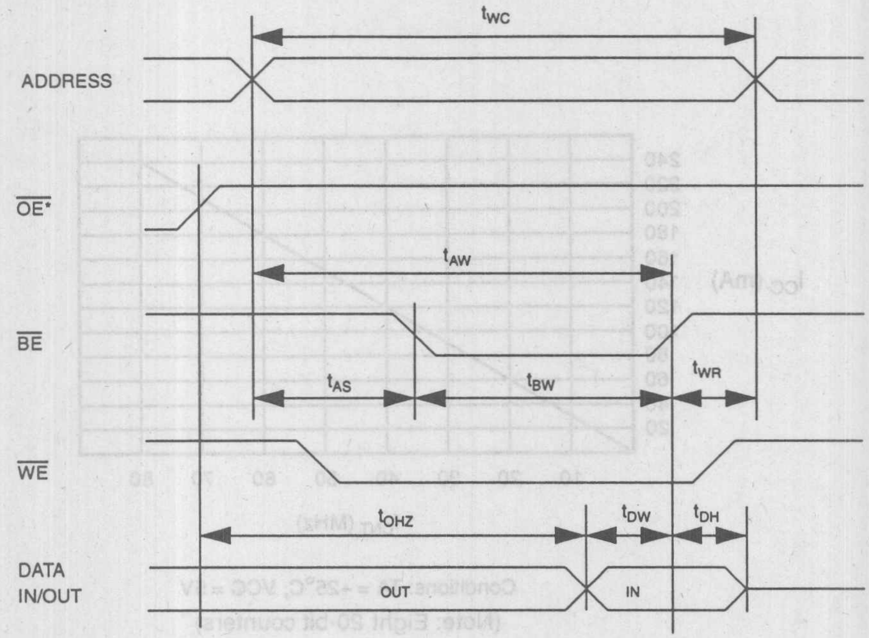
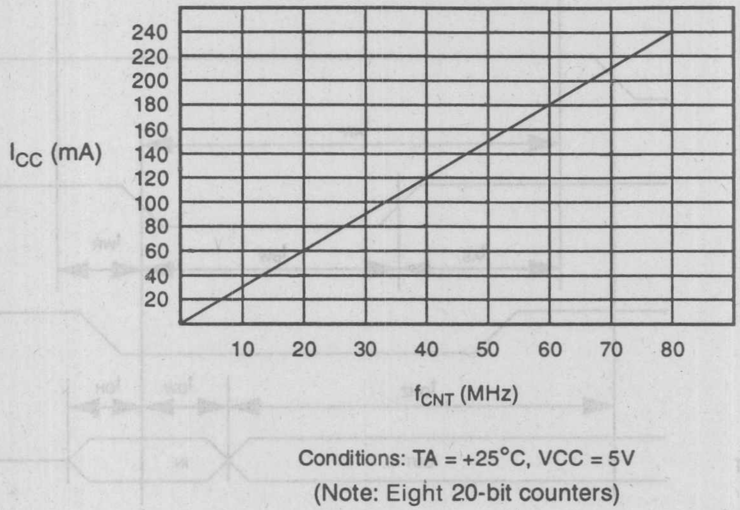


*Note: Cycle shown is for common data in and data out bus.

290461–15



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POWER-UP RESET

Because V_{CC} rise can vary significantly from one application to another, V_{CC} rise must be monotonic. The power-up cycle is complete within a delay of t_{PR} after V_{CC} reaches the V_{ON} value.

Internal power-up reset circuits ensure that all flip-flops will be reset to a logic 0 after the device has powered-up. Also, the JTAG TAP controller will be put into the *Test-Logic-Reset* state. The outputs on an unprogrammed device will power-up in a high impedance state.

POWER-UP RESET CHARACTERISTICS

Symbol	Parameter	Value
t_{PR}	Power-Up Reset Time	100 μs Max
V_{ON}	Turn-On Voltage	4.75V Min

PIN DESCRIPTIONS

Table 4 lists the dedicated pin names and descriptions.

Table 4. Dedicated Pins

Pin Name	Description
V_{CC}(1)	Supply voltage for the iFX8160. All must be connected to 5V.
V_{SS}	Ground connections for the iFX8160. All must be connected to GND.
V_{PP}(1)	Programming voltage for the iFX8160. During programming, 12V must be supplied to this pin. When not in programming mode, this pin may be connected to V_{CC}, V_{PP} or left floating (not GND).
INx	Input only pins. These pins may not be available on all packages. Unused inputs should be connected to V_{CC} or GND.
TDI	The Testability Data Input is the boundary scan serial data input to the iFX8160. JTAG instructions and data are shifted into the iFX8160 on the TDI input pin on the rising edge of TCK. TDI may be left floating if unused.
TDO	The Testability Data Output is the boundary scan serial data output from the iFX8160. JTAG instructions and data are shifted out of the iFX8160 on the TDO output on the falling edge of TCK.
TCK	The Testability Clock input provides the boundary scan clock for the iFX8160. TCK is used to clock state information and data into and out of the iFX8160 during boundary scan or programming modes. The maximum operating frequency of the boundary scan test clock is 8 MHz. TCK may be left floating if unused.
TMS	The Testability Control input is the boundary scan test mode select for the iFX8160. TMS may be left floating if unused.

Table 5 lists the user-defined pin names and descriptions.

Table 5. User-Defined Pins

Pin Name	Description
V_{CC0x}(1)	Supply voltage for the outputs of the CFBs. Connecting these pins to +5V causes the CFB to output 5V signals. Connecting these pins to +3.3V causes the CFB to output 3.3V signals. These pins must always be connected to the desired output drive voltage.
CLKx	Global clocks.
I/Oxx	Pins that can be configured eithor as an input or an output. Unused I/O pins should be connected to V_{CC} or GND.

NOTES:
1. Proper power decoupling is required on all power pins. A 0.01 μF decoupling capacitor is recommended between the power pin and ground.

FPGA Tutorial

Electronic design has been a process of defining and implementing "black boxes". System level parameters are defined, and the system black box is broken into subsystem black boxes, which are subdivided again and again until the component level is reached. FPGAs were developed to function as large, highly-integrated black boxes to implement diverse logic functions, and the FLEXlogic FPGA family gives a designer the ultimate, flexible black box.

FLEXlogic FPGAs were designed to meet increasingly stringent design requirements. The first members of the FLEXlogic family can operate at 80 MHz system frequencies with predictable 10 ns pin-to-pin logic delays. FLEXlogic FPGAs are designed with Configurable Function Blocks (CFB) that can function as 24V10-like logic or SRAM. The CFBs are interconnected with Intel's high-speed Global Interconnect Matrix that allows PLD-like performance in a high density device. Besides traditional sum-of-products and register logic functions, FLEXlogic CFBs can also perform fast identity compares or be configured as a block of 128 x 10 SRAM.

You can start developing with FLEXlogic now using Intel's free PLDshell Plus development tool. This tutorial will show you how to create a simple design using PLDshell Plus. You can also create FLEXlogic designs using the development tools that you now use; FLEXlogic FPGAs are supported on most third-party development tool systems.

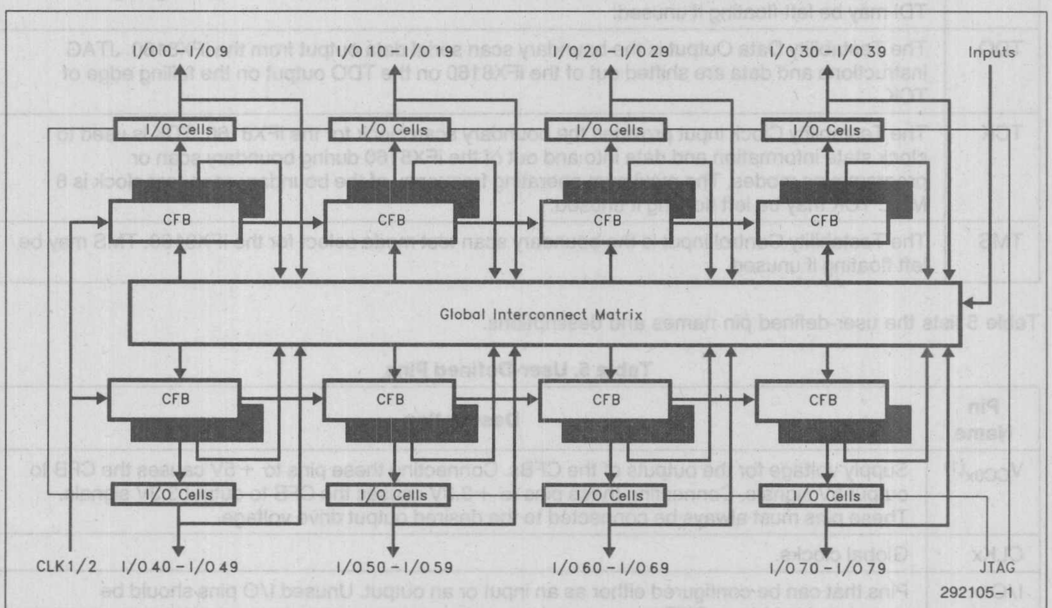

Figure 1. iFX780 Block Diagram

September 1993
Order Number: 292105-002

Designing with FLEXlogic

FLEXlogic FPGAs are as easy to design with as the earliest PLDs; simply write the logical equations, develop a truth table, or enter the schematic equivalent.

$$\begin{aligned} out1 &= in1 * in3 \\ &+ in4 * in5 * in6 * in7 * in8 * in9 * in10 \end{aligned}$$

Up to 16 product terms can be included in a single sum-of-products equation. Most functions require three or fewer product terms, but some functions require many more product terms to implement. Giving each macrocell enough resources to implement all functions is wasteful and expensive, but macrocells must also be able to implement large, complex functions. FLEXlogic uses an innovative product-term allocation scheme to maximize resource utilization and design fit. Pairs of product terms are steered from one macrocell to its neighbor, allowing macrocells to implement functions with up to 16 product terms.

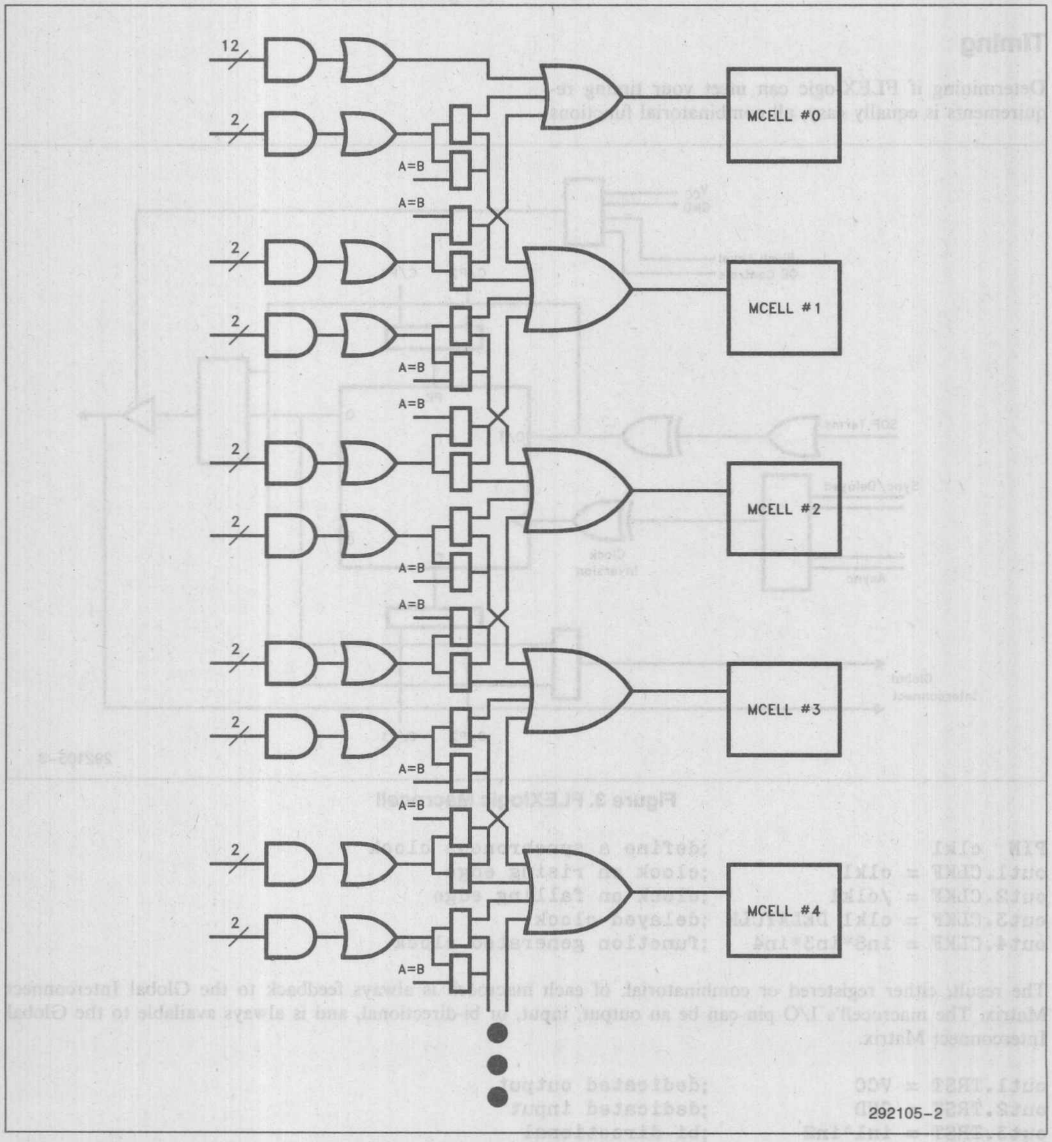

Figure 2. Product Term Allocation

Identity Compare

Identity compares can be defined in parallel with other logic functions:

out2.CMP = [C[0:11]] = = [D]0:11]]

The comparator uses the same inputs as other CFB logic, and works in parallel, so that compares can be included in logic equations, and still deliver the result in 10 ns.

Timing

Determining if FLEXlogic can meet your timing requirements is equally easy; all combinatorial functions requiring one pass through a Configurable Function Block take 10 ns. This includes 16 product-term equations and 12-bit identity compares.

Function results can be loaded into macrocell registers. Each register can be individually configured as a D or T register. SR and JK registers can also be emulated. Register clocking is user programmable in each macrocell, accommodating a variety of timing requirements. Registers can be clocked on the rising or falling edge of an external clock, a delayed external clock, or a function generated clock.

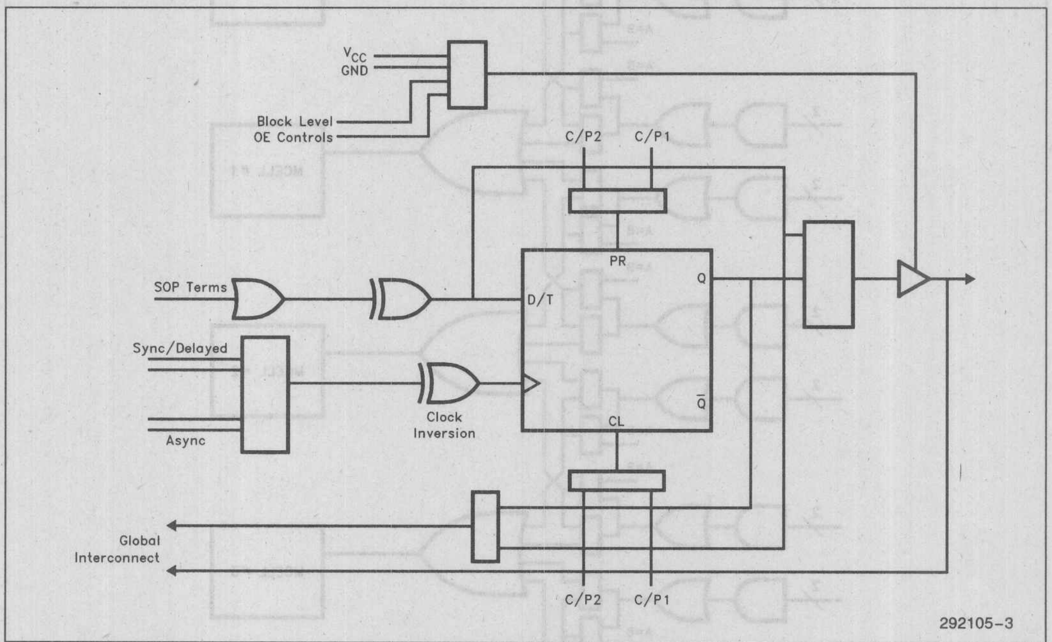

Figure 3. FLEXlogic Macrocell

```
PIN  clkl                   ;define a synchronous clock
outl.CLKF = clkl            ;clock on rising edge
out2.CLKF = /clkl           ;clock on falling edge
out3.CLKF = clkl DELAYCLK   ;delayed clock
out4.CLKF = in8*in3*in4     ;function generated clock
```

The result, either registered or combinatorial, of each macrocell is always feedback to the Global Interconnect Matrix. The macrocell's I/O pin can be an output, input, or bi-directional, and is always available to the Global Interconnect Matrix.

```
outl.TRST = VCC             ;dedicated output
out2.TRST = GND             ;dedicated input
out3.TRST = inl*in2         ;bi-directional
```

CFB as SRAM

Each CFB can be independently configured as 15 ns SRAM.

```
PIN BUFFRAM[0:9]        RAM

BUFFRAM[0:6].ADDR = A0, A1, A2, A3, A4, A5, A6
BUFFRAM[0:9].DATA = DIN[0:9]
BUFFRAM.BE = in8
BUFFRAM.WE = write_enable
```

3.3V/5V I/O

The physical limitations of silicon demand that high-performance electrical designs move to 3.3V or lower voltages. FLEXlogic FPGAs are the first programmable logic devices to address designers' needs for 3.3V and 5V logic. Each CFB can be configured as 3.3V or 5V logic by tying its V_{CC0} pin to the appropriate supply voltage. Adding 3VOLT or 5VOLT to a macrocell's pin definition allows the compiler to group it with other cells with the same logic level.

```
PIN 12 OUT1 3VOLT   ;3.3V pin
```

CFB as SRAM

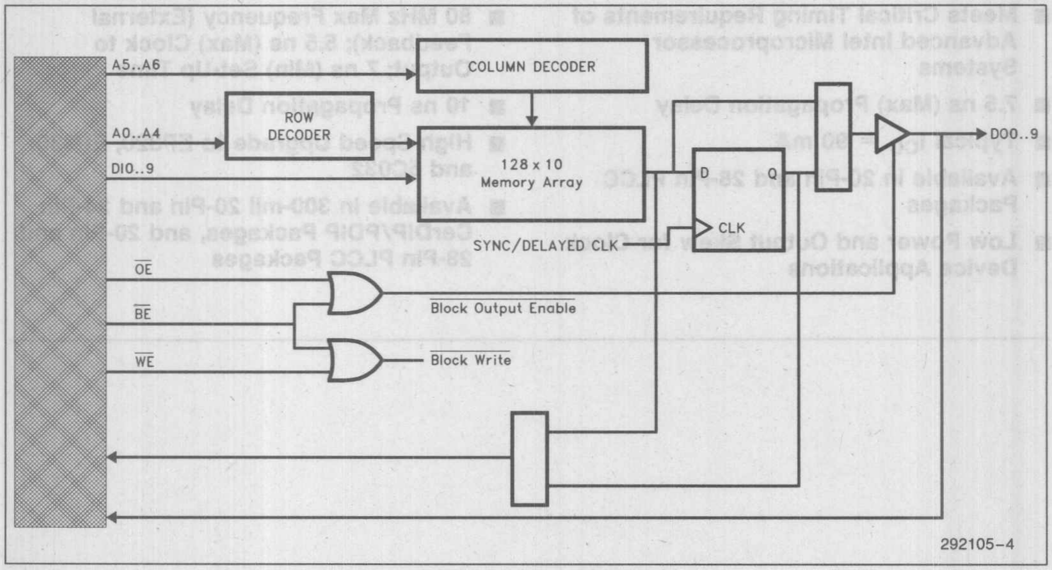

Figure 4. CFB as SRAM

FAST REGISTERED SPEED T_{SU}, T_{SO} 8-MACROCELL PLDs

These register optimized timing PLDs offer superior design features:

- Low-Power, High-Performance Upgrade for SSI/MSI Logic and Bipolar PALs* High-Performance Systems
- Replacement or Upgrade for 16V8/20V8 PAL and GAL Architecture
- 8 Macrocells with Independently Programmable I/O Architecture
- Up to 18 Inputs (10 Dedicated and 8 I/O) and 8 Outputs
- Programmable "Security Bit" Allows Total Protection of Proprietary Designs
- 100% Generally Tested Logic Array

85C220-100 AND 85C224-100

- 100 MHz Max Frequency (External Feedback); 5.5 ns (Max) Clock to Output; 4.5 ns (Min) Set-Up Time
- Meets Critical Timing Requirements of Advanced Intel Microprocessor Systems
- 7.5 ns (Max) Propagation Delay
- Typical I_{CC} = 90 mA
- Available in 20-Pin and 28-Pin PLCC Packages
- Low Power and Output Skew for Clock Device Applications

85C220-80 AND 85C224-80

- Quarter Power (I_{CC} = 40 mA); Programmable Zero Power Mode (50 μA Typical)
- 80 MHz Max Frequency (External Feedback); 5.5 ns (Max) Clock to Output; 7 ns (Min) Set-Up Time
- 10 ns Propagation Delay
- High-Speed Upgrade to EP320, EP330, and 5C032
- Available in 300-mil 20-Pin and 24-Pin CerDIP/PDIP Packages, and 20-Pin and 28-Pin PLCC Packages

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October 1993
Order Number: 290224-005

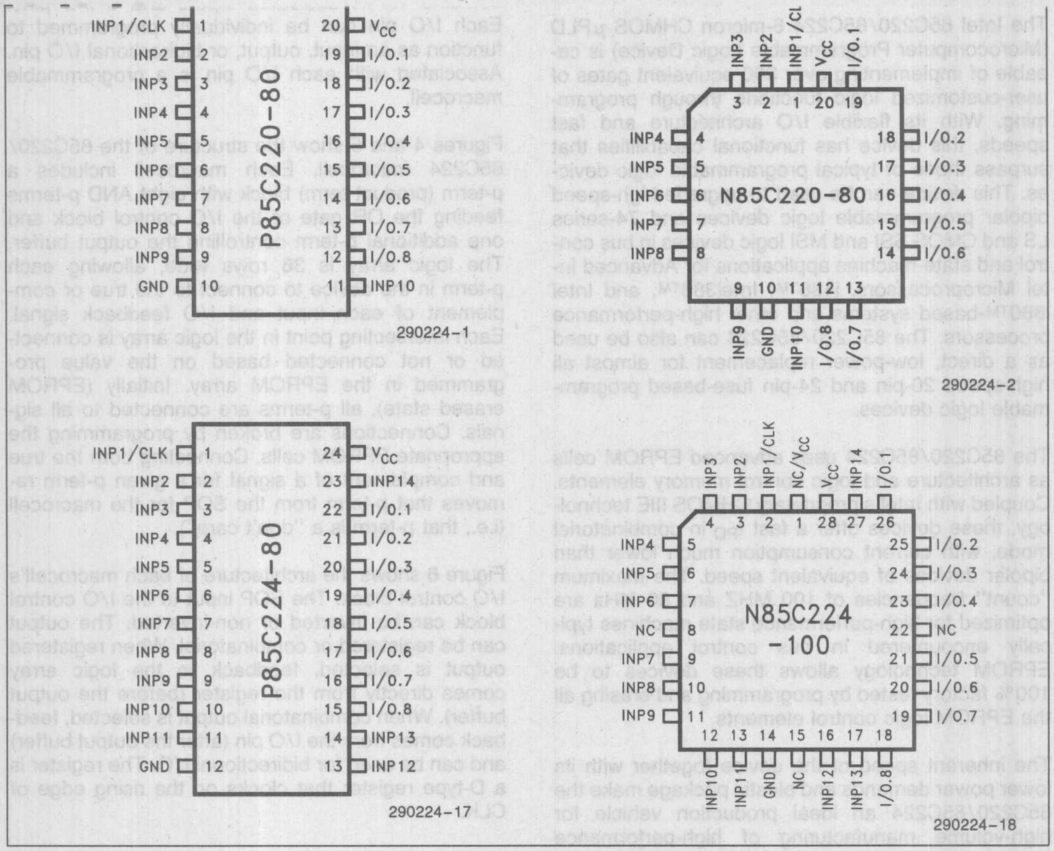


Figure 1. Pinout Diagrams

High Frequency/Low Output Skew Clock Driver

The 85C220 and 85C224-100 displays dramatically reduced output pin skew in comparison with industry clock driver products. With high performance systems relying on increasingly faster clocking frequencies, managing the timing of high frequency system clocks is now more important than ever. Whether the configuration is combinatorial (as with a clock driver) or registered (as with a frequency divider) the output skew (T_{OS}) is typically less than 300 pico seconds! The extremely low output skew of the 85C220 and 85C224 make the devices ideal for a variety of high frequency system clock related applications including Pentium™ microprocessor, Intel486 and PCI Bus designs. The 85C224-100 combines the flexibility of programmable logic with the industry's lowest output skew.

INTRODUCTION

The Intel 85C220/85C224 8-micron CHMOS μPLD (Microcomputer Programmable Logic Device) is capable of implementing over 300 equivalent gates of user-customized logic functions through programming. With its flexible I/O architecture and fast speeds, this device has functional capabilities that surpass those of typical programmable logic devices. This device can be used to upgrade high-speed bipolar programmable logic devices and 74-series LS and CMOS SSI and MSI logic devices in bus control and state-machine applications for Advanced Intel Microprocessors, i486™, Intel386™, and Intel i860™-based systems and other high-performance processors. The 85C220/85C224 can also be used as a direct, low-power replacement for almost all high-speed 20-pin and 24-pin fuse-based programmable logic devices.

The 85C220/85C224 uses advanced EPROM cells as architecture and logic control memory elements. Coupled with Intel's proprietary CHMOS IIIE technology, these devices offer a fast t_{PD} in combinatorial mode, with current consumption much lower than bipolar devices of equivalent speed. The maximum "count" frequencies of 100 MHZ and 80 MHz are optimized for high-performance state machines typically encountered in bus control applications. EPROM technology allows these devices to be 100% factory tested by programming and erasing all the EPROM logic control elements.

The inherent speed of the device together with its lower power demands and plastic package make the 85C220/85C224 an ideal production vehicle for high-volume manufacturing of high-performance systems. The 85C220/85C224 will improve performance and reliability, while decreasing system noise, power consumption and heat generation.

ARCHITECTURE DESCRIPTION

The architecture of the 85C220/85C224 is based on the SOP (Sum of Products) PAL structure with a programmable AND array feeding into a fixed OR array. Programmable macrocells allow the device to accommodate both combinatorial and sequential logic functions. Each macrocell is individually programmable for combinatorial or registered output. An invert option on the SOP allows each output to be configured as an active-high or active-low output.

As shown in Figures 2 and 3, the 85C220/85C224 contains 10/14 dedicated inputs and 8 I/O pins. Each I/O pin can be individually programmed to function as an input, output, or bidirectional I/O pin. Associated with each I/O pin is a programmable macrocell.

Figures 4 and 5 show the structure of the 85C220/85C224 macrocell. Each macrocell includes a p-term (product term) block with eight AND p-terms feeding the OR gate of the I/O control block and one additional p-term controlling the output buffer. The logic array is 36 rows wide, allowing each p-term in the device to connect to the true or complement of each input and I/O feedback signal. Each intersecting point in the logic array is connected or not connected based on the value programmed in the EPROM array. Initially (EPROM erased state), all p-terms are connected to all signals. Connections are broken by programming the appropriate EPROM cells. Connecting both the true and complement of a signal for a given p-term removes that p-term from the SOP for the macrocell (i.e., that p-term is a "don't care").

Figure 6 shows the architecture of each macrocell's I/O control block. The SOP input to the I/O control block can be inverted or non-inverted. The output can be registered or combinatorial. When registered output is selected, feedback to the logic array comes directly from the register (before the output buffer). When combinatorial output is selected, feedback comes from the I/O pin (after the output buffer) and can be used for bidirectional I/O. The register is a D-type register that clocks on the rising edge of CLK.

20-PIN AND 24-PIN PLD COMPATIBILITY

The 85C220/85C224 is designed to be a logical superset of most high-speed 20-pin and 24-pin bipolar PAL and GAL devices. The I/O and logic sections of the device can be configured to emulate any of the devices listed below. Designers can often replace multiple PALs with fewer 85C220/85C224 devices. Tables 1 and 2 include some of the devices with which the 85C220/85C224 are compatible.

Table 1. Replacement/Upgrade

10 ns—20-Pin and 24-Pin		
Company	**20-Pin Part**	**24-Pin Part**
Intel	**85C220-80**	**85C224-80**
AMD	PAL16L8D	PAL20L8-10
AMD	PAL16R8D	PAL20R8-10
AMD	PAL16R8-7	PAL20R8-7
AMD	PALCE16V8	PALCE20V8
National	GAL16V8A	GAL20V8A
National	PAL16L8D	PAL20L8D
National	PAL16R8D	PAL20R8D
National	PAL16R8-7	N/A
Signetics	PLUS16L8D	PLUS20L8D
Signetics	PLUS16R8D	PLUS20R8D
Signetics	PLUS16R8-7	PLUS20R8-7
TI	TIBPAL16L8-10	TIBPAL20L8-10
TI	TIBPAL16R8-10	TIBPAL20R8-10
TI	TIBPAL16R8-7	TIBPAL20R8-7

Table 2. Replacement/Upgrade

12 ns—20-Pin and 24-Pin		
Company	**20-Pin Part**	**24-Pin Part**
Intel	**85C220-66**	**85C224-66**
AMD	PAL16L8	PAL20L8
AMD	PAL16R8	PAL20R8
AMD	PALCE16V8	PALCE20V8
Cypress	PALC16L8	PALC20L8
Cypress	PALC16R8	PALC20R8
National	GAL16V8A	GAL20V8A
National	PAL16L8	PAL20L8
National	PAL16R8	PAL20R8
Signetics	PLUS16L8	PLUS20L8
Signetics	PLUS16R8	PLUS20R8
TI	TIBPAL16L8	TIBPAL20L8
TI	TIBPAL16R6	TIBPAL20R6
TI	TIBPAL16R8	TIBPAL20R8

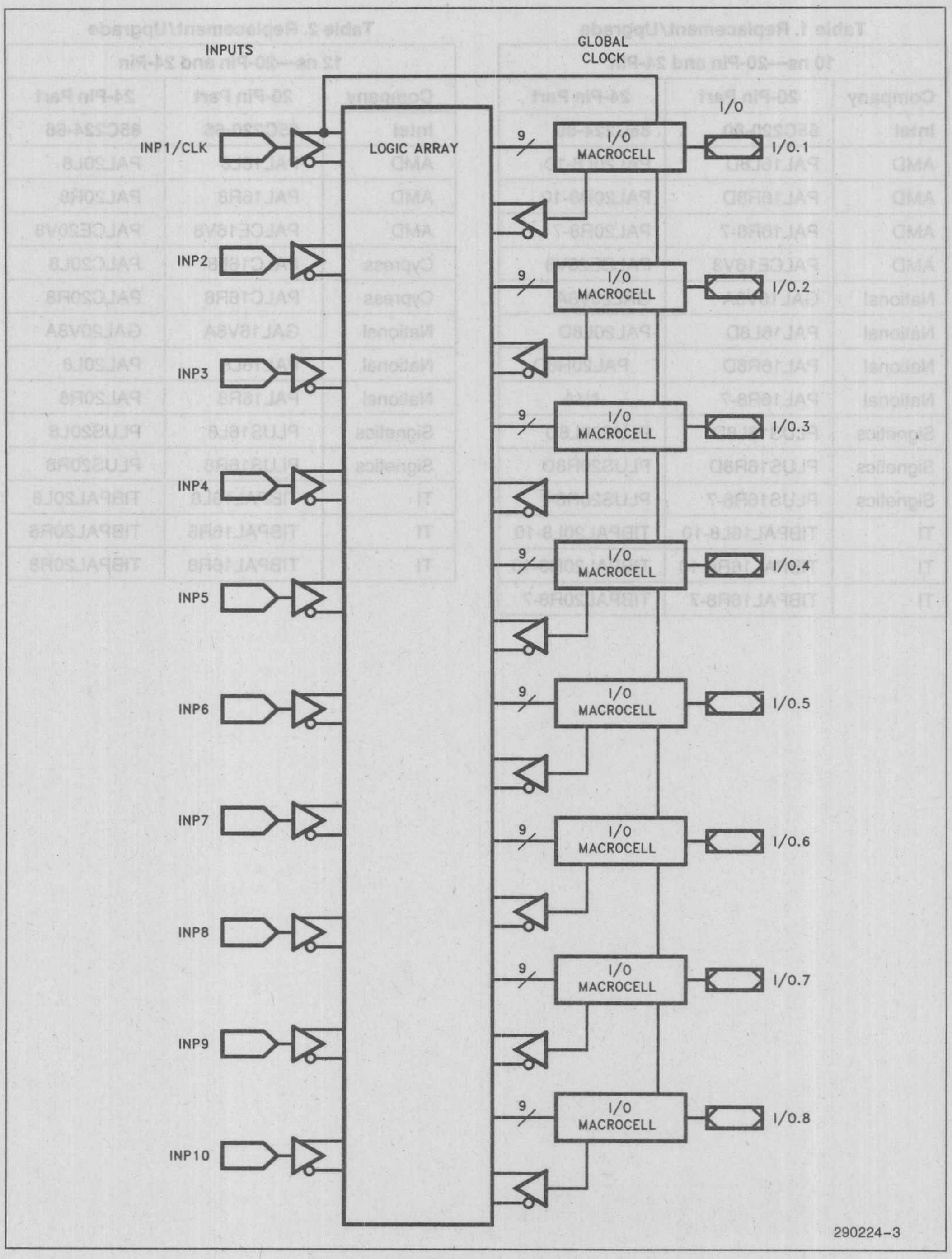


Figure 2. 85C220 Global Architecture

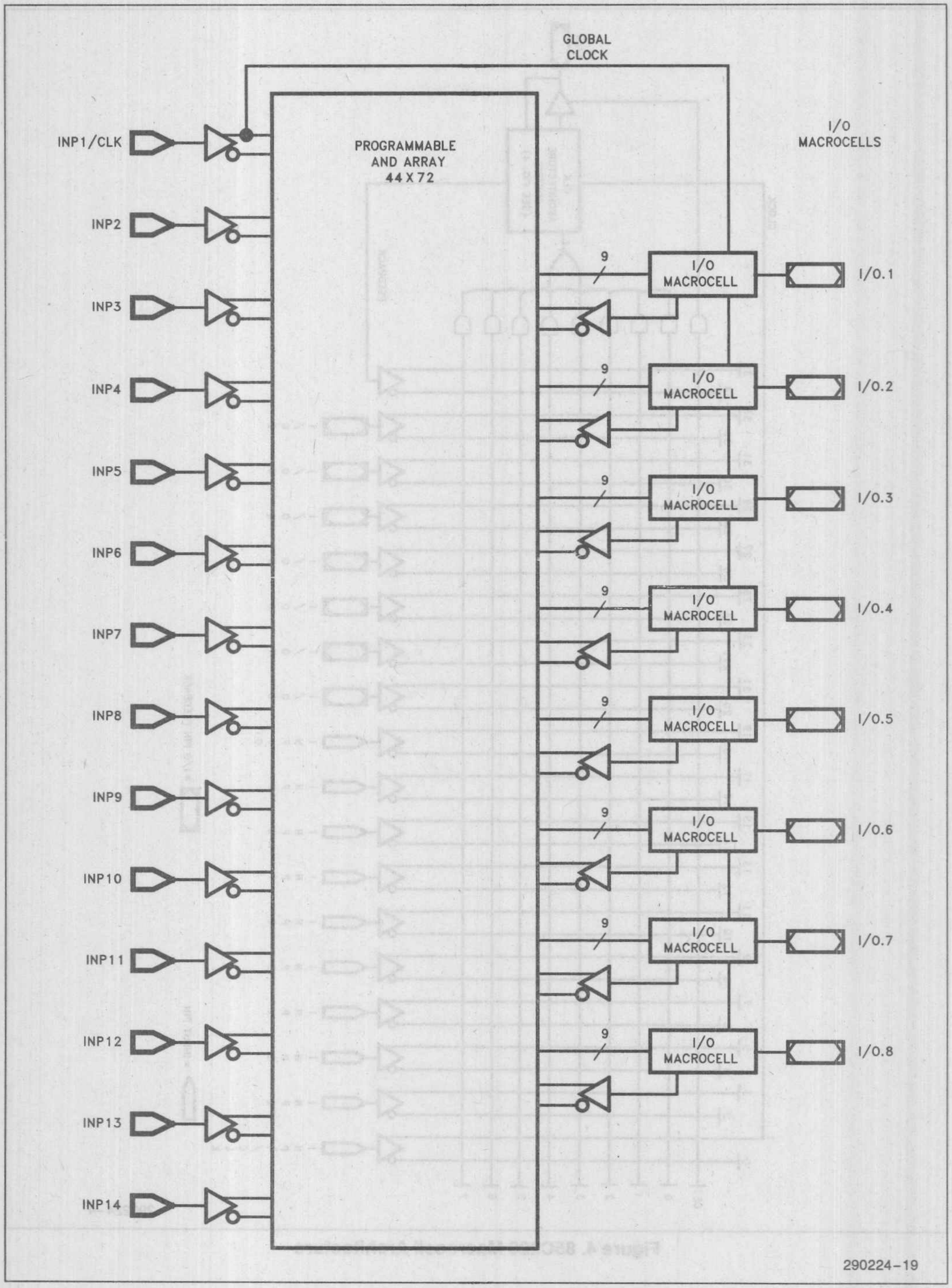
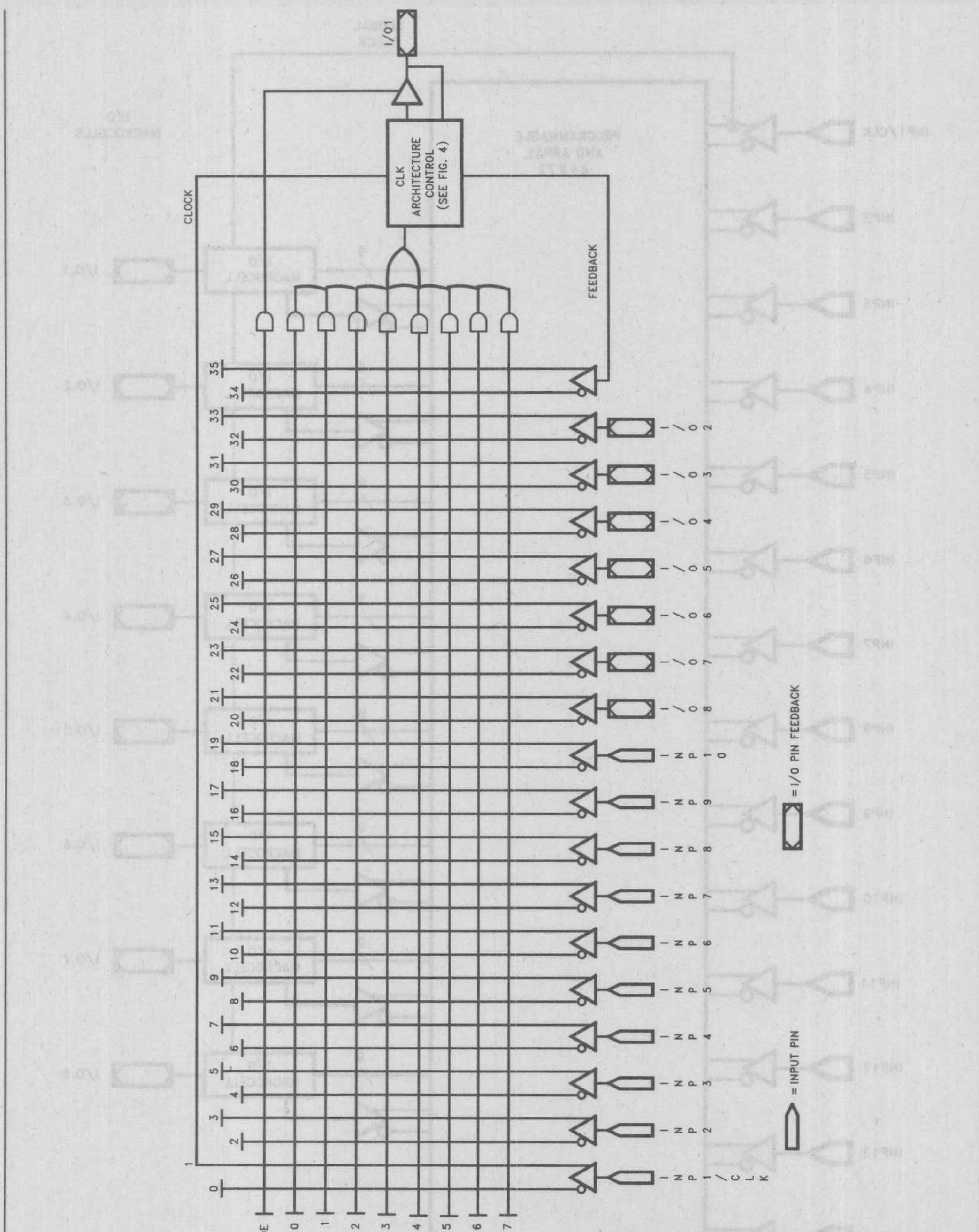


Figure 3. 85C224 Global Architecture



290224-4

Figure 4. 85C220 Macrocell Architecture

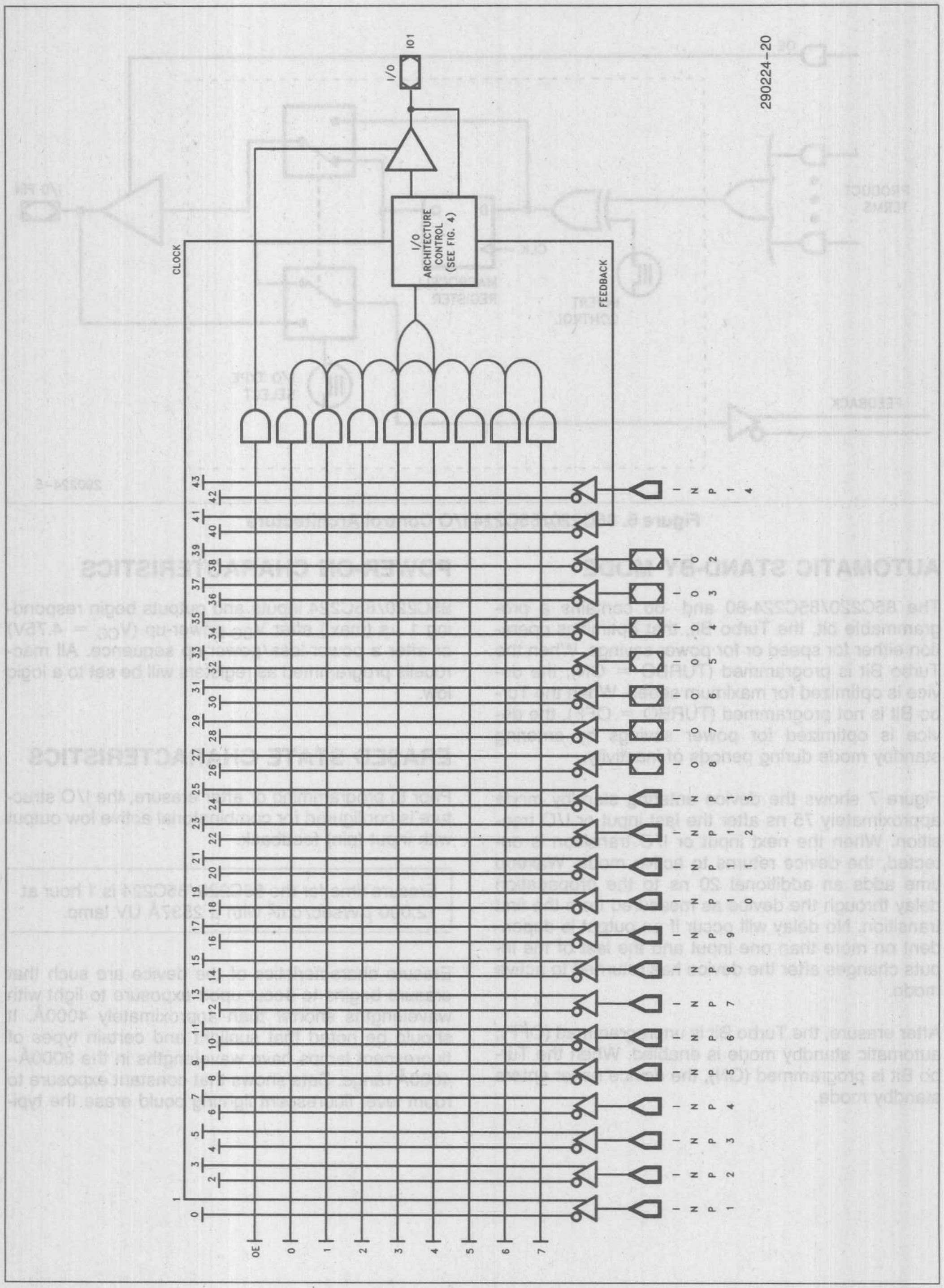


Figure 5. 85C224 Macrocell Architecture

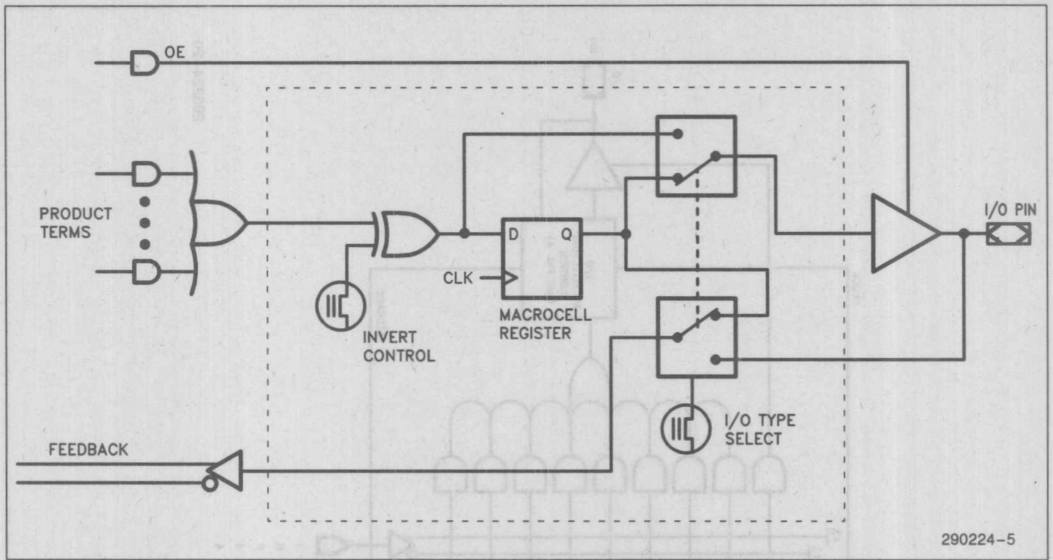


Figure 6. 85C220/85C224 I/O Control Architecture

AUTOMATIC STAND-BY MODE

The 85C220/85C224-80 and -66 contains a programmable bit, the Turbo Bit, that optimizes operation either for speed or for power savings. When the Turbo Bit is programmed (TURBO = ON), the device is optimized for maximum speed. When the Turbo Bit is not programmed (TURBO = OFF), the device is optimized for power savings by entering standby mode during periods of inactivity.

Figure 7 shows the device entering standby mode approximately 75 ns after the last input or I/O transition. When the next input or I/O transition is detected, the device returns to active mode. Wakeup time adds an additional 20 ns to the propagation delay through the device as measured from the first transition. No delay will occur if an output is dependent on more than one input and the last of the inputs changes after the device has returned to active mode.

After erasure, the Turbo Bit is unprogrammed (OFF); automatic standby mode is enabled. When the Turbo Bit is programmed (ON), the device never enters standby mode.

POWER-ON CHARACTERISTICS

85C220/85C224 inputs and outputs begin responding 1 μs (max.) after V_{CC} power-up (V_{CC} = 4.75V) or after a power-loss/power-up sequence. All macrocells programmed as registers will be set to a logic low.

ERASED STATE CHARACTERISTICS

Prior to programming or after erasure, the I/O structure is configured for combinatorial active low output with input (pin) feedback.

Erasure time for the 85C220/85C224 is 1 hour at 12,000 μWsec/cm^2 with a 2537Å UV lamp.

Erasure characteristics of the device are such that erasure begins to occur upon exposure to light with wavelengths shorter than approximately 4000Å. It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000Å–4000Å range. Data shows that constant exposure to room level fluorescent lighting could erase the typi-

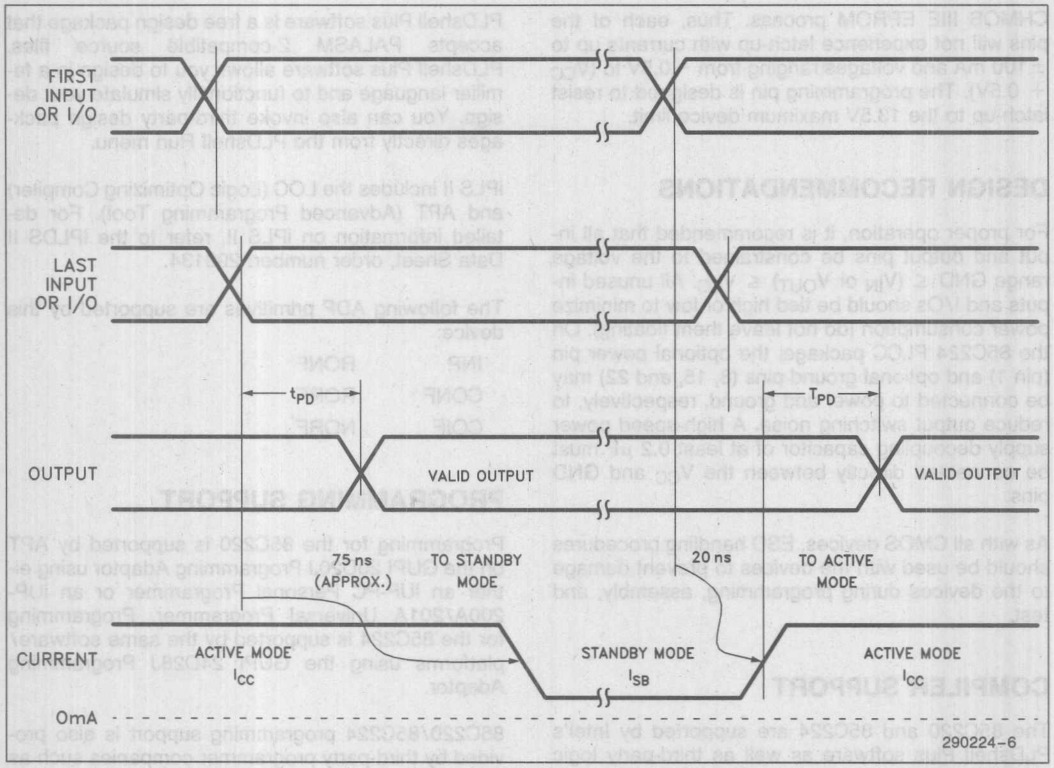


Figure 7. 85C220/85C224 Standby and Active Mode Transitions

cal 85C220/85C224 in approximately six years, while it would take approximately two weeks to erase the device when exposed to direct sunlight. If the device is to be exposed to these lighting conditions for extended periods of time, conductive opaque labels should be placed over the device window to prevent unintentional erasure.

The recommended erasure procedure for the 85C220/85C224 is exposure to shortwave utraviolet light with a wavelength 2537Å. The integrated dose (i.e., UV intensity x exposure time) for erasure should be a minimum of forty (40) Wsec/cm^2. The erasure time with this dosage is approximately 1 hour using an ultraviolet lamp with a 12,000 μW/cm^2 power rating. The device should be placed within 1 inch of the lamp tubes during exposure. The maximum integrated dose the 85C220/85C224 can be exposed to without damage is 7258 Wsec/cm^2 (1 week at 12,000 μW/cm^2). Exposure to high intensity UV light for longer periods may cause permanent damage to the device.

Intelligent Programming Algorithm

The 85C220/85C224 support the Intelligent Programming Algorithm, which rapidly programs Intel EPLDs, and many of Intel's microcontrollers and EPROMs while maintaining a high degree of reliability. It is particularly suited for production programming environments. This method decreases the overall programming time while reliability is ensured as the incremental programming margin of each bit has been verified during programming. Programming voltage and waveform specifications are available by request from Intel to support device programming.

LATCH-UP IMMUNITY

All of the input, output, and clock pins of the device have been designed to resist latch-up which is inherent in inferior CMOS structures. The 85C220/85C224 is designed with Intel's proprietary 1-micron

CHMOS IIIE EPROM process. Thus, each of the pins will not experience latch-up with currents up to ± 100 mA and voltages ranging from $-0.5V$ to (V_{CC} + 0.5V). The programming pin is designed to resist latch-up to the 13.5V maximum device limit.

DESIGN RECOMMENDATIONS

For proper operation, it is recommended that all input and output pins be constrained to the voltage range GND $\leq$ (V_{IN} or V_{OUT}) $\leq$ V_{CC}. All unused inputs and I/Os should be tied high or low to minimize power consumption (do not leave them floating). On the 85C224 PLCC package, the optional power pin (pin 1) and optional ground pins (8, 15, and 22) may be connected to power and ground, respectively, to reduce output switching noise. A high-speed power supply decoupling capacitor of at least 0.2 μF must be connected directly between the V_{CC} and GND pins.

As with all CMOS devices, ESD handling procedures should be used with the devices to prevent damage to the devices during programming, assembly, and test.

COMPILER SUPPORT

The 85C220 and 85C224 are supported by Intel's PLDshell Plus software as well as third-party logic compilers such as ABEL*, CUPL*, PLDDesigner*, Log/IC*, etc.

PLDshell Plus software is a free design package that accepts PALASM 2-compatible source files. PLDshell Plus software allows you to design in a familiar language and to functionally simulate your design. You can also invoke third-party design packages directly from the PLDshell Run menu.

iPLS II includes the LOC (Logic Optimizing Compiler) and APT (Advanced Programming Tool). For detailed information on iPLS II, refer to the iPLDS II Data Sheet, order number: 290134.

The following ADF primitives are supported by this device:

INP	RONF
CONF	RORF
COIF	NORF

PROGRAMMING SUPPORT

Programming for the 85C220 is supported by APT on the GUPI 20D20J Programming Adaptor using either an iUP-PC Personal Programmer or an iUP-200A/201A Universal Programmer. Programming for the 85C224 is supported by the same software/platforms using the GUPI 24D28J Programming Adaptor.

85C220/85C224 programming support is also provided by third-party programmer companies such as Data I/O, Logical Devices, STAG, etc. Please refer to the "Programming Support" lists in the *Programmable Logic* handbook for complete information and vendor contacts.

ORDERING INFORMATION

f_{CNT1} (MHz)	f_{MAX} (MHz)	t_{PD} (ns)	Order Code 20-Pin	Order Code 24-Pin	Package	Operating Range
100	115	7.5	N85C220-100	N85C224-100	PLCC	Commercial
80	111	10	D85C220-80	D85C224-80	†CerDIP	Commercial
			P85C220-80	P85C224-80	PDIP	
			N85C220-80	N85C224-80	PLCC	
66	90.9	12	D85C220-66	D85C224-66	†CerDIP	Commercial
			P85C220-66	P85C224-66	PDIP	
			N85C220-66	N85C224-66	PLCC	

†Windowed CerDIP package allows UV erase.

*ABEL is a trademark of Data I/O, Corporation. CUPL is a trademark of Logical Devices, Inc. PLDesigner is a trademark of MINC, Inc.

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage (V_{CC})(1) .... −2.0V to +7.0V

Programming Supply Voltage (V_{PP})(1) .... −2.0V to +13.5V

D.C. Input Voltage (V_I)(1, 2) ... −0.5V to V_{CC} +0.5V

Storage Temperature (T_{STG}) .... −65°C to +150°C

Ambient Temperature (T_{AMB})(3) .. −10°C to +85°C

NOTES:
1. Voltages with respect to GND.
2. Minimum D.C. input is −0.5V. During transitions, the inputs may undershoot to −2.0V or overshoot to +7.0V for periods of less than 20 ns under no load conditions.
3. Under bias. Extended Temperature versions are also available.

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

2

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Units
V_{CC}	Supply Voltage	4.75	5.25	V
V_{IN}	Input Voltage	0	V_{CC}	V
V_O	Output Voltage	0	V_{CC}	V
T_A	Operating Temperature	0	+70	°C
t_R	Input Rise Time		500	ns
t_F	Input Fall Time		500	ns

D.C. CHARACTERISTICS (T_A = 0°C to +70°C, V_{CC} = 5.0V ±5%)

85C220/85C224-100

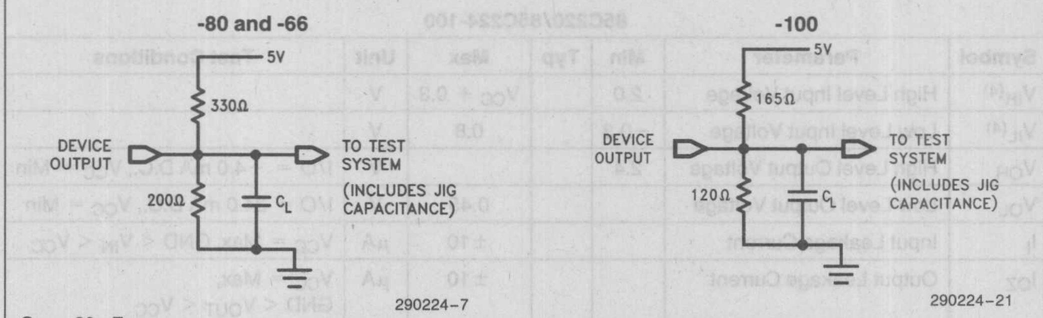
Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}(4)	High Level Input Voltage	2.0		V_{CC} + 0.3	V	
V_{IL}(4)	Low Level Input Voltage	−0.3		0.8	V	
V_{OH}	High Level Output Voltage	2.4			V	I/O = −4.0 mA D.C., V_{CC} = Min
V_{OL}	Low Level Output Voltage			0.45	V	I/O = 24.0 mA D.C., V_{CC} = Min
I_I	Input Leakage Current			±10	μA	V_{CC} = Max, GND < V_{IN} < V_{CC}
I_{OZ}	Output Leakage Current			±10	μA	V_{CC} = Max, GND < V_{OUT} < V_{CC}
I_{SC}(6)	Output Short Circuit Current	−30		−120	mA	V_{CC} = Max, V_{OUT} = 0.5V
I_{CC}	Power Supply Current		60	90	mA	V_{CC} = Max, V_{IN} = V_{CC} or GND, No Load, f_{IN} = 25 MHz, Device Prog. as an 8-Bit Counter
			85	115	mA	f_{IN} = 100 MHz

85C220/85C224-80 and -66

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
$V_{IH}^{(4)}$	High Level Input Voltage	2.0		$V_{CC}+0.3$	V	
$V_{IL}^{(4)}$	Low Level Input Voltage	−0.3		0.8	V	
V_{OH}	High Level Output Voltage	2.4			V	$I_O = -4.0$ mA D.C., V_{CC} = Min
$V_{OL}^{(5)}$	Low Level Output Voltage			0.45	V	$I_O = 12.0$ mA D.C., V_{CC} = Min
I_I	Input Leakage Current			±10	μA	V_{CC} = Max, GND < V_{IN} < V_{CC}
I_{OZ}	Output Leakage Current			±10	μA	V_{CC} = Max, GND < V_{OUT} < V_{CC}
$I_{SC}^{(6)}$	Output Short Circuit Current	−30		−120	mA	V_{CC} = Max, V_{OUT} = 0.5V
$I_{SB}^{(7)}$	Standby Current		50	500	μA	V_{CC} = Max, V_{IN} = V_{CC} or GND, Standby Mode
I_{CC}	Power Supply Current (see I_{CC} vs Frequency Graph)		2	5	mA	V_{CC} = Max, V_{IN} = V_{CC} or GND, No Load, f_{IN} = 1 MHz, Device Prog. as an 8-Bit Counter, Non-Turbo Mode
			35	50	mA	f_{IN} = 15 MHz, Active Mode
			45	60	mA	f_{IN} = 80 MHz, Active Mode

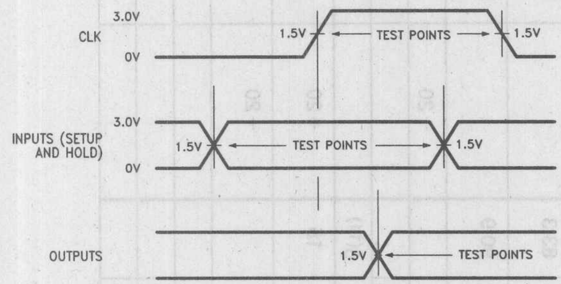
NOTES:
4. Absolute values with respect to device GND; all over and undershoots due to system or tester noise are included.
5. Maximum DC I_{OL} for the device (all 8 outputs) is 64 mA.
6. Not more than 1 output should be tested at a time. Duration of that test should not exceed 1 second.
7. In Non-Turbo Mode (TURBO = OFF), device enters standby mode approximately 75 ns after the last input transition.

A.C. TESTING LOAD CIRCUIT



C_L = 30 pF

A.C. TESTING WAVEFORM—SYNCHRONOUS INPUTS AND OUTPUTS



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A.C. Testing: Inputs (including CLK) are driven at 3.0V for a Logic "1" and 0V for a Logic "0". Setup and hold input measurements relative to CLK are made at 2.0V on CLK (low-to-high transition). Inputs are measured at 2.0V for a high and 0.8V for a low. Outputs are measured at 1.5V. Device input rise and fall times are less than 3 ns.

2

CAPACITANCE (T_A = 0°C to +70°C; V_{CC} = 5.0V ±5%)(8)

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
C_{IN}	Input Capacitance		4	6	pF	V_{IN} = 0V, f = 1.0 MHz
C_{IO}	I/O Capacitance		5	8	pF	V_{OUT} = 0V, f = 1.0 MHz
C_{CLK}	CLK Capacitance		6	8	pF	V_{OUT} = 0V, f = 1.0 MHz
C_{VPP}	V_{PP} Pin Capacitance		8	10	pF	V_{PP} on Pin 11/13, f = 1.0 MHz

NOTES:
8. These values are evaluated during initial characterization and whenever design modifications occur that may affect capacitance.

A.C. CHARACTERISTICS (T_A = 0°C to +70°C, V_{CC} = 5.0V ±5%)(9)

Symbol	Parameter	85C220-100/ 85C224-100			85C220-80/ 85C224-80			85C220-66/ 85C224-66			Non-Turbo(10) Mode	Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
t_{PD}(11)	Input or I/O to Output	3		7.5	4		10	4		12	+20	ns
t_{PZX}(12)	Input or I/O to Output Enable	3		9	4		12	4		12	+20	ns
t_{PXZ}(12)	Input or I/O to Output Disable	3		9	4		10	4		12	+20	ns
T_{os}	Registered Output Skew	150	250	300								ps
T_{os}	Comb. Output Skew	150	300	400								ps

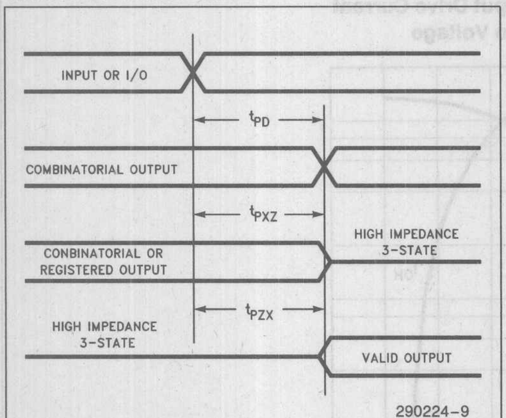
NOTES:
9. Typical values are at T_A = +25°C, V_{CC} = 5V, Active Mode.
10. If device is operated in Standby Mode (Standby bit = Low) and the device is inactive for approximately 75 ns, increase time by amount shown for -80 and -66 only.
11. Measured with all eight outputs switching.
12. t_{PZX} and t_{PXZ} are measured at ±0.5V from steady state voltage as driven by specification output load. t_{PXZ} is measured with C_L = 5 pF. Measured with all eight outputs switching.

SYNCHRONOUS CLOCK MODE (T_A = 0°C to 70°C, V_{CC} = 5V ±5%)[9]

Symbol	Parameter	85C220-100/ 85C224-100			85C220-80/ 85C224-80			85C220-66 85C224-66			Non-Turbo[10] Mode	Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
f_{CNT1}[11]	Maximum Counter Frequency $1/(t_{SU} + t_{CO})$—External Feedback		111	100		100	80		80	66		MHz
f_{CNT2}[11]	Maximum Counter Frequency $1/(t_{CNT})$—Internal Feedback			115		111	100		90	83.3		MHz
f_{MAX}[11]	Maximum Frequency (Pipelined) $1/(t_{CW})$—No Feedback			115		125	111		100	90.9		MHz
t_{SU}	Input or I/O Setup Time to CLK	4.5			7			9			+20	ns
t_H	Input or I/O Hold Time from CLK	0			0			0				ns
t_{CO1}	CLK High to Output Valid	3		5.5	1.5[13]		5.5[11]	1.5[13]		6[11]		ns
t_{CO2}	CLK High to Output Valid Fed through Comb. Macrocell	4.5		10	4.5		13	4.5		15	+20	ns
t_{CNT}[11]	Macrocell Output Feedback to Macrocell Input—Internal Path	10			10			12			+20	ns
t_{CL}	CLK Low Time	4			4			5				ns
t_{CH}	CLK High Time	4			4			5				ns
t_{CW}	CLK Period	10			9			11				ns

NOTE:
13. t_{CO1} min. is measured with one output switching, T_A = 0°C, V_{CC} = 5.25V.

COMBINATORIAL MODE



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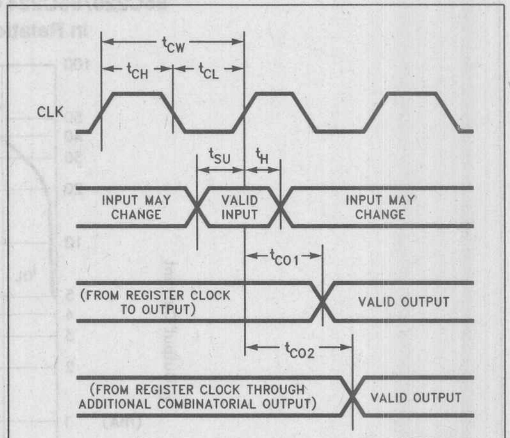
REGISTERED MODE



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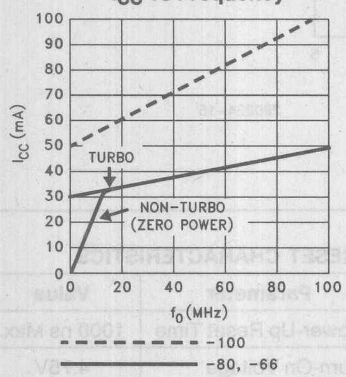
85C220/85224
I_{CC} vs Frequency



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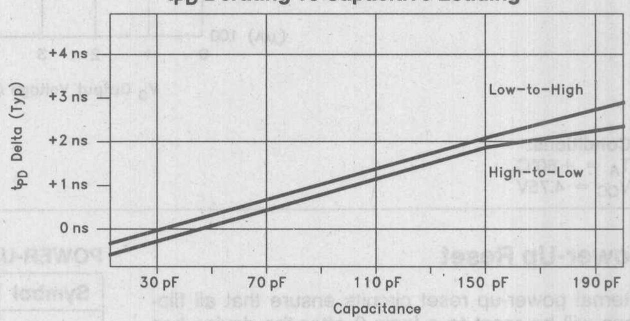
Conditions:
$T_A = 25°C$
$V_{CC} = 5.25V$

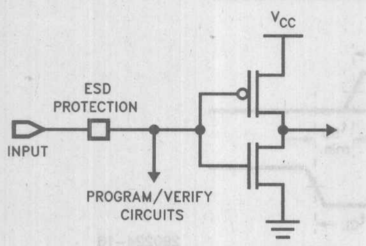
85C220/85C224
t_{PD} Derating vs Capacitive Loading



290224-12

Conditions:
$T_A = 70°C$
$V_{CC} = 4.75V$

INPUT/OUTPUT EQUIVALENT SCHEMATICS



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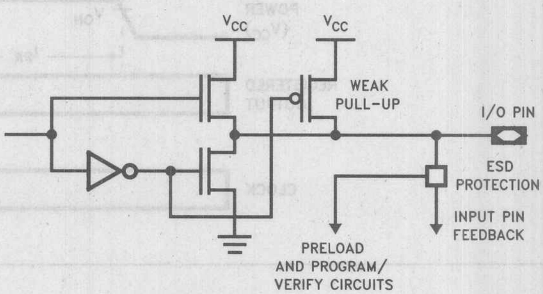

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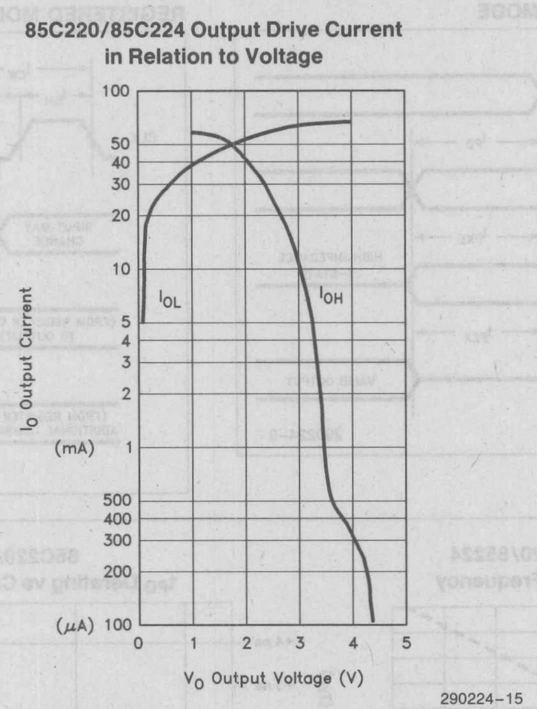


Conditions:
$T_A = +80°C$
$V_{CC} = 4.75V$

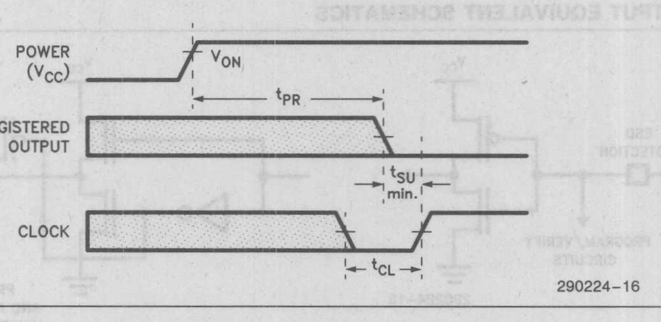
Power-Up Reset

Internal power-up reset circuits ensure that all flip-flops will be reset to a logic 0 after the device has powered up. Because V_{CC} rise can vary significantly from one application to another, V_{CC} rise must be monotonic.

POWER-UP RESET CHARACTERISTICS

Symbol	Parameter	Value
t_{PR}	Power-Up Reset Time	1000 ns Max.
V_{ON}	Turn-On Voltage	4.75V

POWER-UP RESET



PACKAGE/TECHNOLOGY SPECIFICATIONS

Description	85C220	85C224
Θ_{Ja}—Junction-to-Ambient Thermal Resistance	68°C/W—CerDIP 90°C/W—PDIP 90°C/W—PLCC	55°C/W—CerDIP 65°C/W—PDIP 65°C—PLCC
Θ_{Jc}—Junction-to-Case Thermal Resistance	30°C/W—CerDIP 25°C/W—PDIP 25°C/W—PLCC	55°C/W—CerDIP 20°C/W—PDIP 20°C/W—PLCC
Process	CHMOS IIIE, PX29.5	CHMOS IIIE, PX29.5
I_{CC} Hot—Ambient @70°C	40 mA (-80 Only)	
I_{CC} Typical—Ambient @25°C	40 mA (-80 Only)	

REVISION HISTORY

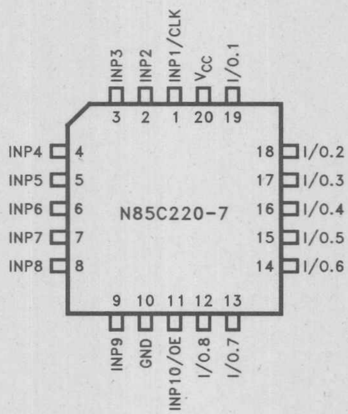
-004 to -005

Addition of specification for clock driver.

85C220/85C224-7 AND -10 FAST T_{PD}, HALF-POWER 8-MACROCELL PLDs

These Combinatorial Optimized Timing PLDs Offer Superior Design Features:

- **High-Performance Low-Power Upgrade for -7 and -10 Bipolar/CMOS* PLD's in High-Performance Systems**
- **t_{PD} 7.5 ns, 74 MHz Frequency with 100 MHz Frequency with Internal Feedback and with No Feedback**
- **Up to 18/22 Inputs and 8 Outputs (18/22 Inputs = 10/14 Dedicated and 8 I/O)**
- **8 I/O Macrocells with Programmable I/O Architecture (Register/Combinatorial)**
- **Low Output Skew for Clock Driver Applications**
- **"Half-Power" I_{CC} = 90 mA Max. at 25 MHz**
- **Output Buffers Optimized for Low-Noise Operation**
- **Extensive Software and Programming Support via Intel and Third-Party Tools**
- **Available in 20-Pin/28-Pin PLCC and 20-Pin/24-Pin PDIP Packages**
  (See Packaging Spec., Order Number 240800, Package Types N and P)



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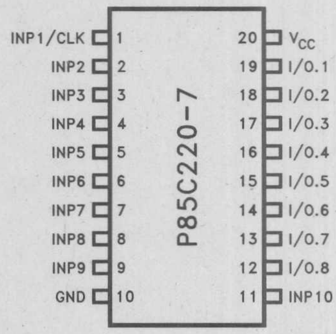

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Figure 1a. Pinout Diagrams

*GAL is a registered trademark of Lattice Semiconductor Corporation.
*PAL is a registered trademark of Advanced Micro Devices.

October 1993
Order Number: 290417-004

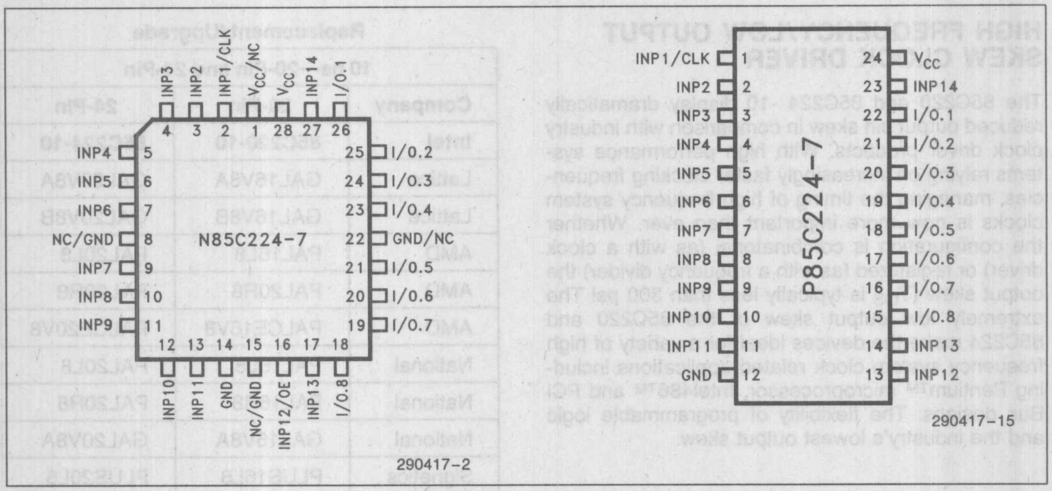

Figure 1b. Pinout Diagrams

INTRODUCTION

The Intel 85C220-7 and 85C224-7 1-micron CMOS μPLDs (Microcomputer Programmable Logic Devices) are superset devices capable of upgrading 7.5 ns PALs/GALs* and 74-series LS and CMOS SSI and MSI logic devices in high-performance microcomputer systems. The inherent speed of the devices together with their lower power demands and plastic packaging make the 85C220 and 85C224 ideal production vehicles for high-volume manufacturing of high-performance systems. These devices can improve performance while decreasing system noise, power consumption, and heat generation.

The 85C220/85C224 use advanced EPROM cells as architecture and logic control memory elements. Coupled with Intel's proprietary CMOS IIIE technology, the devices offer a fast t_{PD} in combinatorial mode, and fast counter frequencies in registered applications with current consumption much lower than bipolar devices of equivalent speed. EPROM technology allows these devices to be 100% factory tested by programming and erasing all the EPROM logic control elements.

ARCHITECTURE DESCRIPTION

The architecture of the devices is based on the SOP (Sum of Products) PAL structure with a programmable AND array feeding into a fixed OR array. Programmable macrocells allow the device to accommodate both combinatorial and sequential logic functions. Each macrocell is individually programmable for combinatorial or registered output. An invert option on the SOP allows each output to be configured as an active-high or active-low output.

As shown in Figure 2, the 85C220 contains 10 dedicated inputs and 8 I/O pins. Figure 3 shows the 85C224, which contains 14 dedicated inputs and 8 I/O pins. On both devices, each I/O pin can be individually programmed to function as an input, output, or bidirectional I/O pin. Associated with each I/O pin is a programmable macrocell.

Figure 4 shows the structure of the 85C220 macrocell; Figure 5 shows the 85C224 macrocell. Each macrocell includes a p-term (product term) block with eight AND p-terms feeding the OR gate of the I/O control block and one additional p-term controlling the output buffer. The global logic array allows each p-term in the devices to connect to the true or complement of each input and I/O feedback signal. The 85C220 contains 36 array rows, while the 85C224 contains 44 array rows. Each intersecting point in the logic array is connected or not connected based on the value programmed in the EPROM array. Initially (EPROM erased state), all p-terms are connected to all signals. Connections are broken by programming the appropriate EPROM cells. Connecting both the true and complement of a signal for a given p-term removes that p-term from the SOP for the macrocell (i.e., that p-term is a "don't care").

Figure 6 shows the architecture of each macrocell's I/O control block. The I/O control blocks for the devices are identical. The SOP input to the I/O control block can be inverted or non-inverted. The output can be registered or combinatorial. When registered output is selected, feedback to the logic array comes directly from the register (before the output buffer). When combinatorial output is selected, feedback comes from the I/O pin (after the output buffer) and can be used for bidirectional I/O. The register is a D-type register that clocks on the rising edge of the global CLK.

HIGH FREQUENCY/LOW OUTPUT SKEW CLOCK DRIVER

The 85C220 and 85C224 -10 display dramatically reduced output pin skew in comparison with industry clock driver products. With high performance systems relying on increasingly faster clocking frequencies, managing the timing of high frequency system clocks is now more important than ever. Whether the configuration is combinatorial (as with a clock driver) or registered (as with a frequency divider) the output skew (T_{OS} is typically less than 300 ps! The extremely low output skew of the 85C220 and 85C224 make the devices ideal for a variety of high frequency system clock related applications including Pentium™ microprocessor, Intel486™ and PCI Bus designs. The flexibility of programmable logic and the industry's lowest output skew.

85C220/85C224-PLD COMPATIBILITY

The 85C224 is a logical superset of most high-speed 24-pin PAL/GAL devices. The I/O and logic sections of the device can be configured to emulate the devices listed. Designers can often replace multiple PALs with the 85C224 devices. In many cases 22V10 devices can also be replaced. The following list includes some of the devices with which 85C224 is compatible.

Replacement/Upgrade

7 ns—20-Pin and 24-Pin		
Company	**20-Pin Part**	**24-Pin Part**
Intel	**85C220-7**	**85C224-7**
Lattice	GAL16V8B	GAL20V8B
AMD	PAL16L8	PAL20L8
AMD	PAL16R8	PAL20R8
AMD	PALCE16V8	PALCE20V8
National	PAL16L8	N/A
National	PAL16R8	N/A
Signetics	PLUS16L8	PLUS20L8
Signetics	PLUS16R8	PLUS20R8
TI	TIBPAL16L8	TIBPAL20L8

Replacement/Upgrade

10 ns—20-Pin and 24-Pin		
Company	**20-Pin**	**24-Pin**
Intel	**85C220-10**	**85C224-10**
Lattice	GAL16V8A	GAL20V8A
Lattice	GAL16V8B	GAL20V8B
AMD	PAL16L8	PAL20L8
AMD	PAL20R8	PAL20R8
AMD	PALCE16V8	PALCE20V8
National	PAL16L8	PAL20L8
National	PAL16R8	PAL20R8
National	GAL16V8A	GAL20V8A
Signetics	PLUS16L8	PLUS20L8
Signetics	PLUS16R8	PLUS20R8
TI	TIBPAL16L8	TIBPAL20L8

NOTES:
- Easy Cross Programming for JEDEC compatibility.
- Extensive software and programming support by Intel and Third-Party Tools.

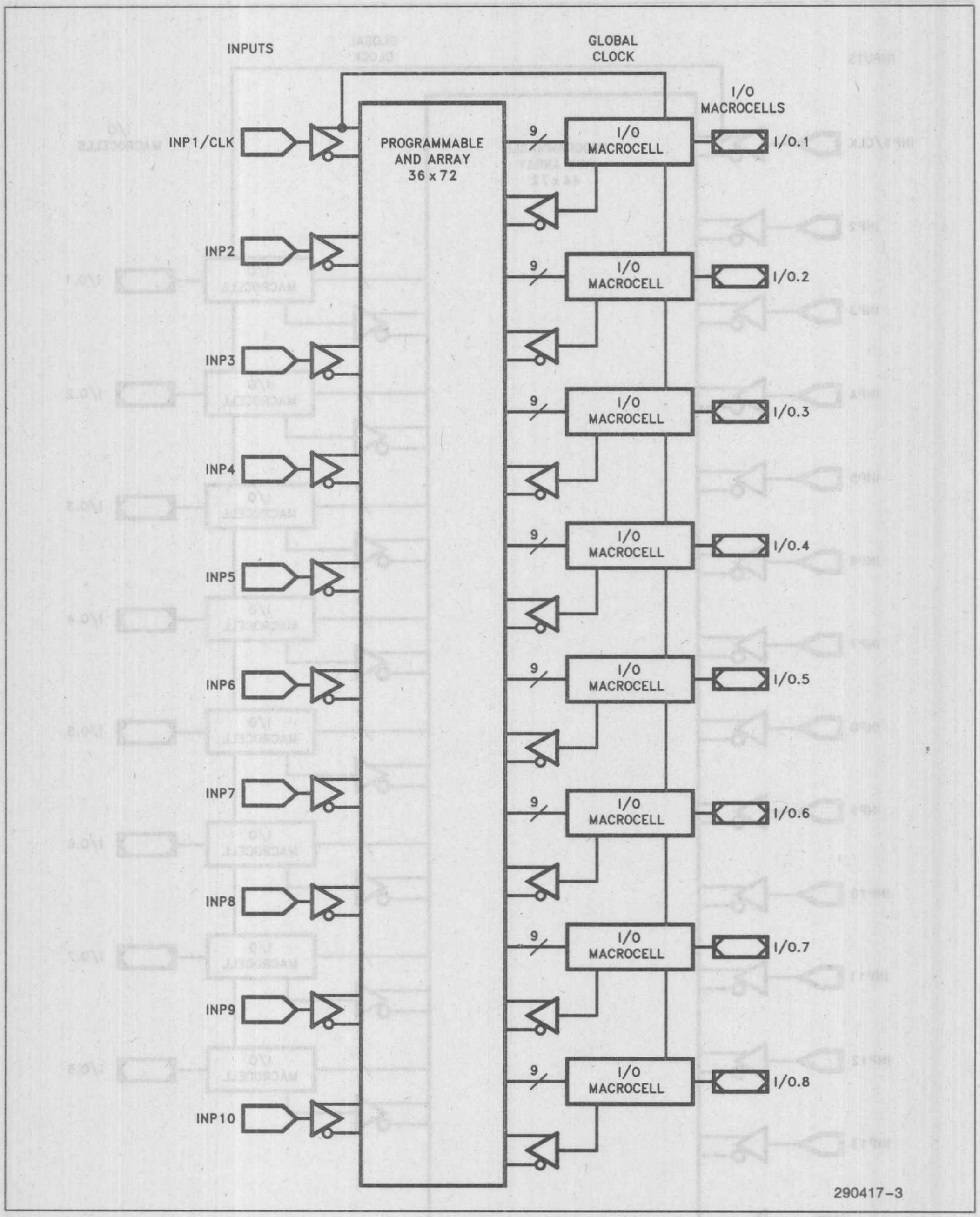

Figure 2. 85C220 Global Architecture

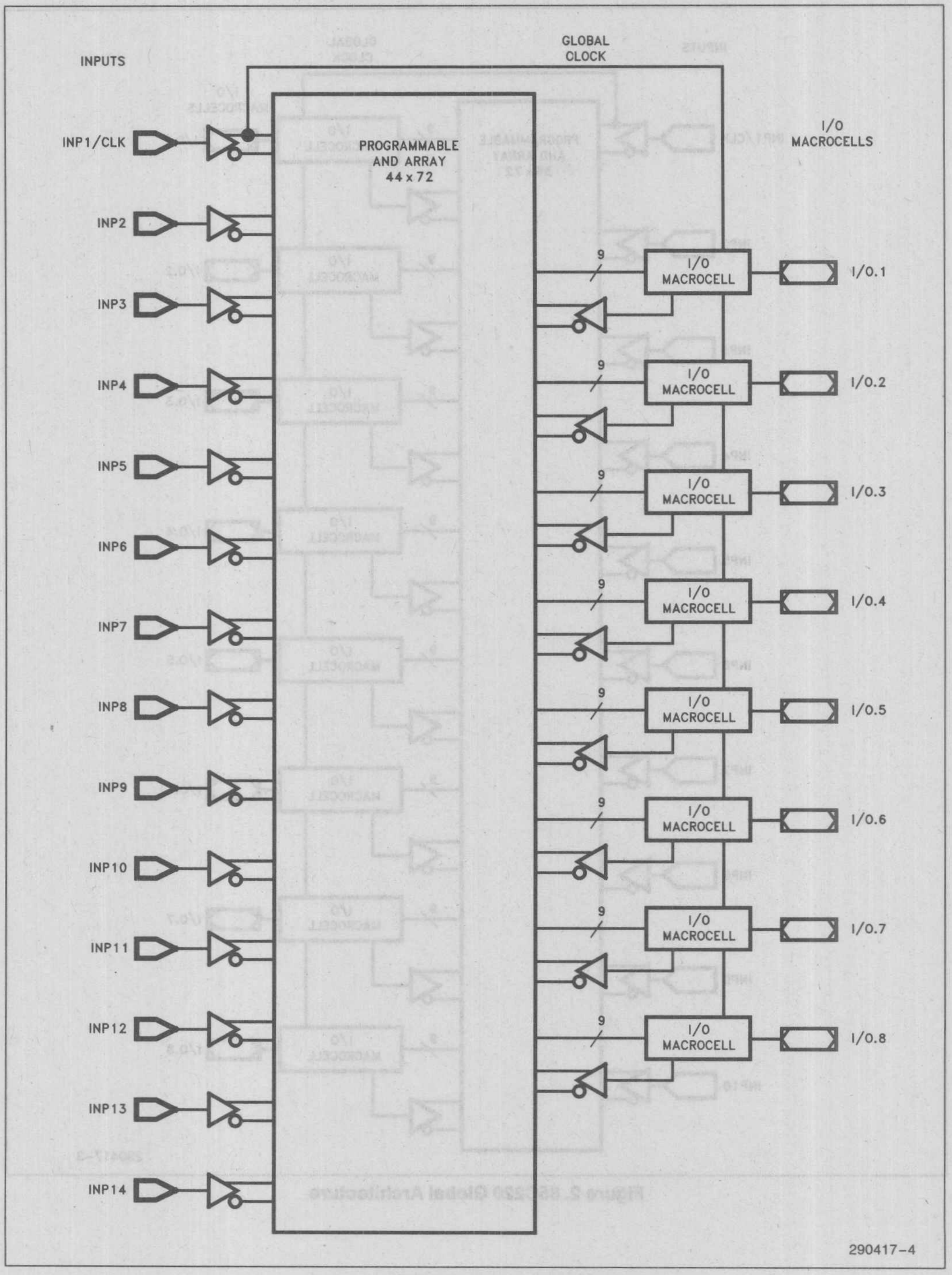

Figure 3. 85C224 Global Architecture

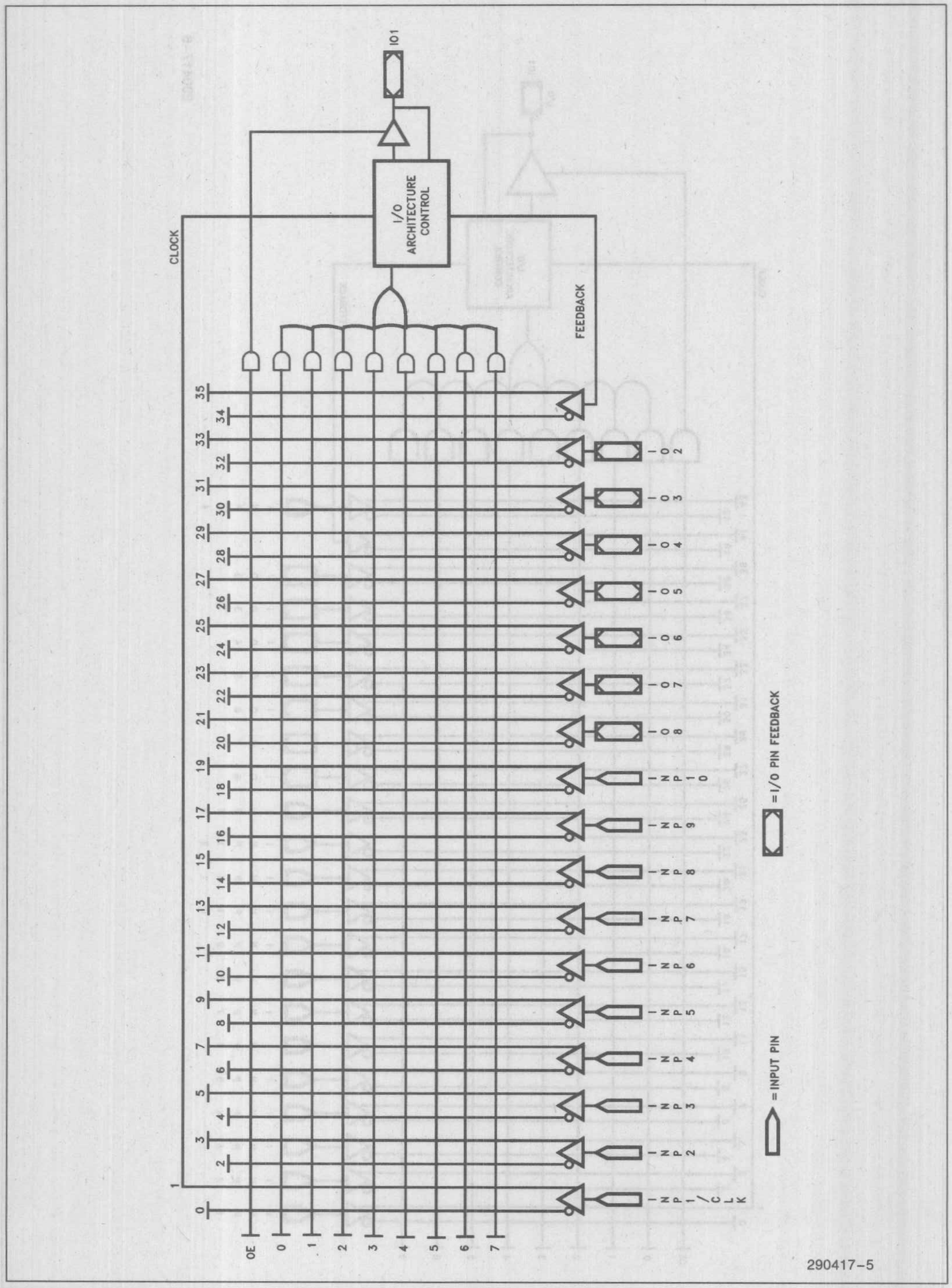

Figure 4. 85C220 Macrocell

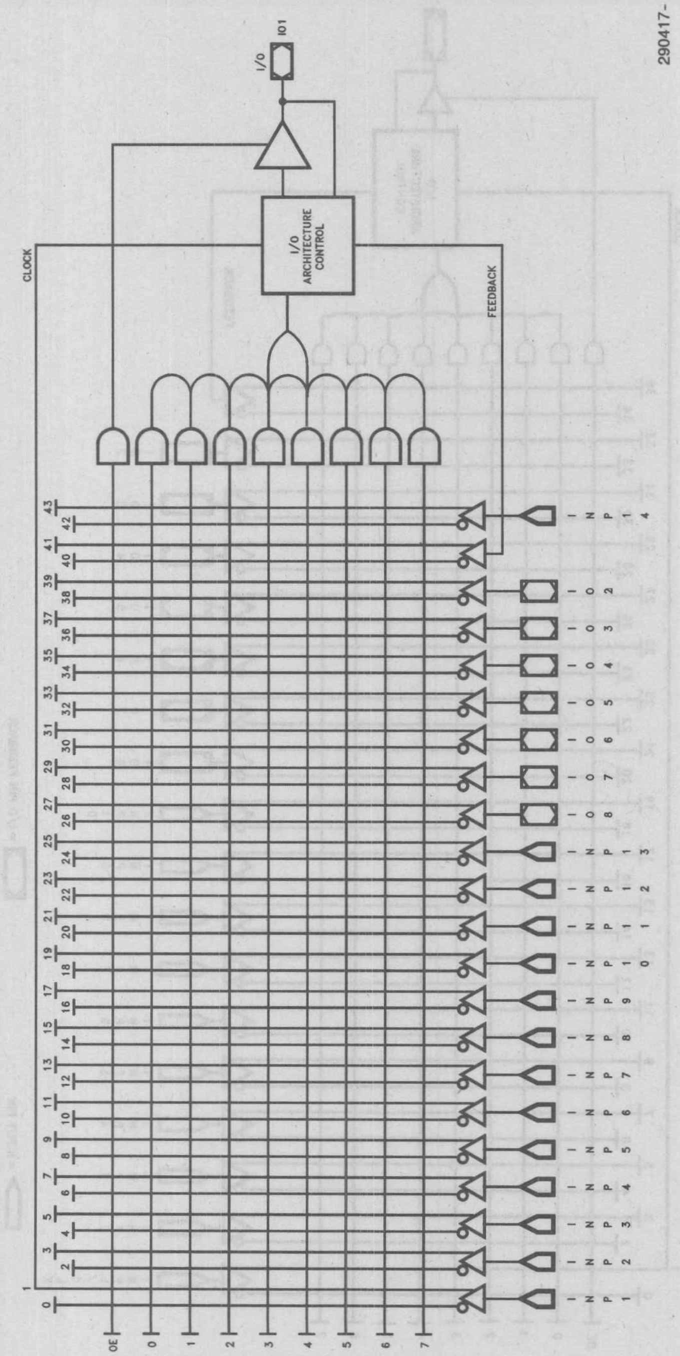

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Figure 5. 85C224 Macrocell

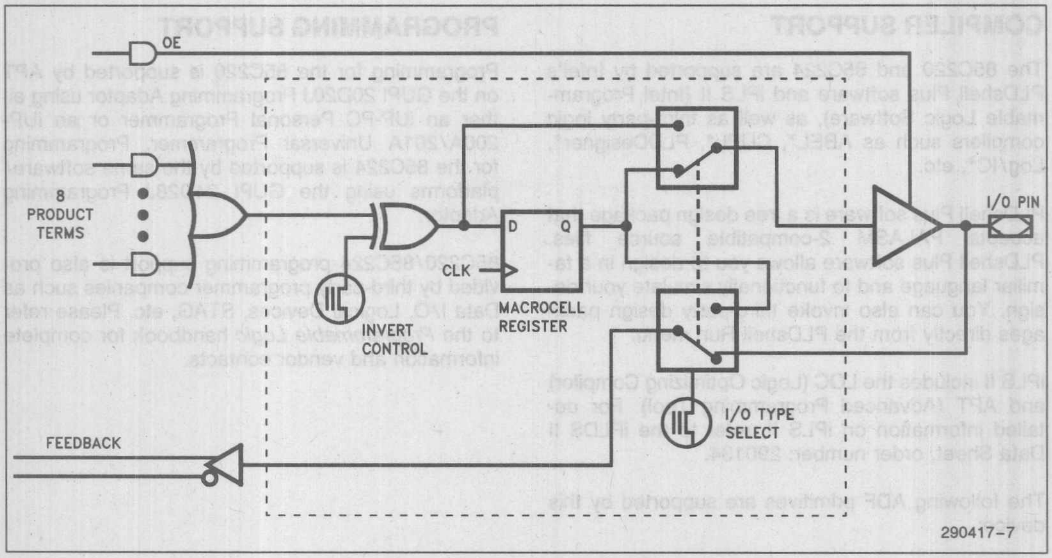


Figure 6. 85C220/85C224 I/O Control Architecture

POWER-ON CHARACTERISTICS

85C220/85C224 inputs and outputs begin responding 1 μs (max.) after V_{CC} power-up (V_{CC} = 4.75V) or after a power-loss/power-up sequence. All macrocells programmed as registers will be set to a logic low.

ERASED STATE CHARACTERISTICS

Prior to programming, the I/O structure is configured for combinatorial active low output with input (pin) feedback.

Intelligent Programming Algorithm

The 85C220/85C224 support the Intelligent Programming Algorithm, which rapidly programs Intel PLDs, and many of Intel's microcontrollers and EPROMs while maintaining a high degree of reliability. It is particularly suited for production programming environments. This method decreases the overall programming time while programming reliability is ensured as the incremental programming margin of each bit has been verified during programming. Programming voltage and waveform specifications are available by request from Intel to support device programming.

LATCH-UP IMMUNITY

All of the input, output, and clock pins of the devices have been designed to resist latch-up which is inherent in inferior CMOS structures. The devices are designed with Intel's proprietary 1-micron CMOS IIIE EPROM process. Thus, each of the pins will not experience latch-up with currents up to ±100 mA and voltages ranging from −0.5V to (V_{CC} + 0.5V). The programming pin is designed to resist latch-up to the 13.5V maximum device limit.

DESIGN RECOMMENDATIONS

For proper operation, it is recommended that all input and output pins be constrained to the voltage range GND ≤ (V_{IN} or V_{OUT}) ≤ V_{CC}*. All unused inputs and I/Os should be tied high or low to minimize power consumption (do not leave them floating). On the 85C224 PLCC Package, the optional power pin (pin 1) and optional ground pins (8, 15, and 22) may be connected to power and ground, respectively, to reduce output switching noise. A high-speed power supply decoupling capacitor of at least 0.2 μF must be connected directly between the V_{CC} and GND pins.

As with all CMOS devices, ESD handling procedures should be used with the devices to prevent damage to the devices during programming, assembly, and test.

*There is no internal pull up register on output pins.

COMPILER SUPPORT

The 85C220 and 85C224 are supported by Intel's PLDshell Plus software and iPLS II (Intel Programmable Logic Software), as well as third-party logic compilers such as ABEL*, CUPL*, PLDDesigner*, Log/IC*, etc.

PLDshell Plus software is a free design package that accepts PALASM 2-compatible source files. PLDshell Plus software allows you to design in a familiar language and to functionally simulate your design. You can also invoke third-party design packages directly from the PLDshell Run menu.

iPLS II includes the LOC (Logic Optimizing Compiler) and APT (Advanced Programming Tool). For detailed information on iPLS II, refer to the iPLDS II Data Sheet, order number: 290134.

The following ADF primitives are supported by this device:

INP	RONF
CONF	RORF
COIF	NORF

PROGRAMMING SUPPORT

Programming for the 85C220 is supported by APT on the GUPI 20D20J Programming Adaptor using either an iUP-PC Personal Programmer or an iUP-200A/201A Universal Programmer. Programming for the 85C224 is supported by the same software/ platforms using the GUPI 24D28J Programming Adaptor.

85C220/85C224 programming support is also provided by third-party programmer companies such as Data I/O, Logical Devices, STAG, etc. Please refer to the *Programmable Logic* handbook for complete information and vendor contacts.

85C220-7 ORDERING INFORMATION

f_{CNT1}	f_{MAX}	t_{PD1}/t_{PD2}	Order Code	Package	Operating Range
74	100	7.5/8.5	N85C220-7 P85C220-7	PLCC PDIP	Commercial
58.8	62.5	10	N85C220-10 P85C220-10	PLCC PDIP	Commercial

85C224-7 ORDERING INFORMATION

f_{CNT1}	f_{MAX}	t_{PD1}/t_{PD2}	Order Code	Package	Operating Range
74	100	7.5/8.5	N85C224-7 P85C224-7	PLCC PDIP	Commercial
58.8	62.5	10	N85C224-10 P85C224-10	PLCC PDIP	Commercial

ABEL is a trademark of Data I/O Corporation.
CUPL is a trademark of Logical Devices, Inc.
Log/IC is a trademark of ISDATA Corporation.
PLDDesigner is a trademark of MINC, Inc.

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage (V_{CC})(1) .... −2.0V to +7.0V

Programming Supply Voltage (V_{PP})(1) .... −2.0V to +13.5V

D.C. Input Voltage (V_I)(1, 2) ... −0.5V to V_{CC} + 0.5V

Storage Temperature (T_{stg}) ..... −65°C to +150°C

Ambient Temperature (T_{amb})(3) ... −10°C to +85°C

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Units
V_{CC}	Supply Voltage	4.75	5.25	V
V_{IN}	Input Voltage	0	V_{CC}	V
V_O	Output Voltage	0	V_{CC}	V
T_A	Operating Temperature	0	+70	°C
t_R	Input Rise Time		500	ns
t_F	Input Fall Time		500	ns

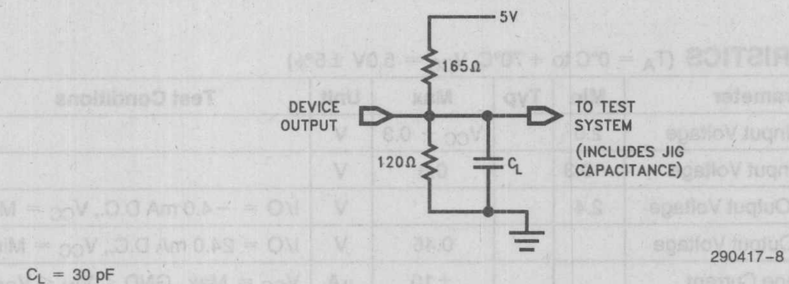
D.C. CHARACTERISTICS (T_A = 0°C to +70°C, V_{CC} = 5.0V ±5%)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}(4)	High Level Input Voltage	2.0		V_{CC} + 0.3	V	
V_{IL}(4)	Low Level Input Voltage	−0.3		0.8	V	
V_{OH}	High Level Output Voltage	2.4			V	I/O = −4.0 mA D.C., V_{CC} = Min.
V_{OL}	Low Level Output Voltage			0.45	V	I/O = 24.0 mA D.C., V_{CC} = Min.
I_I	Input Leakage Current			±10	μA	V_{CC} = Max., GND < V_{IN} < V_{CC}
I_{OZ}	Output Leakage Current			±10	μA	V_{CC} = Max., GND < V_{OUT} < V_{CC}
I_{SC}(5)	Output Short Circuit Current	−30		−120	mA	V_{CC} = Max., V_{OUT} = 0.5V

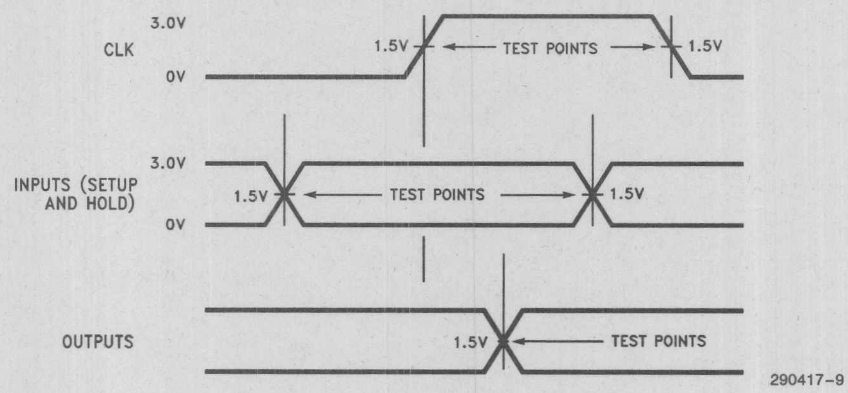
Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
I_{CC}	Power Supply Current (PLCC)		60	90	mA	V_{CC} = Max., V_{IN} = V_{CC} or GND, No Load, f_{IN} = 25 MHz, Device Prog. as 8-Bit Counter
			75	105	mA	f_{IN} = 74 MHz
	Power Supply Current (PDIP)		75	115	mA	V_{CC} = Max., V_{IN} = V_{CC} or GND, No Load, f_{IN} = 25 MHz, Device Prog. as 8-Bit Counter
			94	135	mA	f_{IN} = 74 MHz

NOTES:
1. Voltages with respect to GND.
2. Minimum D.C. input is −0.5V. During transitions, the inputs may undershoot to −2.0V or overshoot to +7.0V for periods of less than 20 ns under no load conditions.
3. Under bias.
4. Absolute values with respect to device GND; all over and undershoots due to system or tester noise are included.
5. Not more than 1 output should be tested at a time. Duration of that test should not exceed 1 second.

A.C. TESTING LOAD CIRCUIT



A.C. TESTING WAVEFORM—SYNCHRONOUS INPUTS AND OUTPUTS



A.C. Testing: Inputs (including CLK) are driven at 3.0V for a Logic "1" and 0V for a Logic "0". Setup and hold input measurements relative to CLK are made at 1.5V on CLK (low-to-high transition). Input and Output transitions are measured at 1.5V. Device input rise and fall times are less than 3 ns.

CAPACITANCE (T_A = 0°C to +70°C; V_{CC} = 5.0V ±5%)(6)

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
C_{IN}	Input Capacitance		4	6	pF	V_{IN} = 0V, f = 1.0 MHz
C_{IO}	I/O Capacitance		5	8	pF	V_{OUT} = 0V, f = 1.0 MHz
C_{CLK}	CLK Capacitance		6	8	pF	V_{OUT} = 0V, f = 1.0 MHz
C_{VPP}	V_{PP} Pin Capacitance		8	10	pF	V_{PP} on Pin 11/13, f = 1.0 MHz

NOTE:
6. These values are evaluated during initial characterization and whenever design modifications occur that may affect capacitance.

A.C. CHARACTERISTICS (T_A = 0°C to +70°C, V_{CC} = 5.0V ±5%)(7)

Symbol	Parameter	85C220-7/85C224-7			85C220-10/85C224-10			Units
		Min	Typ	Max	Min	Typ	Max	
t_{PD1}(8)	Input or I/O to Output Valid, Invert On	3		7.5	3		10	ns
t_{PD2}(8)	Input or I/O to Output Valid, Invert Off	3		8.5	3		10	ns
t_{PZX}(9)	Input or I/O to Output Enable	3		9	3		10	ns
t_{PXZ}(9)	Input or I/O to Output Disable	3		9	3		10	ns
t_{OS}	Register Output Mode Output Pin to Output Pin Skew	150	250	300	150	250	300	ps
t_{OS}	Combinatorial Mode Output to Output Pin Skew	150	300	400	150	300	400	ps

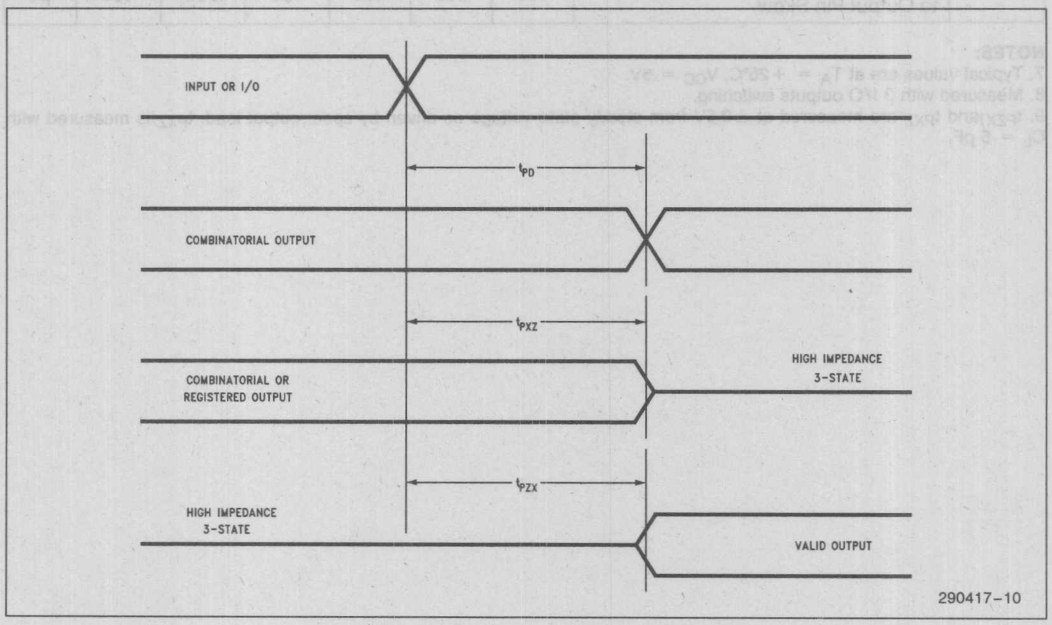
NOTES:
7. Typical values are at T_A = +25°C, V_{CC} = 5V.
8. Measured with 3 I/O outputs switching.
9. t_{PZX} and t_{PXZ} are measured at ±0.5V from steady state voltage as driven by spec. output load. t_{PXZ} is measured with C_L = 5 pF.

2

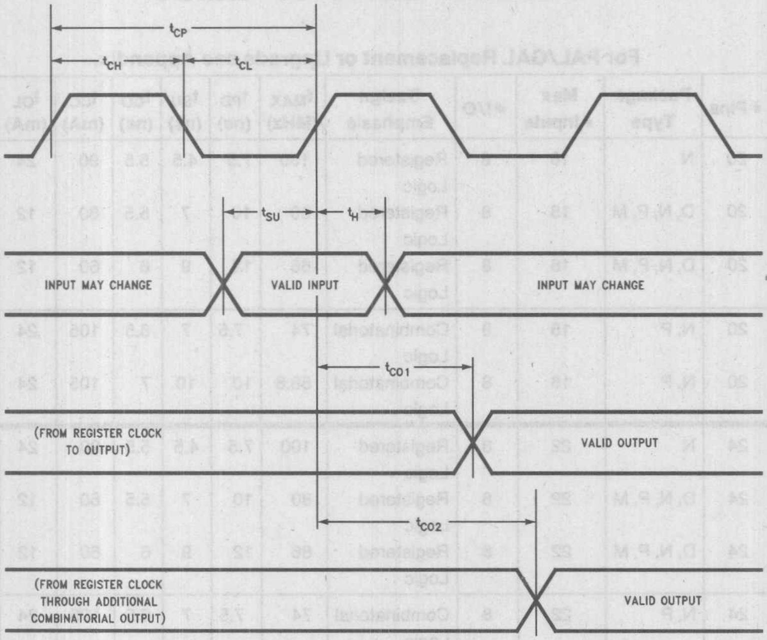
SYNCHRONOUS CLOCK MODE ($T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 5\%$)(7)

Symbol	Parameter	85C220-7/85C224-7			85C220-10/85C224-10			Units
		Min	Typ	Max	Min	Typ	Max	
f_{CNT1}(8)	Max. Counter Frequency, $1/(t_{SU} + t_C)$—External Feedback		90	74		74	58.8	MHz
f_{CNT2}(8)	Max. Counter Frequency, $1/t_{CNT}$—Internal Feedback		110	100		80	60.6	MHz
f_{MAX}(8)	Max. Frequency, $1/t_{CP}$—No Feedback (Pipelined)		110	100		80	62.5	MHz
t_{SU}	Input or I/O Setup Time to CLK	7			10			ns
t_H	Input or I/O Hold Time from CLK	0			0			ns
t_{CO1}(8)	CLK High to Output Valid	3		6.5	3		7	ns
t_{CO2}	CLK High to Output Valid Fed through Combinatorial Macrocell	4.5		11	4.5		13	ns
t_{CNT}(8)	Macrocell Output Feedback to Macrocell Input—Internal Path	10			16.5			ns
t_{CL}	CLK Low Time	4			7			ns
t_{CH}	CLK High Time	4			7			ns
t_{CP}	CLK Period	10			16			ns

COMBINATORIAL MODE

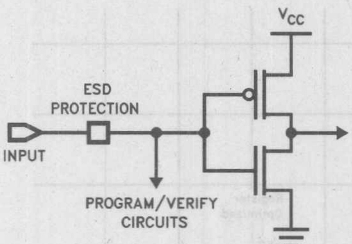


REGISTERED MODE

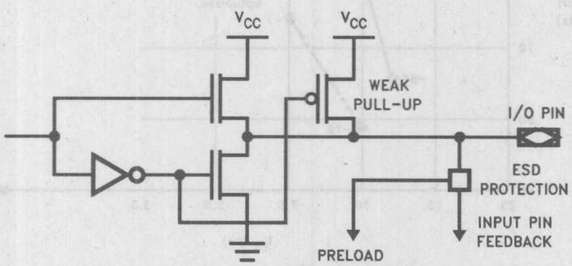


290417-11

INPUT AND OUTPUT EQUIVALENT SCHEMATICS



290417-12



290417-13

85C220/85C224 Family Product Selector Guide

For PAL/GAL Replacement or Upgrade see Appendix.

Device	#Pins	Package Type	Max #Inputs	#I/O	Design Emphasis	f_{MAX} (MHz)	t_{PD} (ns)	t_{SU} (ns)	t_{CO} (ns)	I_{CC} (mA)	I_{OL} (mA)	Standby Mode	T_{OS} PS
85C220-100	20	N	18	8	Registered Logic	100	7.5	4.5	5.5	90	24	No	
85C220-80	20	D, N, P, M	18	8	Registered Logic	80	10	7	5.5	60	12	Yes	
85C220-66	20	D, N, P, M	18	8	Registered Logic	66	12	9	6	60	12	Yes	
85C220-7	20	N, P	18	8	Combinatorial Logic	74	7.5	7	6.5	105	24	No	
85C220-10	20	N, P	18	8	Combinatorial Logic	58.8	10	10	7	105	24	No	
85C224-100	24	N	22	8	Registered Logic	100	7.5	4.5	5.5	90	24	No	<400
85C224-80	24	D, N, P, M	22	8	Registered Logic	80	10	7	5.5	60	12	Yes	
85C224-66	24	D, N, P, M	22	8	Registered Logic	66	12	9	6	60	12	Yes	
85C224-7	24	N, P	22	8	Combinatorial Logic	74	7.5	7	6.5	105	24	No	
85C224-10	24	N, P	22	8	Combinatorial Logic	58.8	10	10	7	105	24	No	<400

D = Ceramic, DIP, N = PLCC, P = Plastic DIP, M = Military Package.

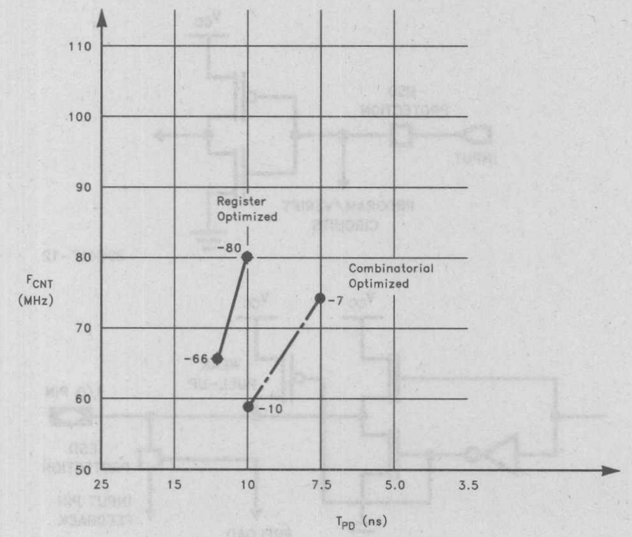


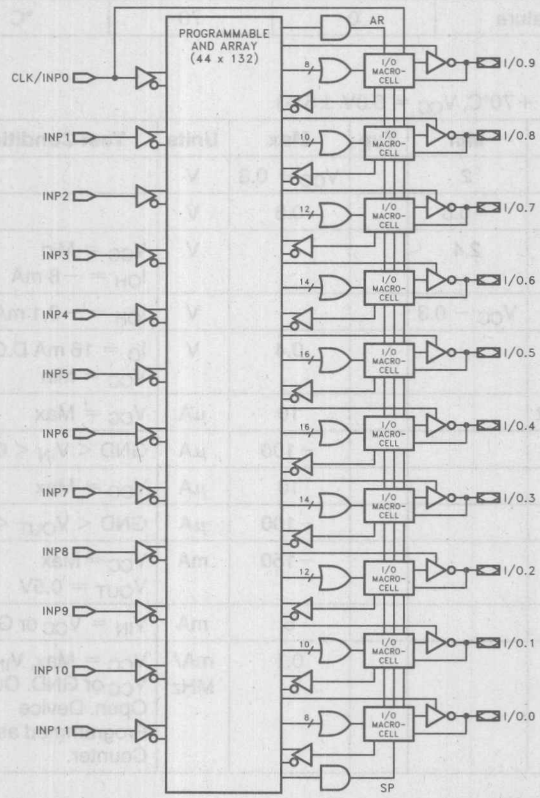
FIGURE 1. 85C220/85C224 Family Speed Bin Comparison

September 1993
Order Number: 297002-003

iPLD22V10L-5
LOW POWER, ELECTRICALLY ERASABLE 10-MACROCELL CMOS PLD

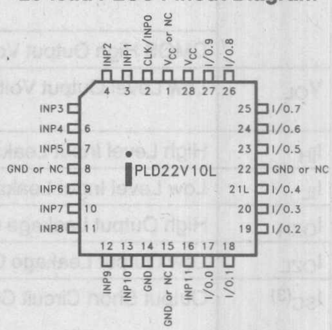
- **Low Power, High Speed Upgrade to BiCMOS/Bipolar 22V10 and CMOS Equivalents**
- **Supply Voltage Range 4.75V to 5.25V**
- **t_{PD} 5 ns, 142 MHz with Feedback**
- **Maximum I_{SB} = 5 mA**
- **Typical I_{CC} = 15 mA @100 MHz**
- **12 Dedicated Inputs and 10 I/O Pins**
- **10 Macrocells with Programmable I/O Architecture (Registered/Combinatorial)**
- **Sub-micron CHMOS III Electrical Erasable Technology**
- **Programmable "Security Bit" Allows Total Protection of Proprietary Designs**
- **100% Generically Tested Logic Array**
- **Available in 28-Pin PLCC Packages**

iPLD22V10 Global Architecture



290503-2

28-lead PLCC Pinout Diagram



290503-1

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage (V_{CC})(1) .... −1.0 to +5.25V
Programming Supply Voltage (V_{PP})(1) .... −1.0V to +8.0V
DC Input Voltage (V_I)(1, 2) .... −0.5V to V_{CC} + 0.5V
Storage Temperature (T_{STG}) .... −65°C to +150°C

NOTICE: This data sheet contains information on products in the sampling and initial production phases of development. The specifications are subject to change without notice. Verify with your local Intel Sales office that you have the latest data sheet before finalizing a design.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Units
V_{CC}	Supply Voltage	4.75	5.25	V
V_{IN}	Input Voltage	0	V_{CC}	V
V_O	Output Voltage	0	V_{CC}	V
T_A	Operating Temperature	0	70	°C

D.C. CHARACTERISTIC (T_A = 0°C to +70°C, V_{CC} = 5.0V ±5%)

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
V_{IH}(1)	High Level Input Voltage	2		V_{CC} + 0.3	V	
V_{IL}(1)	Low Level Input Voltage	−0.5		0.8	V	
V_{OH}	TTL High Output Voltage	2.4			V	V_{CC} = Min I_{OH} = −8 mA
	CMOS High Output Voltage	V_{CC} − 0.3			V	I_{OH} = −0.1 mA
V_{OL}	Low Level Output Voltage			0.4	V	I_O = 16 mA D.C. V_{CC} = Min
I_{IH}	High Level Input Leakage Current			10	μA	V_{CC} = Max
I_{IL}	Low Level Input Leakage Current			−100	μA	GND < V_{IN} < 0.8V
I_{OZH}	High Output Leakage Current			10	μA	V_{CC} = Max
I_{OZL}	Low Output Leakage Current			−100	μA	GND < V_{OUT} < 0.8V
I_{SC}(3)	Output Short Circuit Current			−150	mA	V_{CC} = Max V_{OUT} = 0.5V
I_{SB}	Standby Power Supply Current			5	mA	V_{IN} = V_{CC} or GND
I_{CC} Active	Power Supply Current			0.1	mA/MHz	V_{CC} = Max, V_{IN} = V_{CC} or GND. Outputs Open. Device Programmed as 8-Bit Counter.

NOTES:
1. Voltages with respect to GND
2. Minimum D.C. input is −0.5V. During transitions, the Inputs may undershoot to −2.0V or overshoot to +7.0V for periods of less than 20 ns under no load conditions.
3. Not more than 1 output should be tested at a time. Duration of that test should not exceed 1 second.

COMBINATORIAL MODE A.C. CHARACTERISTICS

$T_A = 0°C$ to $+70°C$, $V_{CC} = 5.0 \pm 5\%^{(4)}$

Symbol	Parameter	iPLD22V10 5			Units
		Min	Typ	Max	
$t_{PD}^{(5)}$	Input or I/O to Output Valid	2		5	ns
$t_{PZX}^{(6)}$	Input or I/O to Output Enable	2		6	ns
$t_{PXZ}^{(6)}$	Input or I/O to Output Disable	2		5	ns
t_{CLR}	Input or I/O to Asynchronous Reset	2		6	ns

NOTES:
4. Typical values are at $T_A = +25°C$, $V_{CC} = 5.25V$.
5. Refer to switching test conditions.
6. t_{PZX} and t_{PXZ} are measured at ±0.5V from steady state voltage as driven by specified output load. t_{PXZ} is measured with $C_L = 5$ pF. Z → H and Z → L are measured at 1.5V on output.

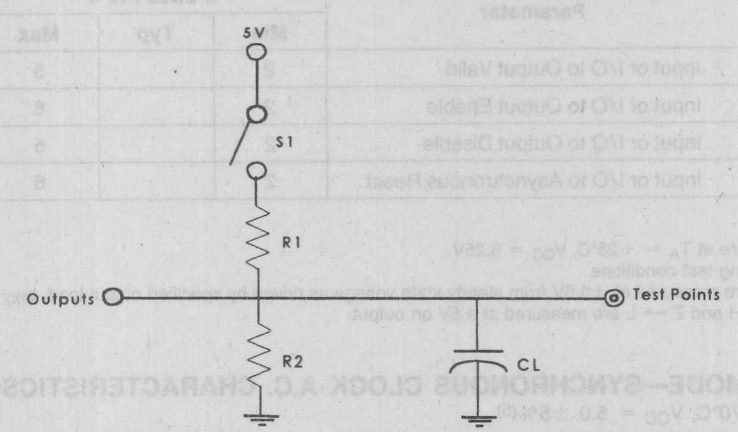
2

REGISTER MODE—SYNCHRONOUS CLOCK A.C. CHARACTERISTICS

$T_A = 0°C$ to $+70°C$, $V_{CC} = 5.0 \pm 5\%^{(5)}$

Symbol	Parameter	iPLD22V10 5			Units
		Min	Typ	Max	
$f_{CNT}^{(6)}$	Maximum Counter Frequency $1/(t_{SU} + t_{CO})$—External Feedback	142			MHz
$f_{CNT}^{(6)}$	Maximum Counter Frequency $1/(t_{CNT})$—Internal Feedback	166			MHz
$f_{MAX}^{(6)}$	Maximum Frequency (Pipelined) $1/t_{CP}$—No Feedback	166			MHz
t_{SU}	Input or I/O Setup Time to CLK	3.5			ns
t_H	Input or I/O Hold Time from CLK	0			ns
t_{CO1}	CLK to Output Valid	1.5		3.5	ns
t_{CO2}	CLK to Output Valid Fed Through Combinatorial Macrocell	4		8	ns
t_{CNT}	Register Output Feedback to Register Input—Internal Path			6	ns
t_{CL}	CLK Low Time	3			ns
t_{CH}	CLK High Time	3			ns
t_{CP}	CLK Period	6			ns

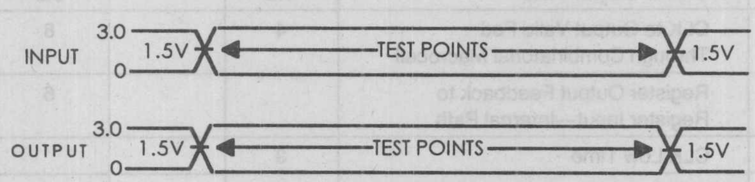
A.C. TESTING LOAD CIRUIT



290503-3

Specifications	S1	C_L	Commercial R1	Commercial R2	Measured Output Value
t_{PD}, t_{CO}	Closed	50 pF	230Ω	260Ω	1.5V
t_{PZX}	Z → H:Open Z → L:Closed				1.5V
t_{PXZ}	H → Z:Open L → Z:Closed	5 pF			H → Z:V_{OH} − 0.5V L → Z:V_{OL} + 0.5V

A.C. TESTING INPUT, OUTPUT WAVEFORM



290503-4

NOTE:
AC Testing: Inputs are driven at 3.0V for a logic "1" and 0V for a logic "0". Timing measurements are made at 1.5V on inputs and outputs. Device input rise and fall times <2 ns.

CAPACITANCE (T_A = 0°C to 70°C; V_{CC} = 5.0V ±5%)(6)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
C_{IN}	Input Capacitance		5	8	pF	V_{IN} = 0V, f = 1.0 MHz
C_{IO}	I/O Capacitance		6	8	pF	V_{OUT} = 0V, f = 1.0 MHz
C_{CLK}	CLK Capacitance		15	17	pF	V_{OUT} = 0V, f = 1.0 MHz

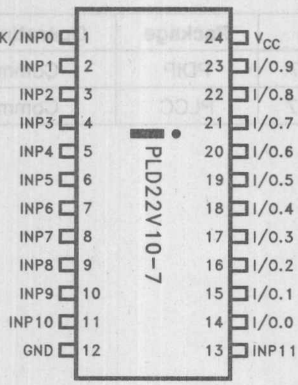
NOTE:
7. These values are evaluated at initial characterization and whenever design modifications occur that may affect capacitance.

iPLD22V10-7
HIGH PERFORMANCE 10-MACROCELL CMOS PLD

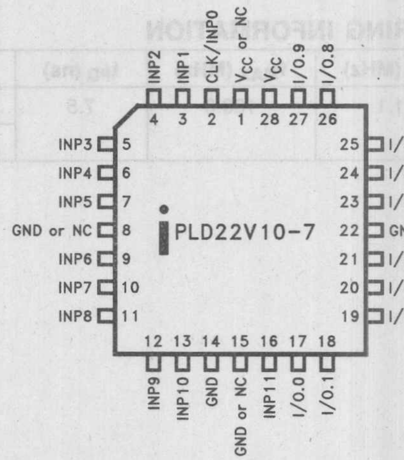
High-Speed Upgrade to Bipolar 22V10 and CMOS Equivalents

- t_{PD} 7.5 ns, 111.1 MHz with Feedback, 111.1 MHz with No Feedback
- Typical I_{CC} = 90 mA @ 15 MHz
- 12 Dedicated Inputs and 10 I/O Pins
- 10 Macrocells with Programmable I/O Architecture (Register/Combinatorial)
- Variable P-terms—Up to 16 per Macrocell, Selectable Output Polarity, Separate Output Enable P-term
- Global Asynchronous Clear and Synchronous Preset P-terms
- 1-Micron CHMOS IIIE EPROM Technology
- Programmable "Security Bit" Allows Total Protection of Proprietary Designs
- 100% Generically Tested Logic Array
- Available in 300-mil 24-Pin PDIP and 28-Pin PLCC Packages
  (See Packaging Spec., Order Number 240800, Package Type N and P)

2



290485–1



290485–2

Figure 1. Pinout Diagrams

Log/IC is a trademark of ISDATA, Inc.

October 1993
Order Number: 290485-001

INTRODUCTION

The iPLD22V10-7 is a high-performance, high-integration, general-purpose CMOS PLD. The iPLD22V10-7 accommodates logic functions with up to 22 inputs and 10 I/O macrocells. I/O macrocells include an average of 12 p-terms for input, with a separate p-term for output enable. Figure 2 shows the global architecture of the device.

JEDEC AND PIN COMPATIBILITY

The iPLD22V10-7 is 100% JEDEC-, pin- and function- compatible with the industry-standard 22V10 PLD. JEDEC files developed for 22V10 devices can be used to program the iPLD22V10-7. When the N PLD22V10 (28-pin PLCC) is used to replace a conventional 22V10 in an existing design socket, pins 8, 15, 22 and 1 are left as No Connects (NC). New designs can take advantage of the additional device V_{CC} and grounds these pins offer.

PROGRAMMABLE MACROCELLS

In addition to the 12 dedicated input pins, the iPLD22V10-7 contains 10 programmable macrocells. Each of the macrocells can be programmed to function as an input or as a combinatorial or registered output. Programmable output polarity and programmable feedback options allow the iPLD22V10-7 to be tailored to the precise needs of the target application. Figure 3 shows the architecture of each macrocell.

Output Polarity

The output polarity for each iPLD22V10-7 macrocell is programmable. Each combinatorial or registered output can be active-high or active-low.

Feedback Options

iPLD22V10-7 macrocells programmed as combinatorial outputs support pin feedback to the logic array (i.e., feedback from the I/O pin). iPLD22V10-7 macrocells programmed as registers allow internal register feedback to the logic array.

ORDERING INFORMATION

f_{CNT1} (MHz)	f_{MAX} (MHz)	t_{PD} (ns)	Order Code	Package	Operating Range
111.1	109.8	7.5	P PLD22V10-7	PDIP	Commercial
			N PLD22V10-7	PLCC	Commercial

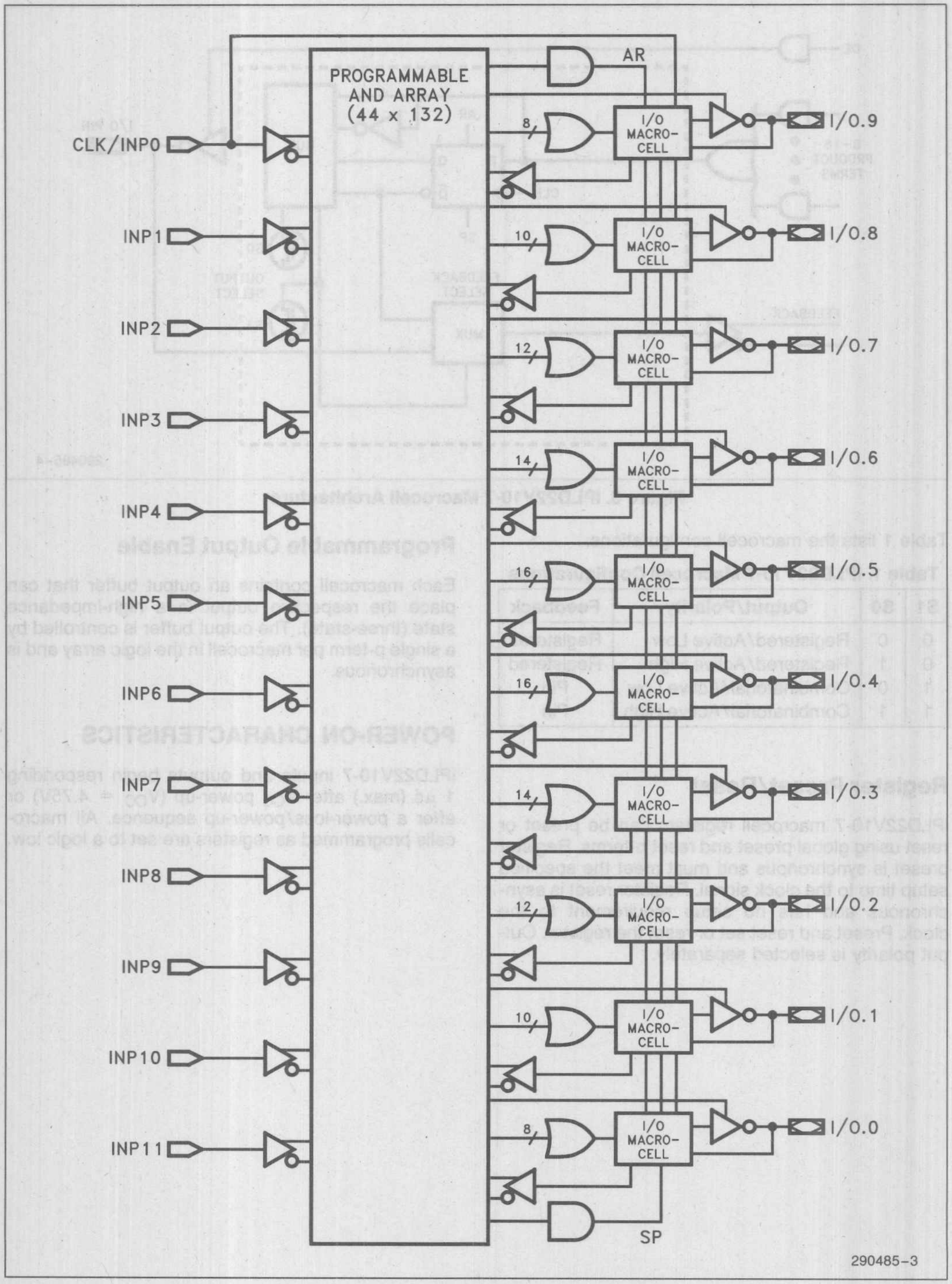


Figure 2. iPLD22V10-7 Global Architecture

2

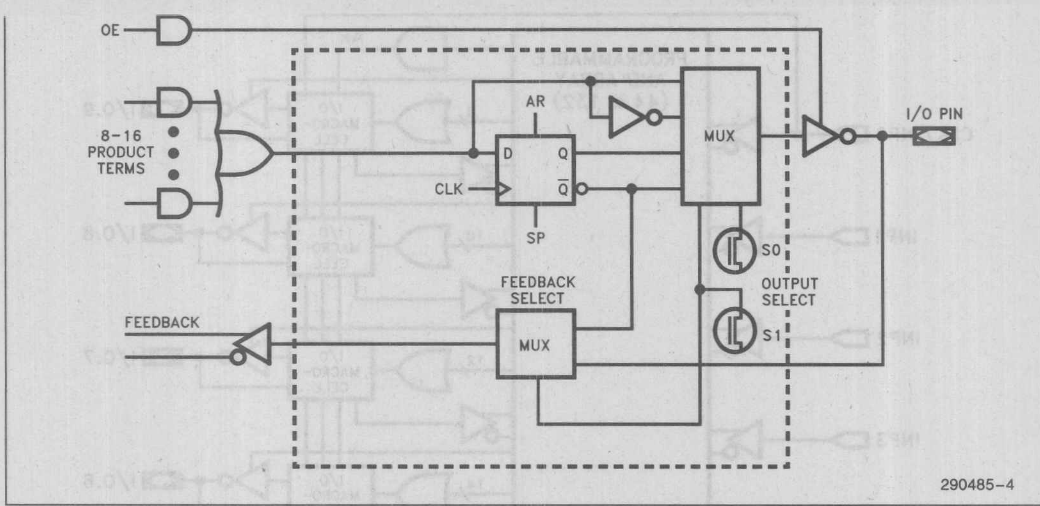


Figure 3. iPLD22V10-7 Macrocell Architecture

Table 1 lists the macrocell configurations:

Table 1. iPLD22V10-7 Macrocell Configurations

S1	S0	Output/Polarity	Feedback
0	0	Registered/Active Low	Registered
0	1	Registered/Active High	Registered
1	0	Combinatorial/Active Low	Pin
1	1	Combinatorial/Active High	Pin

Register Preset/Reset

iPLD22V10-7 macrocell registers can be preset or reset using global preset and reset p-terms. Register preset is synchronous and must meet the specified setup time to the clock signal. Register reset is asynchronous and has no setup requirement to the clock. Preset and reset set or reset the register. Output polarity is selected separately.

Programmable Output Enable

Each macrocell contains an output buffer that can place the respective output in a high-impedance state (three-state). The output buffer is controlled by a single p-term per macrocell in the logic array and is asynchronous.

POWER-ON CHARACTERISTICS

iPLD22V10-7 inputs and outputs begin responding 1 μs (max.) after V_{CC} power-up (V_{CC} = 4.75V) or after a power-loss/power-up sequence. All macrocells programmed as registers are set to a logic low.

PROGRAMMING CHARACTERISTICS

Prior to programming, all EPROM logic array cells are in the "connected" state. The macrocells by default are configured for registered output, active-low operation with registered feedback.

Intelligent Programming Alogrithm

The iPLD22V10-7 supports the Intelligent Programming Algorithm, a fast, reliable algorithm for programming many types of Intel programmable devices.

PROCESS TECHNOLOGY

The iPLD22V10-7 is fabricated on Intel's CHMOS EPROM process. Over 20 million devices (including EPROMs and Microcontrollers) have been fabricated on this process.

TESTABILITY

The iPLD22V10-7 is completely tested at the factory. Unlike fuse-based PLDs, which have one-time programmable fuse links that limit testing to small-scale sampling, each EPROM cell in the iPLD22V10-7 is tested and erased prior to shipment.

SECURITY

A single programmable bit, called the security bit or verify protect bit, controls access to the data programmed into the device. Once this security bit is set, the design cannot be copied.

Since data in the device is stored in EPROM cells, the contents of the device cannot be read even with microscopic examination, providing an additional level of design security not available with fuse-based devices.

DEVELOPMENT SOFTWARE

Third Party Support

The iPLD22V10-7 is supported by third-party logic compilers such as ABEL*, CUPL*, PLDesigner*, Log/IC, etc. Programming support is provided by third-party programmer companies such as Data I/O, Logical Devices, STAG, etc. Please refer to the "Third-Party Support" lists in the *Programmable Logic* handbook for complete information and vendor contacts.

PLDshell PLUS

Full logic compilation and functional simulation for the iPLD22V10-7 is supported by PLDshell Plus software.

PLDshell Plus design software is Intel's new, user-friendly design tool for PLD design. PLDshell Plus allows users to incorporate their preferred text editor, programming software, and additional design tools into a easy-to-use, menued design environment that includes Intel's PLDasm logic compiler and simulation software along with disassembly, conversion, and translation utilities. The PLDasm compiler and simulator software accepts industry-standard PDS source files that express designs as Boolean equations, truth tables, or state machines. On-line help, datasheet briefs, technical notes, and error message information, along with waveform viewing/printing capability make the design task as easy as possible. PLDshell Plus software is available from Intel Literature channels or from your local Intel sales representative.

*ABEL is a trademark of Data I/O Corp. CUPL is a trademark of Logical Devices, Inc. PLDesigner is a trademark of MINC, Inc. Log/IC is a trademark of ISDATA, Corporation.

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage (V_{CC})(1) .... −2.0V to +7.0V

Programming Supply Voltage (V_{PP})(1) .... −2.0V to +13.5V

D.C. Input Voltage (V_I)(1, 2) ... −0.5V to V_{CC} + 0.5V

Storage Temperature (T_{stg}) ..... −65°C to +150°C

Ambient Temperature (T_A)(3) ..... −10°C to +85°C

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

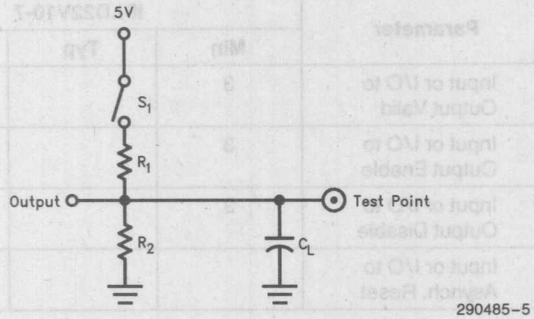
Symbol	Parameter	Min	Max	Units
V_{CC}	Supply Voltage	4.75	5.25	V
V_{IN}	Input Voltage	0	V_{CC}	V
V_O	Output Voltage	0	V_{CC}	V
T_A	Operating Temperature	0	+70	°C

D.C. CHARACTERISTICS (T_A = 0°C to +70°C, V_{CC} = 5.0V +5%)

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
V_{IH}(4)	High Level Input Voltage	2.0		V_{CC} + 0.3	V	
V_{IL}(4)	Low Level Input Voltage	−0.3		0.8	V	
V_{OH}	TTL High Output Voltage	2.4			V	I_O = −4 mA D.C., V_{CC} = Min
	CMOS High Output Voltage	V_{CC} − 0.3			V	I_O = −100 pH = V_{CC} Min
V_{OL}	Low Level Output Voltage			0.45	V	I_O = 16 mA D.C., V_{CC} = Min
I_I	Input Leakage Current			10	μA	V_{CC} = Max., GND < V_{IN} < V_{CC}
I_{OZ}	Output Leakage Current			10	μA	V_{CC} = Max., GND < V_{OUT} < V_{CC}
I_{SC}(5)	Output Short Circuit Current			120	mA	V_{CC} = Max., V_{OUT} = 0.5V
I_{CC}	Power Supply Current (See I_{CC} vs. Freq. Graph)		90	130	mA	V_{CC} = Max., V_{IN} = V_{CC} or GND, No Load, f_{IN} = 15 MHz, Device Prog. as a 10-Bit Counter

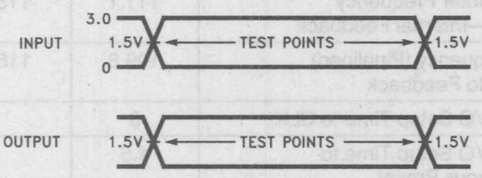
NOTES:
1. Voltages with respect to GND.
2. Minimum D.C. input is −0.5V. During transitions, the inputs may undershoot to −2.0V or overshoot to +7.0V for periods of less than 20 ns under no load conditions.
3. Under bias. Extended Temperature versions are also available.
4. Absolute values with respect to device GND; all over and undershoots due to system or tester noise are included.
5. Not more than 1 output should be tested at a time. Duration of that test should not exceed 1 second.

A.C. TESTING LOAD CIRCUIT



Specification	S_1	C_L	Commercial R_1	Commercial R_2	Measured Output Value
t_{PD}, t_{CO}	Closed	50 pF	240Ω	160Ω	1.5V
t_{PZX}	Z → H: Open Z → L: Closed				1.5V
t_{PXZ}	H → Z: Open L → Z: Closed	5 pF			H → Z: $V_{OH} - 0.5V$ L → Z: $V_{OL} + 0.5V$

A.C. TESTING INPUT, OUTPUT WAVEFORM



A.C. Testing: Inputs are Driven at 3.0V for a Logic "1" and 0V for a Logic "0". Timing Measurements are made at 1.5V. Outputs are measured at 1.5V. Device input rise and fall times < 3 ns.

CAPACITANCE (T_A = 0°C to 70°C; V_{CC} = 5.0V ±5%)(6)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
C_{IN}	Input Capacitance		5	8	pF	V_{IN} = 0V, f = 1.0 MHz
C_{IO}	I/O Capacitance		6	8	pF	V_{OUT} = 0V, f = 1.0 MHz
C_{CLK}	CLK Capacitance		8	10	pF	V_{OUT} = 0V, f = 1.0 MHz

COMBINATORIAL MODE A.C. CHARACTERISTICS

(T_A = 0°C to +70°C, V_{CC} = 5.0V ±5%)(7)

Symbol	Parameter	iPLD22V10-7			Units
		Min	Typ	Max	
t_{PD}(8)	Input or I/O to Output Valid	3		7.5	ns
t_{PZX}(9)	Input or I/O to Output Enable	3		9	ns
t_{PXZ}(9)	Input or I/O to Output Disable	3		9	ns
t_{CLR}	Input or I/O to Asynch. Reset			10	ns

NOTES:

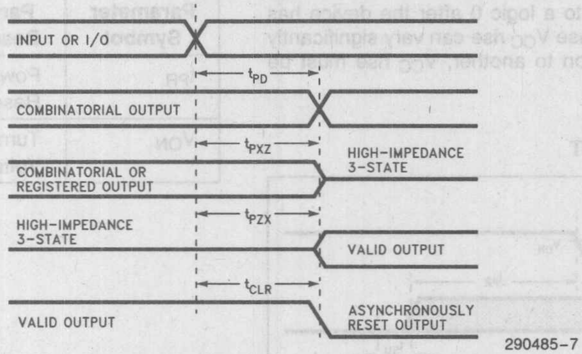
6. These values are evaluated at initial characterization and whenever design modifications occur that may affect capacitance.
7. Typical values are at T_A = +25°C, V_{CC} = 5V.
8. Refer to switching test conditions.
9. t_{PZX} and t_{PXZ} are measured at ±0.5V from steady state voltage as driven by spec. output load. t_{PXZ} is measured with C_L = 5 pF. Z → H and Z → L are measured at 1.5V on output.

REGISTER MODE—SYNCHRONOUS CLOCK A.C. CHARACTERISTICS

(T_A = 0°C to +70°C, V_{CC} = 5.0V ±5%)(7)

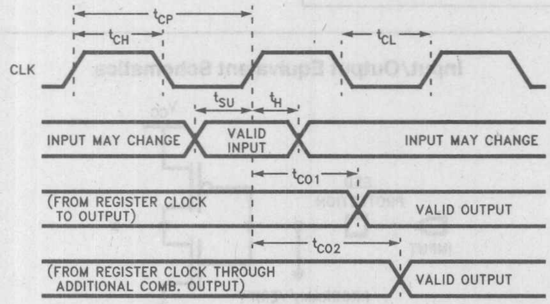
Symbol	Parameter	iPLD22V10-7			Units
		Min	Typ	Max	
f_{CNT1}(8)	Max. Counter Frequency 1/(t_{SU} + t_{CO})—External Feedback	111.1	115		MHz
f_{CNT2}(8)	Max. Counter Frequency 1/(t_{CNT})—Internal Feedback	111.1	115		MHz
f_{MAX}	Max. Frequency (Pipelined) 1/t_{CP}—No Feedback	109.8	115		MHz
t_{SU}	Input or I/O Setup Time to CLK	3			ns
t_{SP}	Input or I/O Setup Time to Synchronous Preset	4.5			ns
t_H	Input or I/O Hold Time from CLK	0			ns
t_{CO1}	CLK to Output Valid	3		6	ns
t_{CO2}	CLK to Output Valid Fed Through Combinatorial Macrocell			13	ns
t_{CNT}	Register Output Feedback to Register Input—Internal Path			13	ns
t_{CL}	CLK Low Time	4			ns
t_{CH}	CLK High Time	4			ns
t_{CP}	CLK Period	9.1			ns
t_{arw}	Asynchronous Reset Pulse Duration	4			ns
t_{arr}	Asynchronous Reset to CLK ↑ Recovery Time	7			ns

COMBINATORIAL MODE



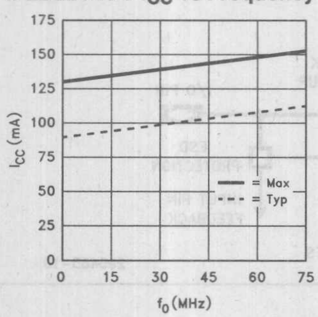
290485-7

SYNCHRONOUS REGISTERED MODE



290485-8

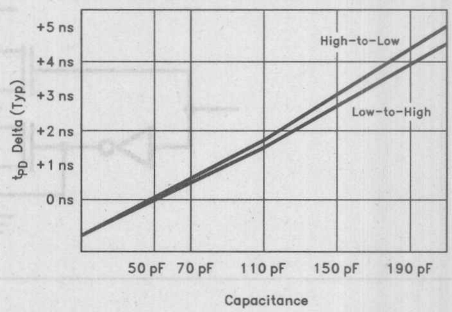
iPLD22V10-7 I_{CC} vs Frequency



Conditions:
$T_A = 0°$
$V_{CC} = 5.25V$

290485-9

t_{PD} Derating vs Capacitive Loading



Conditions:
$T_A = 70°C$
$V_{CC} = 4.75V$

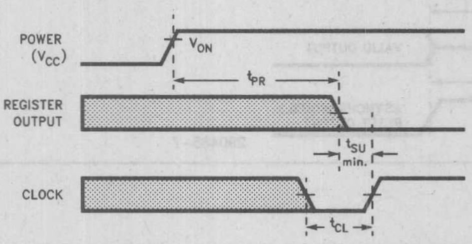
290485-10

2

POWER-UP RESET

Internal power-up reset circuits ensure that all flip-flops will be reset to a logic 0 after the device has powered up. Because V_{CC} rise can vary significantly from one application to another, V_{CC} rise must be monotonic.

POWER-UP RESET

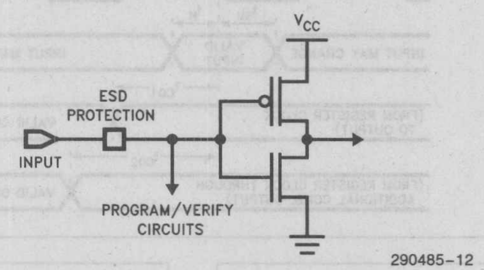


290485-11

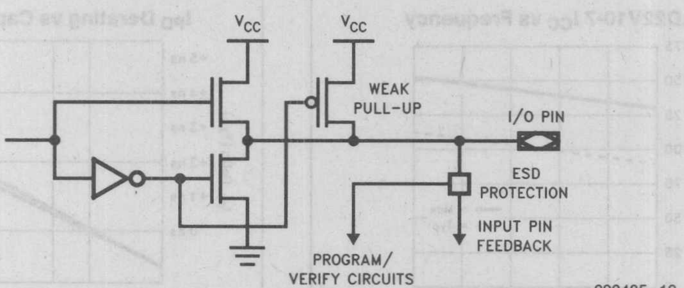
POWER-UP RESET CHARACTERISTICS

Parameter Symbol	Parameter Description	Value
t_{PR}	Power-Up Reset Time	1000 ns Max.
V_{ON}	Turn-On Voltage	4.75V

Input/Output Equivalent Schematics



290485-12

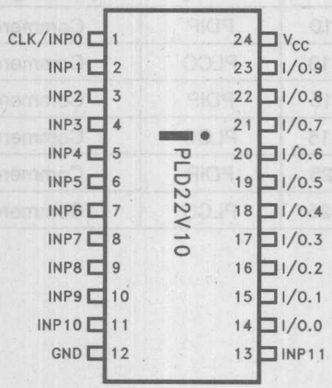


290485-13

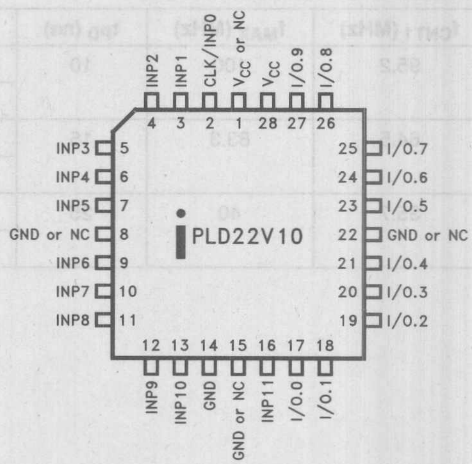
HIGH PERFORMANCE 10-MACROCELL CMOS PLD

High-Speed Upgrade to Bipolar 22V10 and CMOS Equivalents

- t_{PD} 10 ns, 95.2 MHz with Feedback, 100 MHz with No Feedback
- Typical I_{CC} = 90 mA @ 15 MHz
- 12 Dedicated Inputs and 10 I/O Pins
- 10 Macrocells with Programmable I/O Architecture (Register/Combinatorial)
- Variable P-terms—Up to 16 per Macrocell, Selectable Output Polarity, Separate Output Enable P-term
- Global Asynchronous Clear and Synchronous Preset P-terms
- 1-Micron CHMOS IIIE EPROM Technology
- Programmable "Security Bit" Allows Total Protection of Proprietary Designs
- 100% Generically Tested Logic Array
- Available in 300-mil 24-Pin PDIP and 28-Pin PLCC Packages
  (See Packaging Spec., Order Number 240800, Package Type N and P)



290457–1



290457–2

Figure 1. Pinout Diagrams

Log/IC is a trademark of ISDATA, Inc.

October 1993
Order Number: 290457-003

INTRODUCTION

The iPLD22V10 is a high-performance, high-integration, general-purpose CMOS PLD. The iPLD22V10 accommodates logic functions with up to 22 inputs and 10 I/O macrocells. I/O macrocells include an average of 12 p-terms for input, with a separate p-term for output enable. Figure 2 shows the global architecture of the device.

JEDEC AND PIN COMPATIBILITY

The iPLD22V10 is 100% JEDEC-, pin- and function-compatible with the industry-standard 22V10 PLD. JEDEC files developed for 22V10 devices can be used to program the iPLD22V10. When the N PLD22V10 (28-pin PLCC) is used to replace a conventional 22V10 in an existing design socket, pins 8, 15, 22 and 1 are left as No Connects (NC). New designs can take advantage of the additional device V_{CC} and grounds these pins offer.

PROGRAMMABLE MACROCELLS

In addition to the 12 dedicated input pins, the iPLD22V10 contains 10 programmable macrocells. Each of the macrocells can be programmed to function as an input or as a combinatorial or registered output. Programmable output polarity and programmable feedback options allow the iPLD22V10 to be tailored to the precise needs of the target application. Figure 3 shows the architecture of each macrocell.

Output Polarity

The output polarity for each iPLD22V10 macrocell is programmable. Each combinatorial or registered output can be active-high or active-low.

Feedback Options

iPLD22V10 macrocells programmed as combinatorial outputs support pin feedback to the logic array (i.e., feedback from the I/O pin). iPLD22V10 macrocells programmed as registers allow internal register feedback to the logic array.

ORDERING INFORMATION

f_{CNT1} (MHz)	f_{MAX} (MHz)	t_{PD} (ns)	Order Code	Package	Operating Range
95.2	100	10	P PLD22V10-10	PDIP	Commercial
			N PLD22V10-10	PLCC	Commercial
64.5	83.3	15	P PLD22V10-15	PDIP	Commercial
			N PLD22V10-15	PLCC	Commercial
35.7	40	25	P PLD22V10-25	PDIP	Commercial
			N PLD22V10-25	PLCC	Commercial

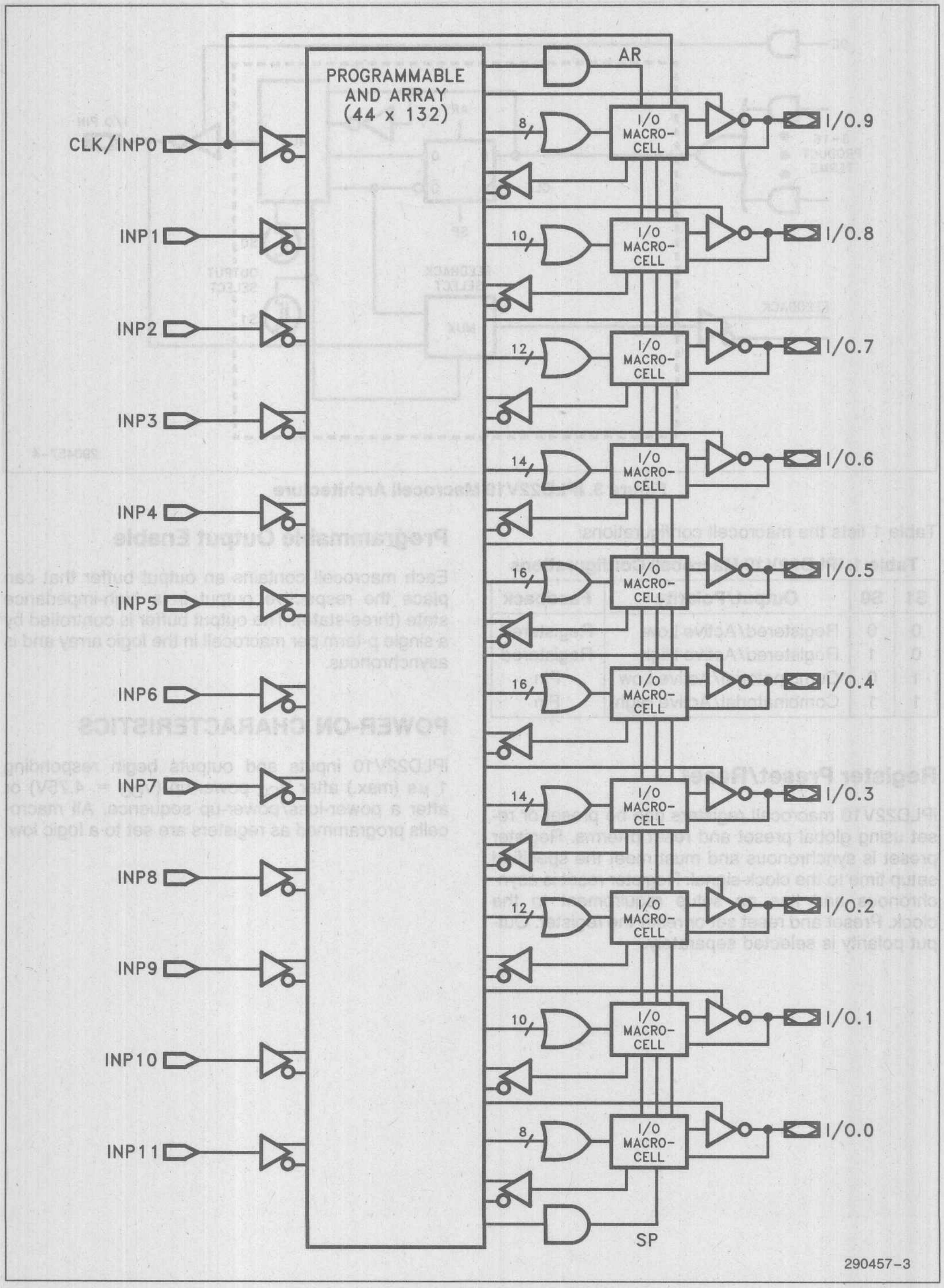


Figure 2. iPLD22V10 Global Architecture

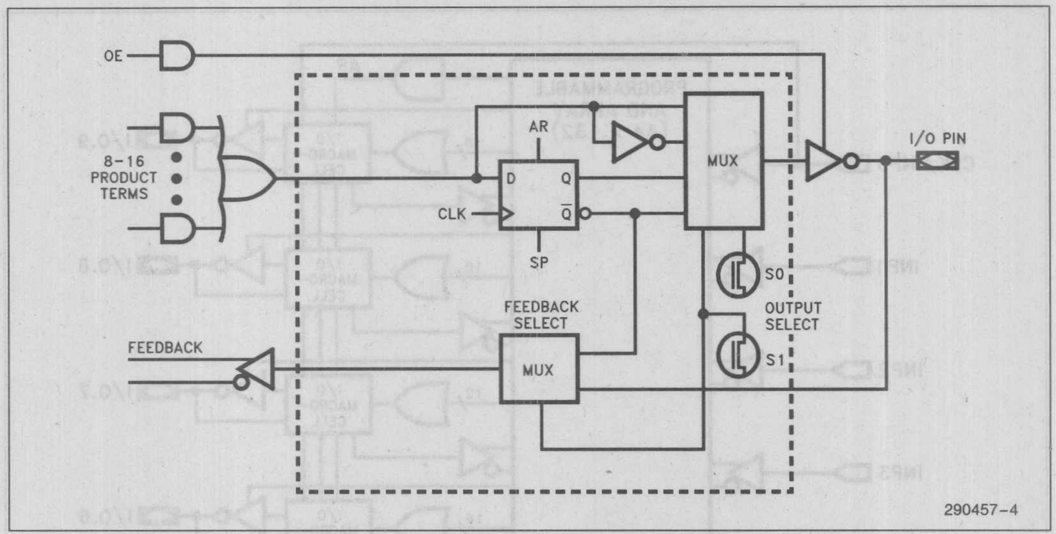


Figure 3. iPLD22V10 Macrocell Architecture

Table 1 lists the macrocell configurations:

Table 1. iPLD22V10 Macrocell Configurations

S1	S0	Output/Polarity	Feedback
0	0	Registered/Active Low	Registered
0	1	Registered/Active High	Registered
1	0	Combinatorial/Active Low	Pin
1	1	Combinatorial/Active High	Pin

Register Preset/Reset

iPLD22V10 macrocell registers can be preset or reset using global preset and reset p-terms. Register preset is synchronous and must meet the specified setup time to the clock signal. Register reset is asynchronous and has no setup requirement to the clock. Preset and reset set or reset the register. Output polarity is selected separately.

Programmable Output Enable

Each macrocell contains an output buffer that can place the respective output in a high-impedance state (three-state). The output buffer is controlled by a single p-term per macrocell in the logic array and is asynchronous.

POWER-ON CHARACTERISTICS

iPLD22V10 inputs and outputs begin responding 1 μs (max.) after V_{CC} power-up (V_{CC} = 4.75V) or after a power-loss/power-up sequence. All macrocells programmed as registers are set to a logic low.

PROGRAMMING CHARACTERISTICS

Prior to programming, all EPROM logic array cells are in the "connected" state. The macrocells by default are configured for registered output, active-low operation with registered feedback.

Intelligent Programming Alogrithm

The iPLD22V10 supports the Intelligent Programming Algorithm, a fast, reliable algorithm for programming many types of Intel programmable devices.

PROCESS TECHNOLOGY

The iPLD22V10 is fabricated on Intel's CHMOS EPROM process. Over 20 million devices (including EPROMs and Microcontrollers) have been fabricated on this process.

TESTABILITY

The iPLD22V10 is completely tested at the factory. Unlike fuse-based PLDs, which have one-time programmable fuse links that limit testing to small-scale sampling, each EPROM cell in the iPLD22V10 is tested and erased prior to shipment.

SECURITY

A single programmable bit, called the security bit or verify protect bit, controls access to the data programmed into the device. Once this security bit is set, the design cannot be copied.

Since data in the device is stored in EPROM cells, the contents of the device cannot be read even with microscopic examination, providing an additional level of design security not available with fuse-based devices.

DEVELOPMENT SOFTWARE

Third Party Support

The iPLD22V10 is supported by third-party logic compilers such as ABEL*, CUPL*, PLDesigner*, Log/IC, etc. Programming support is provided by third-party programmer companies such as Data I/O, Logical Devices, STAG, etc. Please refer to the "Third-Party Support" lists in the *Programmable Logic* handbook for complete information and vendor contacts.

PLDshell PLUS

Full logic compilation and functional simulation for the iPLD22V10 is supported by PLDshell Plus software.

PLDshell Plus design software is Intel's new, user-friendly design tool for PLD design. PLDshell Plus allows users to incorporate their preferred text editor, programming software, and additional design tools into a easy-to-use, menued design environment that includes Intel's PLDasm logic compiler and simulation software along with disassembly, conversion, and translation utilities. The PLDasm compiler and simulator software accepts industry-standard PDS source files that express designs as Boolean equations, truth tables, or state machines. On-line help, datasheet briefs, technical notes, and error message information, along with waveform viewing/printing capability make the design task as easy as possible. PLDshell Plus software is available from Intel Literature channels or from your local Intel sales representative, order #468810.

*ABEL is a trademark of Data I/O Corp. CUPL is a trademark of Logical Devices, Inc. PLDesigner is a trademark of MINC, Inc. Log/IC is a trademark of ISDATA, Corporation.

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage (V_{CC})(1) .... $-2.0V$ to $+7.0V$

Programming Supply
Voltage (V_{PP})(1) .... $-2.0V$ to $+13.5V$

D.C. Input Voltage (V_I)(1, 2) ... $-0.5V$ to $V_{CC} + 0.5V$

Storage Temperature (T_{stg}) ..... $-65°C$ to $+150°C$

Ambient Temperature (T_A)(3) ..... $-10°C$ to $+85°C$

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

RECOMMENDED OPERATING CONDITIONS

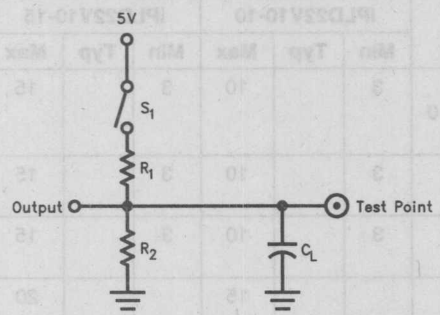
Symbol	Parameter	Min	Max	Units
V_{CC}	Supply Voltage	4.75	5.25	V
V_{IN}	Input Voltage	0	V_{CC}	V
V_O	Output Voltage	0	V_{CC}	V
T_A	Operating Temperature	0	+70	°C
t_R	Input Rise Time		5	ns
t_F	Input Fall Time		5	ns

D.C. CHARACTERISTICS ($T_A = 0°C$ to $+70°C$, $V_{CC} = 5.0V + 5\%$)

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
V_{IH}(4)	High Level Input Voltage	2.0		$V_{CC} + 0.3$	V	
V_{IL}(4)	Low Level Input Voltage	-0.3		0.8	V	
V_{OH}	TTL High Output Voltage	2.4			V	$I_O = -4$ mA D.C., V_{CC} = Min
	CMOS High Output Voltage	$V_{CC} - 0.3$			V	$I_O = -100$ pH = V_{CC} Min
V_{OL}	Low Level Output Voltage			0.45	V	$I_O = 16$ mA D.C., V_{CC} = Min
I_I	Input Leakage Current			10	μA	V_{CC} = Max., GND < V_{IN} < V_{CC}
I_{OZ}	Output Leakage Current			10	μA	V_{CC} = Max., GND < V_{OUT} < V_{CC}
I_{SC}(5)	Output Short Circuit Current			120	mA	V_{CC} = Max., $V_{OUT} = 0.5V$
I_{CC}	Power Supply Current (See I_{CC} vs. Freq. Graph)		90	130	mA	V_{CC} = Max., $V_{IN} = V_{CC}$ or GND, No Load, $f_{IN} = 15$ MHz, Device Prog. as a 10-Bit Counter

NOTES:
1. Voltages with respect to GND.
2. Minimum D.C. input is $-0.5V$. During transitions, the inputs may undershoot to $-2.0V$ or overshoot to $+7.0V$ for periods of less than 20 ns under no load conditions.
3. Under bias. Extended Temperature versions are also available.
4. Absolute values with respect to device GND; all over and undershoots due to system or tester noise are included.
5. Not more than 1 output should be tested at a time. Duration of that test should not exceed 1 second.

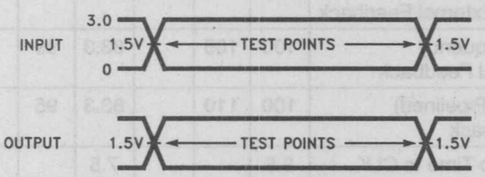
A.C. TESTING LOAD CIRCUIT



290457–5

Specification	S_1	C_L	Commercial R_1	Commercial R_2	Measured Output Value
t_{PD}, t_{CO}	Closed	50 pF	240Ω	160Ω	1.5V
t_{PZX}	Z → H: Open Z → L: Closed				1.5V
t_{PXZ}	H → Z: Open L → Z: Closed	5 pF			H → Z: V_{OH} − 0.5V L → Z: V_{OL} + 0.5V

A.C. TESTING INPUT, OUTPUT WAVEFORM



290457–6

A.C. Testing: Inputs are Driven at 3.0V for a Logic "1" and 0V for a Logic "0". Timing Measurements are made at 1.5V. Outputs are measured at 1.5V. Device input rise and fall times < 3 ns.

CAPACITANCE (T_A = 0°C to 70°C; V_{CC} = 5.0V ±5%)(6)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
C_{IN}	Input Capacitance		5	8	pF	V_{IN} = 0V, f = 1.0 MHz
C_{IO}	I/O Capacitance		6	8	pF	V_{OUT} = 0V, f = 1.0 MHz
C_{CLK}	CLK Capacitance		15	17	pF	V_{OUT} = 0V, f = 1.0 MHz

COMBINATORIAL MODE A.C. CHARACTERISTICS

(T_A = 0°C to +70°C, V_{CC} = 5.0V ±5%)(7)

Symbol	Parameter	iPLD22V10-10			iPLD22V10-15			PLD22V10-25			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{PD}(8)	Input or I/O to Output Valid—w/10 Outputs Switching	3		10	3		15			25	ns
t_{PZX}(9)	Input or I/O to Output Enable	3		10	3		15			25	ns
t_{PXZ}(9)	Input or I/O to Output Disable	3		10	3		15			25	ns
t_{CLR}	Input or I/O to Asynch. Reset			15			20			20	ns

NOTES:

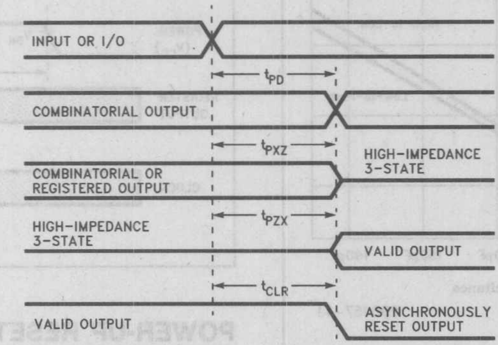
6. These values are evaluated at initial characterization and whenever design modifications occur that may affect capacitance.
7. Typical values are at T_A = +25°C, V_{CC} = 5V.
8. Ten outputs switching.
9. t_{PZX} and t_{PXZ} are measured at ±0.5V from steady state voltage as driven by spec. output load. t_{PXZ} is measured with C_L = 5 pF. Z → H and Z → L are measured at 1.5V on output.
10. Measured with device configured as a 10-bit counter.

REGISTER MODE—SYNCHRONOUS CLOCK A.C. CHARACTERISTICS

(T_A = 0°C to +70°C, V_{CC} = 5.0V ±5%)(7)

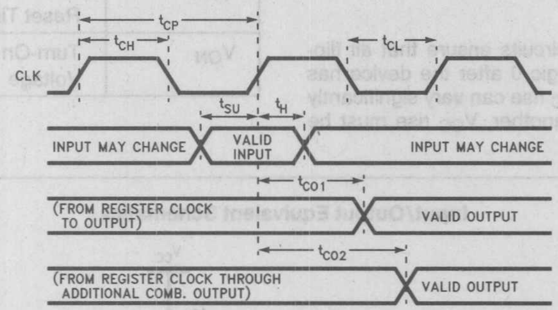
Symbol	Parameter	iPLD22V10-10			iPLD22V10-15			PLD22V10-25			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{CNT1}(8)	Max. Counter Frequency $1/(t_{SU} + t_{CO})$—External Feedback	95.2	100		64.5	70		35.7	40		MHz
f_{CNT2}(8)	Max. Counter Frequency $1/(t_{CNT})$—Internal Feedback	100	105		83.3	95		40	45		MHz
f_{MAX}	Max. Frequency (Pipelined) $1/t_{CP}$—No Feedback	100	110		83.3	95		40	45		MHz
t_{SU}	Input or I/O Setup Time to CLK	3.5			7.5			14			ns
t_{SP}	Input or I/O Setup Time to Synchronous Preset	4.5				7.5		10.5			ns
t_H	Input or I/O Hold Time from CLK	0			0			0			ns
t_{CO1}	CLK to Output Valid	3		7	2		8	2		14	ns
t_{CO2}	CLK to Output Valid Fed Through Combinatorial Macrocell			16			18			30	ns
t_{CNT}	Register Output Feedback to Register Input—Internal Path			10			12			25	ns
t_{CL}	CLK Low Time	4			5			10			ns
t_{CH}	CLK High Time	4			5			10			ns
t_{CP}	CLK Period	10			12			25			ns
t_{arw}	Asynchronous Reset Pulse Duration	4			5			5			ns
t_{arr}	Asynchronous Reset to CLK ↑ Recovery Time	7			9			10			ns

COMBINATORIAL MODE



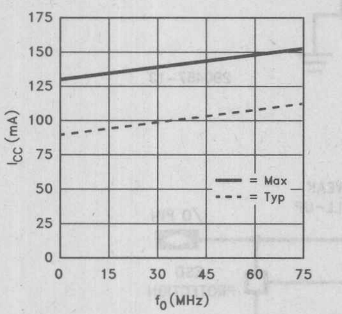
290457-7

SYNCHRONOUS REGISTERED MODE



290457-8

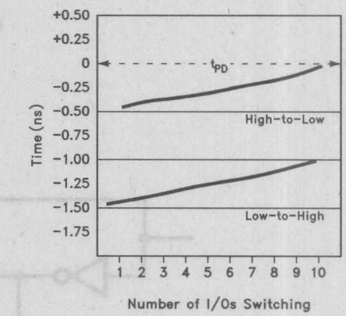
iPLD22V10 I_{CC} vs Frequency



290457-9

Conditions:
$T_A = 0°$
$V_{CC} = 5.25V$

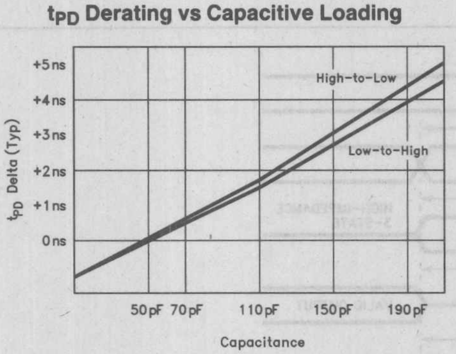
t_{PD} Derating vs Number of Outputs Switching



290457-10

Conditions:
$T_A = 70°C$
$V_{CC} = 4.75V$
$C_L = 50\ pF$

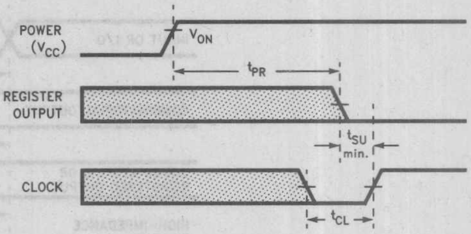
2



290457-11

Conditions:
$T_A = 70°C$
$V_{CC} = 4.75V$

POWER-UP RESET



290457-12

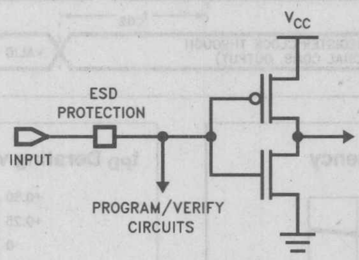
POWER-UP RESET CHARACTERISTICS

Parameter Symbol	Parameter Description	Value
t_{PR}	Power-Up Reset Time	1000 ns Max.
V_{ON}	Turn-On Voltage	4.75V

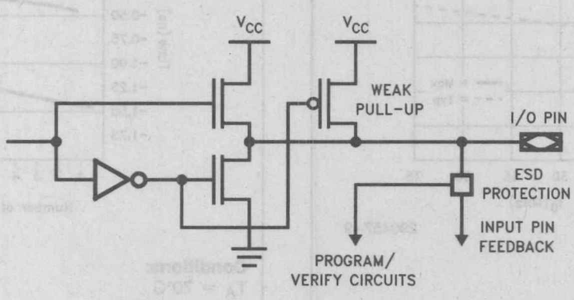
POWER-UP RESET

Internal power-up reset circuits ensure that all flip-flops will be reset to a logic 0 after the device has powered up. Because V_{CC} rise can vary significantly from one application to another, V_{CC} rise must be monotonic.

Input/Output Equivalent Schematics



290457-13



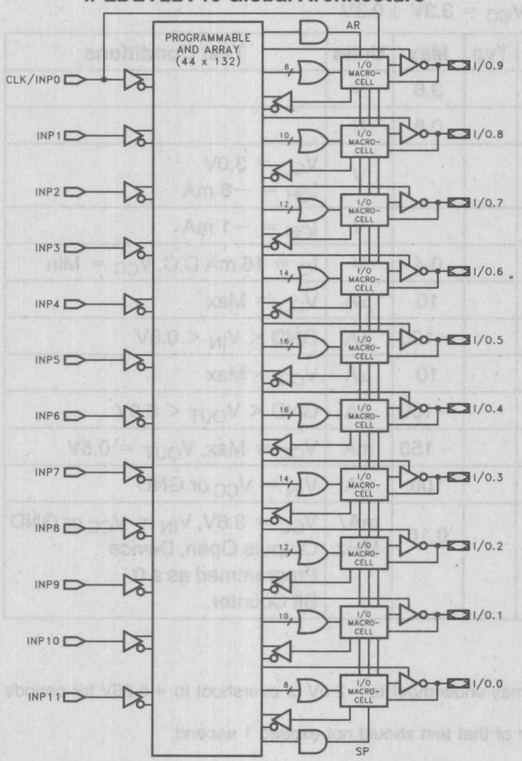
290457-14

LOW VOLTAGE, ELECTRICALLY ERASABLE 10-MACROCELL CMOS PLD

- **Low Voltage, Low Current, High Speed Upgrade to BiCMOS/Bipolar 22V10 and CMOS Equivalents**
- **Supply Voltage Range 3.0V to 3.6V. Ideal for Battery Powered Systems**
- **t_{PD} 5 ns, 142 MHz with Feedback**
- **Maximum I_{SB} = 100 μA**
- **Typical I_{CC} = 10 mA @ 100 MHz**
- **12 Dedicated Inputs, 10 I/O Pins**
- **10 Macrocells with Programmable I/O Architecture (Registered/ Combinatorial)**
- **Global Asynchronous Clear and Synchronous Preset P-terms**
- **Sub-micron CHMOS III Electrical Erasable Technology**
- **Programmable "Security Bit" Allows Total Protection of Proprietary Designs**
- **Available in 28-Pin PLCC Packages**

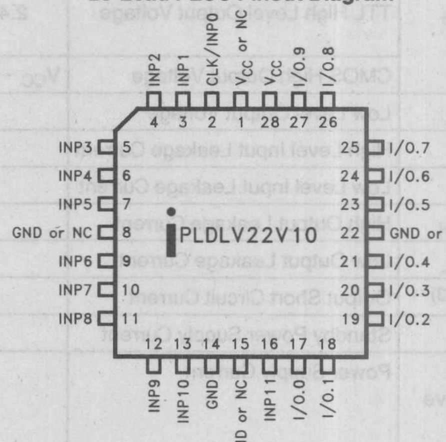
2

iPLDLV22V10 Global Architecture



290495–2

28-Lead PLCC Pinout Diagram



290495–1

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage (V_{CC})(1) .... −1.0V to +3.6V

Programming Supply Voltage (V_{PP})(1) .... −1.0V to +8.0V

DC Input Voltage (V_I)(1, 2) .... −0.5V to +3.6V

Storage Temperature (T_{stg}) .... −65°C to +150°C

NOTICE: This data sheet contains information on products in the sampling and initial production phases of development. The specifications are subject to change without notice. Verify with your local Intel Sales office that you have the latest data sheet before finalizing a design.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Units
V_{CC}	Supply Voltage	3	3.6	V
V_{IN}	Input Voltage	0	V_{CC}	V
V_O	Output Voltage	0	V_{CC}	V
T_A	Operating Temperature	0	70	°C

D.C. CHARACTERISTICS T_A = 0°C to +70°C, V_{CC} = 3.3V ±0.3V

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
V_{IH}(1)	High Level Input Voltage	2		3.6	V	
V_{IL}(2)	Low Level Input Voltage	−0.5		0.8	V	
V_{OH}	TTL High Level Output Voltage	2.4			V	V_{CC} = 3.0V I_{OH} = −8 mA
	CMOS High Output Voltage	V_{CC} −0.3			V	I_{OH} = −1 mA
V_{OL}	Low Level Output Voltage			0.4	V	I_O = 16 mA D.C. V_{CC} = Min
I_{IH}	High Level Input Leakage Current			10	μA	V_{CC} = Max
I_{IL}	Low Level Input Leakage Current			−100	μA	GND < V_{IN} < 0.8V
I_{OZH}	High Output Leakage Current			10	μA	V_{CC} = Max
I_{OZL}	Low Output Leakage Current			−100	μA	GND < V_{OUT} < 0.8V
I_{SC}(3)	Output Short Circuit Current			−150	mA	V_{CC} = Max, V_{OUT} = 0.5V
I_{SB}	Standby Power Supply Current			100	μA	V_{IN} = V_{CC} or GND
I_{CC} Active	Power Supply Current			0.10	mA/MHz	V_{CC} = 3.6V, V_{IN} = V_{CC} or GND Outputs Open, Device Programmed as a 0 Bit Counter.

NOTES:
1. Voltages with respect to GND
2. Minimum D.C. input is −0.5V. During transitions, the inputs may undershoot to −2.0V or overshoot to +5.25V for periods less than 20 ns under no load conditions.
3. Not more than 1 output should be tested at a time. Duration of that test should not exceed 1 second.

COMBINATORIAL MODE A.C. CHARACTERISTICS

$T_A = 0°C$ to $+70°C$, $V_{CC} = 3.3V \pm 0.3V^{(4)}$

Symbol	Parameter	iPLDLV22V10-5 Min	Typ	Max	Units
t_{PD}(5)	Input or I/O to Output Valid	2		5	ns
t_{PZX}(6)	Input or I/O to Output Enable	2		6	ns
t_{PXZ}(6)	Input or I/O to Output Disable	2		5	ns
t_{CLR}	Input or I/O to Asynch. Reset	2		6	ns

NOTES:
4. Typical values are at $T_A = +25°C$, $V_{CC} = 3.3V$.
5. Refer to switching test conditions.
6. t_{PXZ} is measured at $\pm 0.5V$ from steady state voltage as driven by specified output load. t_{PXZ} is measured with $C_L = 5$ pF. Z → H and Z → L are measured at 1.5V on output.

2

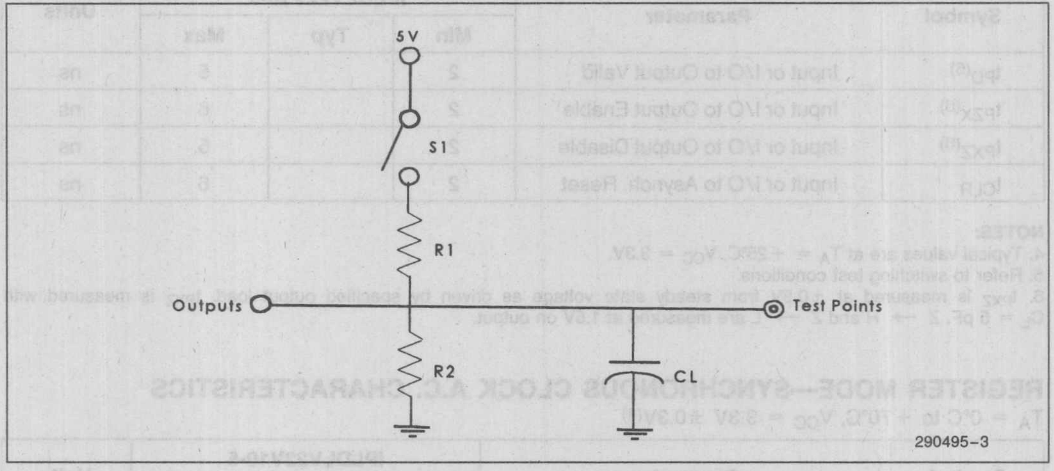
REGISTER MODE—SYNCHRONOUS CLOCK A.C. CHARACTERISTICS

$T_A = 0°C$ to $+70°C$, $V_{CC} = 3.3V \pm 0.3V^{(4)}$

Symbol	Parameter	iPLDLV22V10-5 Min	Typ	Max	Units
f_{CNT}(5)	Maximum Counter Frequency $1/(t_{SU} + t_{CO})$—External Feedback	142			MHz
f_{CNT}(5)	Maximum Counter Frequency $1/(t_{CNT})$—Internal Feedback	166			MHz
f_{MAX}(5)	Maximum Frequency (Pipelined) $1/t_{CP}$—No Feedback	166			MHz
t_{SU}	Input or I/O Setup Time to CLK	3.5			ns
t_H	Input or I/O Hold Time from CLK	0		0	ns
t_{CO1}	CLK to Output Valid	1.5		3.5	ns
t_{CO2}	CLK to Output Valid Fed Through Combinatorial Macrocell	4		8	ns
t_{CNT}	Register Output Feedback to Register Input—Internal Path			6	ns
t_{CL}	CLK Low Time	3			ns
t_{CH}	CLK High Time	3			ns
t_{CP}	CLK Period	6			ns

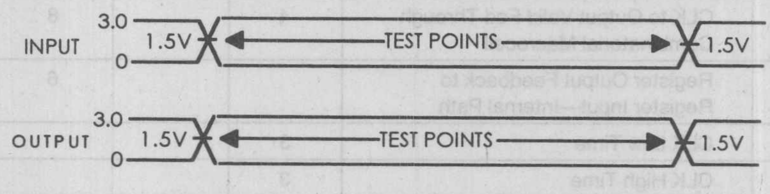
SWITCHING TEST CONDITIONS

A.C. TESTING LOAD CIRCUIT



Specification	S1	CL	Commercial		Measured Output Value
			R1	R2	
t_{PD}, t_{CO}	Closed	50 pF	230Ω	260Ω	1.5V
t_{PZX}	Z → H: Open Z → L: Closed				1.5
t_{PXZ}	H → Z: Open L → Z: Closed	5 pF			H → Z: V_{OH} − 0.5V L → Z: V_{OL} + 0.5V

A.C. TESTING INPUT, OUTPUT WAVEFORM



NOTE:
A.C. Testing: Inputs are driven at 3.0V for a logic "1" and 0V for a logic "0". Timing measurements are made at 1.5V on inputs and outputs. Device input rise and fall times <2 ns.

CAPACITANCE $T_A = 0°C$ to $+70°C$, $V_{CC} = 3.3V \pm 0.3V$(7)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
C_{IN}	Input Capacitance	$V_{IN} = 0V$, f = 1.0 MHz		5	8	pF
C_{IO}	I/O Capacitance	$V_{OUT} = 0V$, f = 1.0 MHz		6	8	pF
C_{CLK}	CLK Capacitance	$V_{OUT} = 0V$, f = 1.0 MHz		15	17	pF

NOTES:
7. These values are evaluated at initial characterization and whenever design modifications occur that may affect capacitance.

intel®

iPLDLV22V10-15
LOW VOLTAGE, HIGH PERFORMANCE 10-MACROCELL CMOS PLD

Low Voltage High-Speed Upgrade to Bipolar 22V10 and CMOS Equivalents

- **Supply Voltage Range 3.0V to 3.6V**
- **t_{PD} 15 ns, 50 MHz with Feedback, 83.3 MHz with No Feedback**
- **Max I_{CC} = 35 mA**
- **12 Dedicated Inputs and 10 I/O Pins**
- **10 Macrocells with Programmable I/O Architecture (Register/Combinatorial)**
- **Variable P-terms—Up to 16 per Macrocell, Selectable Output Polarity, Separate Output Enable P-term**
- **Global Asynchronous Clear and Synchronous Preset P-terms**
- **1-Micron CHMOS IIIE EPROM Technology**
- **Programmable "Security Bit" Allows Total Protection of Proprietary Designs**
- **100% Generically Tested Logic Array**
- **Available in 300-mil 24-Pin PDIP and 28-Pin PLCC Packages**
  (See Packaging Spec., Order Number 240800, Package Type N and P)

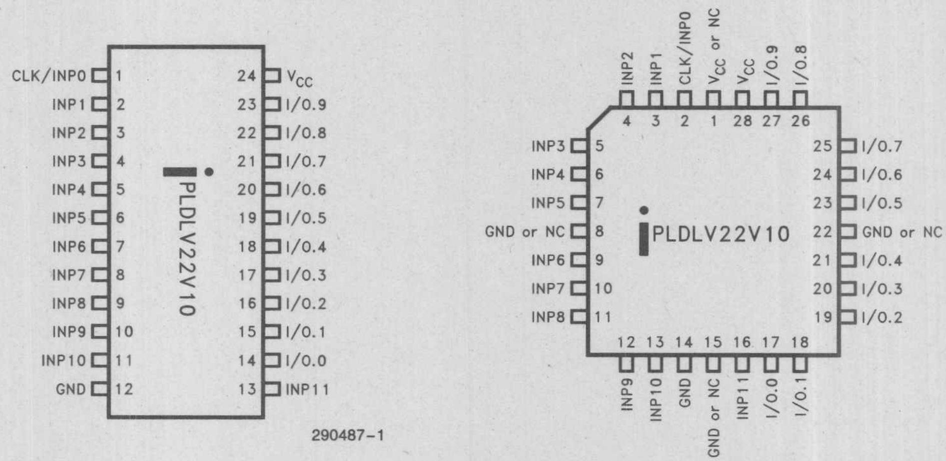


Figure 1. Pinout Diagrams

Log/IC is a trademark of ISDATA, Inc.

October 1993
Order Number: 290487-001

INTRODUCTION

The iPLDLV22V10 is a low voltage, high-performance, high-integration, general-purpose CMOS PLD and operates at 3.3V core logic and I/O. The iPLDLV22V10 accommodates logic functions with up to 22 inputs and 10 I/O macrocells. I/O macrocells include an average of 12 p-terms for input, with a separate p-term for output enable. Figure 2 shows the global architecture of the device.

JEDEC AND PIN COMPATIBILITY

The iPLDLV22V10 is 100% JEDEC-, pin- and function-compatible with the industry-standard 22V10 PLD. JEDEC files developed for 22V10 devices can be used to program the iPLDLV22V10. When the N PLDLV22V10 (28-pin PLCC) is used to replace a conventional 22V10 in an existing design socket, pins 8, 15, 22 and 1 are left as No Connects (NC). New designs can take advantage of the additional device V_{CC} and grounds these pins offer.

PROGRAMMABLE MACROCELLS

In addition to the 12 dedicated input pins, the iPLDLV22V10 contains 10 programmable macrocells. Each of the macrocells can be programmed to function as an input or as a combinatorial or registered output. Programmable output polarity and programmable feedback options allow the iPLDLV22V10 to be tailored to the precise needs of the target application. Figure 3 shows the architecture of each macrocell.

Output Polarity

The output polarity for each iPLDLV22V10 macrocell is programmable. Each combinatorial or registered output can be active-high or active-low.

Feedback Options

iPLDLV22V10 macrocells programmed as combinatorial outputs support pin feedback to the logic array (i.e., feedback from the I/O pin). iPLDLV22V10 macrocells programmed as registers allow internal register feedback to the logic array.

ORDERING INFORMATION

f_{CNT1} (MHz)	f_{MAX} (MHz)	t_{PD} (ns)	Order Code	Package	Operating Range
50	83.3	15	P PLDLV22V10-15	PDIP	Commercial
			N PLDLV22V10-15	PLCC	Commercial

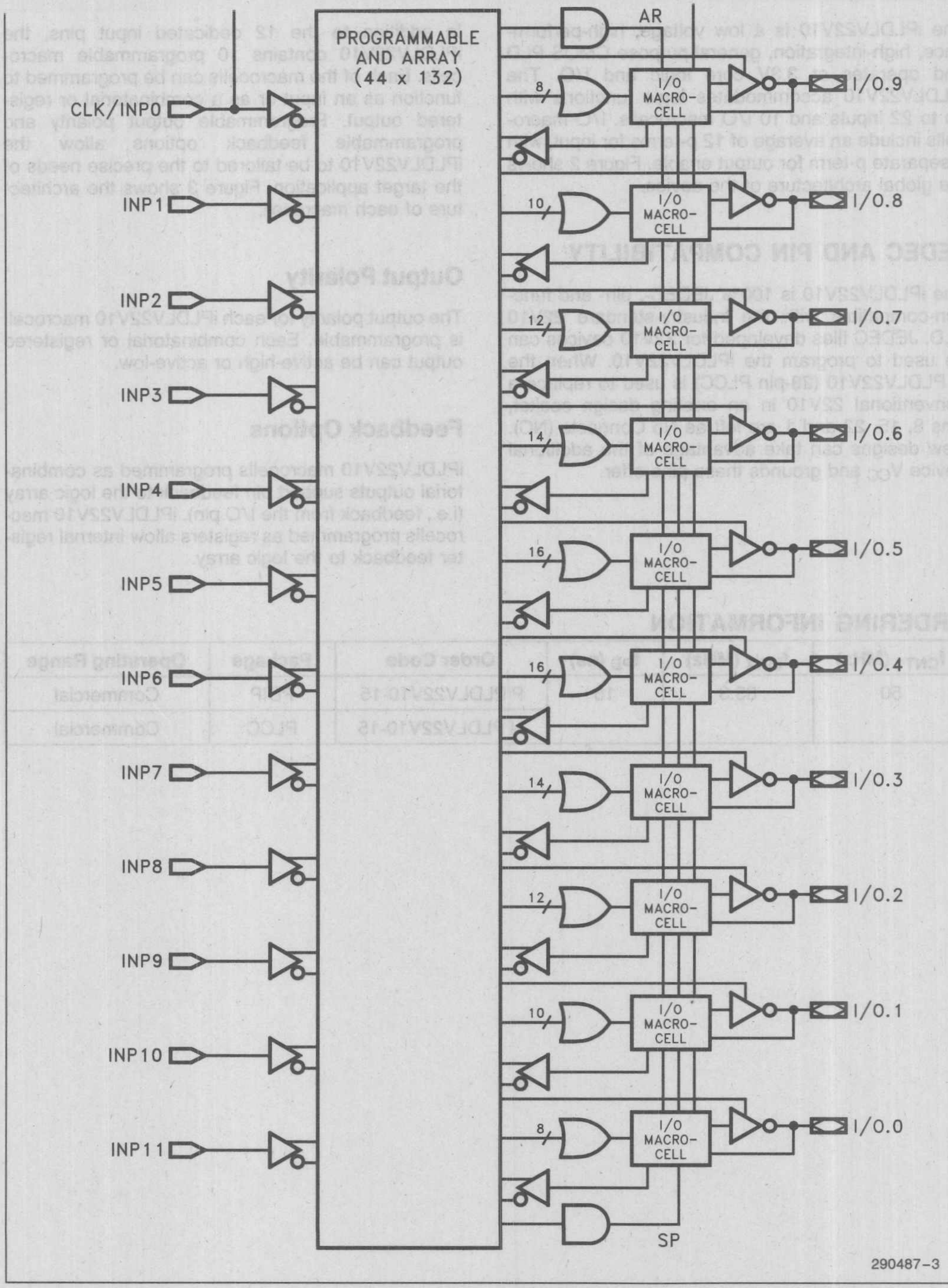


Figure 2. iPLDLV22V10 Global Architecture

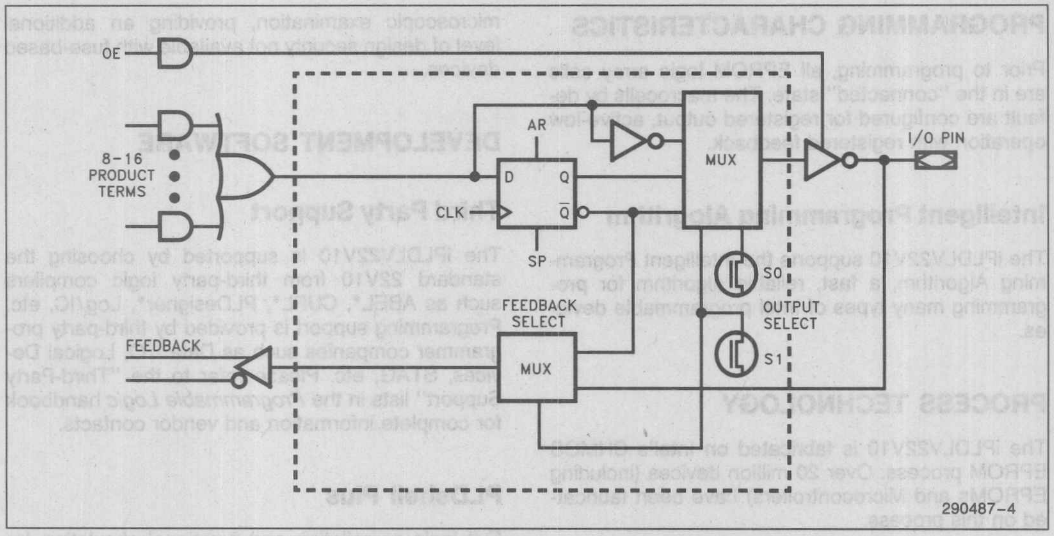


Figure 3. iPLDLV22V10 Macrocell Architecture

Table 1 lists the macrocell configurations:

Table 1. iPLDLV22V10 Macrocell Configurations

S1	S0	Output/Polarity	Feedback
0	0	Registered/Active Low	Registered
0	1	Registered/Active High	Registered
1	0	Combinatorial/Active Low	Pin
1	1	Combinatorial/Active High	Pin

Register Preset/Reset

iPLDLV22V10 macrocell registers can be preset or reset using global preset and reset p-terms. Register preset is synchronous and must meet the specified setup time to the clock signal. Register reset is asynchronous and has no setup requirement to the clock. Preset and reset set or reset the register. Output polarity is selected separately.

Programmable Output Enable

Each macrocell contains an output buffer that can place the respective output in a high-impedance state (three-state). The output buffer is controlled by a single p-term per macrocell in the logic array and is asynchronous.

POWER-ON CHARACTERISTICS

iPLDLV22V10 inputs and outputs begin responding 1 μs (max.) after V_{CC} power-up (V_{CC} = 3.0V) or after a power-loss/power-up sequence. All macrocells programmed as registers are set to a logic low.

PROGRAMMING CHARACTERISTICS

Prior to programming, all EPROM logic array cells are in the "connected" state. The macrocells by default are configured for registered output, active-low operation with registered feedback.

Intelligent Programming Alogrithm

The iPLDLV22V10 supports the Intelligent Programming Algorithm, a fast, reliable algorithm for programming many types of Intel programmable devices.

PROCESS TECHNOLOGY

The iPLDLV22V10 is fabricated on Intel's CHMOS EPROM process. Over 20 million devices (including EPROMs and Microcontrollers) have been fabricated on this process.

TESTABILITY

The iPLDLV22V10 is completely tested at the factory. Unlike fuse-based PLDs, which have one-time programmable fuse links that limit testing to small-scale sampling, each EPROM cell in the iPLDLV22V10 is tested and erased prior to shipment.

SECURITY

A single programmable bit, called the security bit or verify protect bit, controls access to the data programmed into the device. Once this security bit is set, the design cannot be copied.

Since data in the device is stored in EPROM cells, the contents of the device cannot be read even with microscopic examination, providing an additional level of design security not available with fuse-based devices.

DEVELOPMENT SOFTWARE

Third Party Support

The iPLDLV22V10 is supported by choosing the standard 22V10 from third-party logic compilers such as ABEL*, CUPL*, PLDesigner*, Log/IC, etc. Programming support is provided by third-party programmer companies such as Data I/O, Logical Devices, STAG, etc. Please refer to the "Third-Party Support" lists in the *Programmable Logic* handbook for complete information and vendor contacts.

PLDshell Plus

Full logic compilation and functional simulation for the iPLDLV22V10 is supported by PLDshell Plus software by choosing the PLD22V10 option on the programming menu.

PLDshell Plus design software is Intel's new, user-friendly design tool for PLD design. PLDshell Plus allows users to incorporate their preferred text editor, programming software, and additional design tools into a easy-to-use, menued design environment that includes Intel's PLDasm logic compiler and simulation software along with disassembly, conversion, and translation utilities. The PLDasm compiler and simulator software accepts industry-standard PDS source files that express designs as Boolean equations, truth tables, or state machines. On-line help, datasheet briefs, technical notes, and error message information, along with waveform viewing/printing capability make the design task as easy as possible. PLDshell Plus software is available from Intel Literature channels or from your local Intel sales representative, order #611942.

*ABEL is a trademark of Data I/O Corp. CUPL is a trademark of Logical Devices, Inc. PLDesigner is a trademark of MINC, Inc. Log/IC is a trademark of ISDATA, Corporation.

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage (V_{CC})(1) .... −2.0V to +7.0V
Programming Supply Voltage (V_{PP})(1).............. −2.0V to +13.5V
D.C. Input Voltage (V_I)(1, 2) ... −0.5V to V_{CC} + 0.5V
Storage Temperature (T_{stg}) ..... −65°C to +150°C
Ambient Temperature (T_A) .... −10°C to +85°C

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

******WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

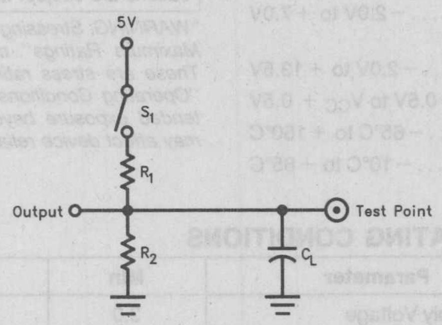
RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Units
V_{CC}	Supply Voltage	3.0	3.6	V
V_{IN}	Input Voltage	0	V_{CC}	V
V_O	Output Voltage	0	V_{CC}	V
T_A	Operating Temperature	0	+70	°C

D.C. CHARACTERISTICS (T_A = 0°C to +70°C, V_{CC} = 3.3V ±10%)

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
V_{IH}(3)	High Level Input Voltage	2.0		V_{CC} + 0.3	V	
V_{IL}(3)	Low Level Input Voltage	−0.6		0.8	V	
V_{OH}	TTL High Output Voltage	2.4			V	V_{CC} = 3.0V I_{OH} = −0.4 mA
	CMOS High Output Voltage	V_{CC} − 0.3			V	I_O = −100 pH = V_{CC} Min
V_{OL}	Low Level Output Voltage			0.5	V	I_O = 16 mA D.C., V_{CC} = Min
I_I	Input Leakage Current			10	μA	V_{CC} = Max., GND < V_{IN} < V_{CC}
I_{OZ}	Output Leakage Current			10	μA	V_{CC} = Max., GND < V_{OUT} < V_{CC}
I_{SC}(4)	Output Short Circuit Current			120	mA	V_{CC} = Max., V_{OUT} = 0.5V
I_{CC}	Power Supply Current			35	mA	V_{CC} = 3.6V

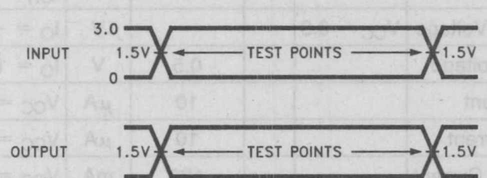
NOTES:
1. Voltages with respect to GND.
2. Minimum D.C. input is −0.5V. During transitions, the inputs may undershoot to −2.0V or overshoot to +7.0V for periods of less than 20 ns under no load conditions.
3. Absolute values with respect to device GND; all over and undershoots due to system or tester noise are included.
4. Not more than 1 output should be tested at a time. Duration of that test should not exceed 1 second.



290487-5

Specification	S_1	C_L	Commercial R_1	Commercial R_2	Measured Output Value
t_{PD}, t_{CO}	Closed	50 pF	240Ω	160Ω	1.5V
t_{PZX}	Z → H: Open Z → L: Closed	50 pF	240Ω	160Ω	1.5V
t_{PXZ}	H → Z: Open L → Z: Closed	5 pF	240Ω	160Ω	H → Z: $V_{OH} - 0.5V$ L → Z: $V_{OL} + 0.5V$

A.C. TESTING INPUT, OUTPUT WAVEFORM



290487-6

A.C. Testing: Inputs are Driven at 3.0V for a Logic "1" and 0V for a Logic "0". Timing Measurements are made at 1.5V. Outputs are measured at 1.5V. Device input rise and fall times < 3 ns.

CAPACITANCE ($T_A = 0°C$ to $70°C$; $V_{CC} = 3.3V \pm 10\%$)(5)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
C_{IN}	Input Capacitance		5	8	pF	$V_{IN} = 0V$, f = 1.0 MHz
C_{IO}	I/O Capacitance		6	8	pF	$V_{OUT} = 0V$, f = 1.0 MHz
C_{CLK}	CLK Capacitance		15	17	pF	$V_{OUT} = 0V$, f = 1.0 MHz

(T_A = 0°C to +70°C, V_{CC} = 3.3V ±10%)(6)

Symbol	Parameter	iPLDLV22V10-15			Units
		Min	Typ	Max	
t_{PD}(7)	Input or I/O to Output Valid—w/10 Outputs Switching	6		15	ns
t_{PZX}(8)	Input or I/O to Output Enable	6		15	ns
t_{PXZ}(8)	Input or I/O to Output Disable	6		15	ns
t_{CLR}	Input or I/O to Asynch. Reset			20	ns

NOTES:

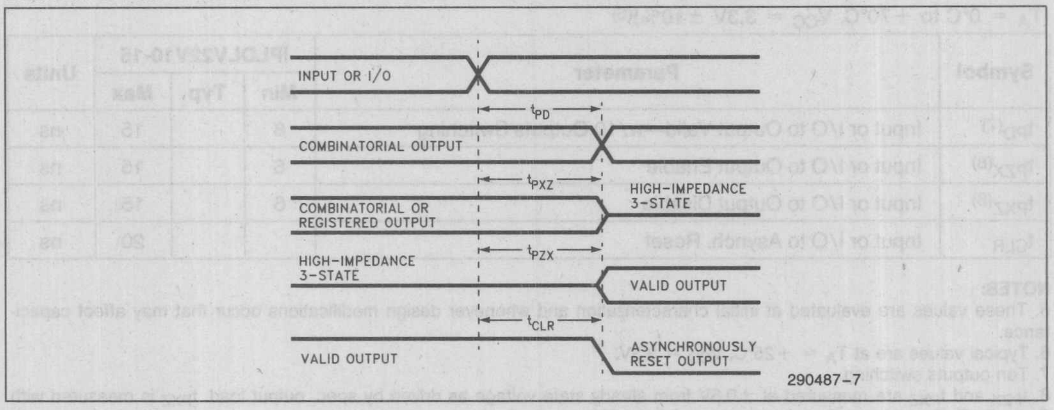
5. These values are evaluated at initial characterization and whenever design modifications occur that may affect capacitance.
6. Typical values are at T_A = +25°C, V_{CC} = 3.3V.
7. Ten outputs switching.
8. t_{PZX} and t_{PXZ} are measured at ±0.5V from steady state voltage as driven by spec. output load. t_{PXZ} is measured with C_L = 5 pF. Z → H and Z → L are measured at 1.5V on output.
9. Measured with device configured as a 10-bit counter.

REGISTER MODE—SYNCHRONOUS CLOCK A.C. CHARACTERISTICS

(T_A = 0°C to +70°C, V_{CC} = 3.3V ±10%)(6)

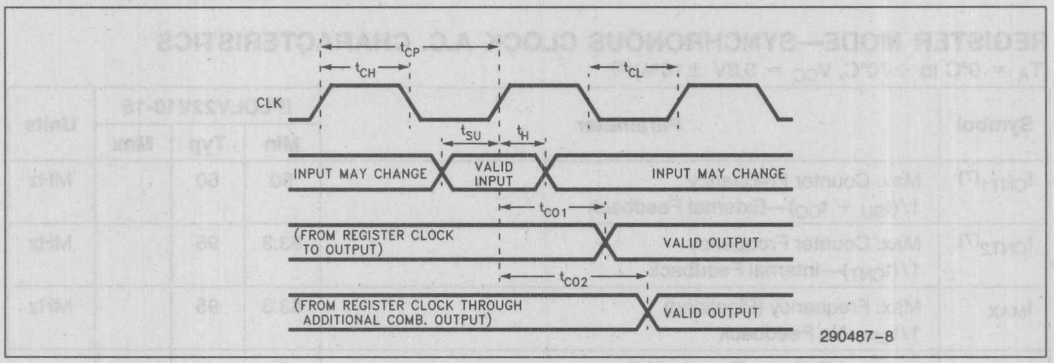
Symbol	Parameter	iPLDLV22V10-15			Units
		Min	Typ	Max	
f_{CNT1}(7)	Max. Counter Frequency 1/(t_{SU} + t_{CO})—External Feedback	50	60		MHz
f_{CNT2}(7)	Max. Counter Frequency 1/(t_{CNT})—Internal Feedback	83.3	95		MHz
f_{MAX}	Max. Frequency (Pipelined) 1/t_{CP}—No Feedback	83.3	95		MHz
t_{SU}	Input or I/O Setup Time to CLK	3			ns
t_{SP}	Input or I/O Setup Time to Synchronous Preset	10			ns
t_H	Input or I/O Hold Time from CLK	0			ns
t_{CO1}	CLK to Output Valid	3		10	ns
t_{CO2}	CLK to Output Valid Fed Through Combinatorial Macrocell			18	ns
t_{CNT}	Register Output Feedback to Register Input—Internal Path			12	ns
t_{CL}	CLK Low Time	5			ns
t_{CH}	CLK High Time	5			ns
t_{CP}	CLK Period	12			ns
t_{arw}	Asynchronous Reset Pulse Duration	5			ns
t_{arr}	Asynchronous Reset to CLK ↑ Recovery Time	10			ns

COMBINATORIAL MODE

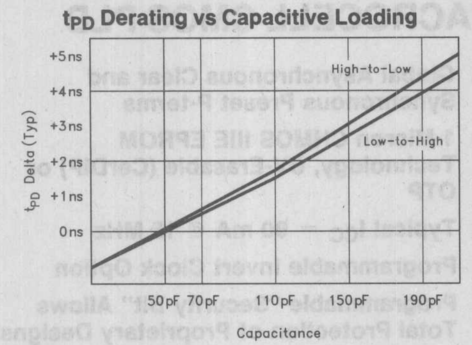


290487–7

SYNCHRONOUS REGISTERED MODE



290487–8



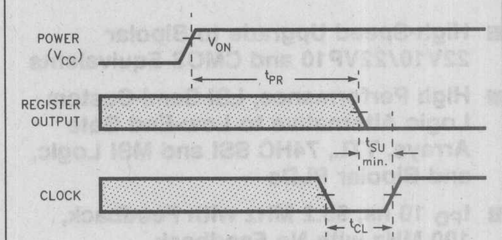
290487-9

Conditions:
$T_A = 70°C$
$V_{CC} = 4.75V$

POWER-UP RESET

Internal power-up reset circuits ensure that all flip-flops will be reset to a logic 0 after the device has powered up. Because V_{CC} rise can vary significantly from one application to another, V_{CC} rise must be monotonic.

POWER-UP RESET

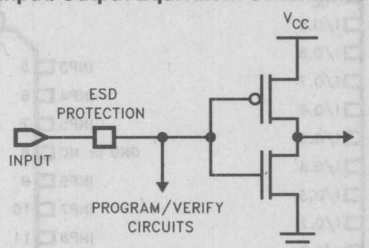


290487-10

POWER-UP RESET CHARACTERISTICS

Parameter Symbol	Parameter Description	Value
t_{PR}	Power-Up Reset Time	1000 ns Max.
V_{ON}	Turn-On Voltage	2.5V

Input/Output Equivalent Schematics



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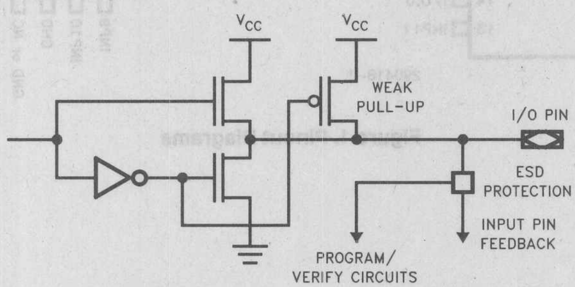
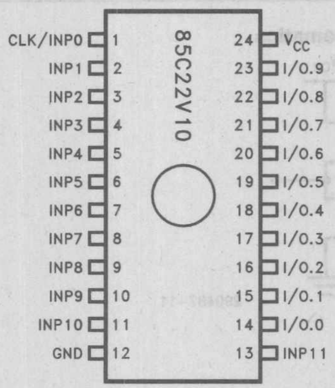


290487-12

85C22V10
HIGH PERFORMANCE 10-MACROCELL CMOS PLD

- High-Speed Upgrade to Bipolar 22V10/22VP10 and CMOS Equivalents
- High Performance, LSI Semi-Custom Logic Alternative to Low-End Gate Arrays, TTL, 74HC SSI and MSI Logic, and Bipolar PLDs
- t_{PD} 10 ns, 95.2 MHz with Feedback, 100 MHz with No Feedback
- 12 Dedicated Inputs and 10 I/O Pins
- 10 Macrocells with Programmable I/O Architecture (Register/Combinatorial)
- Variable P-terms—Up to 16 per Macrocell, Selectable Output Polarity, Separate Output Enable P-term
- Global Asynchronous Clear and Synchronous Preset P-terms
- 1-Micron CHMOS IIIE EPROM Technology, UV-Erasable (CerDIP) or OTP
- Typical I_{CC} = 90 mA @ 15 MHz
- Programmable Invert Clock Option
- Programmable "Security Bit" Allows Total Protection of Proprietary Designs
- 100% Generically Tested Logic Array
- Available in 300-mil 24-Pin CerDIP/PDIP and 28-Pin PLCC Packages
  (See Packaging Spec., Order Number 240800, Package Type D, N and P)



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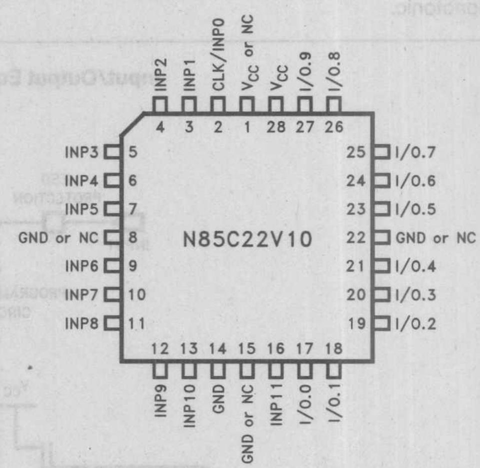


290416-2

Figure 1. Pinout Diagrams

October 1993
Order Number: 290416-005

The 85C22V10 is a high-performance, high-integration, general-purpose CMOS PLD. The 85C22V10 accommodates logic functions with up to 22 inputs and 10 I/O macrocells. I/O macrocells include an average of 12 p-terms for input, with a separate p-term for output enable. Figure 2 shows the global architecture of the device.

JEDEC AND PIN COMPATIBILITY

The 85C22V10 is 100% JEDEC-, pin- and function-compatible with the industry-standard 22V10 PLD. JEDEC files developed for 22V10 devices can be used to program the 85C22V10. For designs requiring the 85C22V10 *superset* features, a new JEDEC must be developed. When the N85C22V10 (28-pin PLCC) is used to replace a conventional 22V10 in an existing design socket, pins 8, 15, 22 and 1 are left as No Connects (NC). New designs can take advantage of the additional device V_{CC} and grounds these pins offer.

PROGRAMMABLE MACROCELLS

In addition to the 12 dedicated input pins, the 85C22V10 contains 10 programmable macrocells. Each of the macrocells can be programmed to function as an input or as a combinatorial or registered output. Programmable output polarity and program-tailored to the precise needs of the target application. Figure 3 shows the architecture of each macrocell.

Output Polarity

The output polarity for each 85C22V10 macrocell is programmable. Each combinatorial or registered output can be active-high or active-low.

Feedback Options

85C22V10 macrocells programmed as combinatorial outputs support pin feedback to the logic array (i.e., feedback from the I/O pin). 85C22V10 macrocells programmed as registers allow internal register feedback to the logic array. These options are supported on both the 22V10 and 22VP10 devices.

85C22V10 macrocells programmed as registers also allow feedback to the logic array from the I/O pin. This feature is also supported on 22VP10 devices.

In addition, however, the 85C22V10 provides a *superset* feature with its ability to implement a combinatorial output with registered feedback to the logic array. This feedback option allows a single 85C22V10 macrocell to implement designs that would take up two macrocells in 22V10/22VP10 devices.

ORDERING INFORMATION

f_{CNT1} (MHz)	f_{MAX} (MHz)	t_{PD} (ns)	Order Code	Package	Operating Range
95.2	100	10	D85C22V10-10	*CerDIP	Commercial
			P85C22V10-10	PDIP	Commercial
			N85C22V10-10	PLCC	Commercial
64.5	83.3	15	D85C22V10-15	*CerDIP	Commercial
			P85C22V10-15	PDIP	Commercial
			N85C22V10-15	PLCC	Commercial

*Only the windowed CerDIP package allows UV erase.

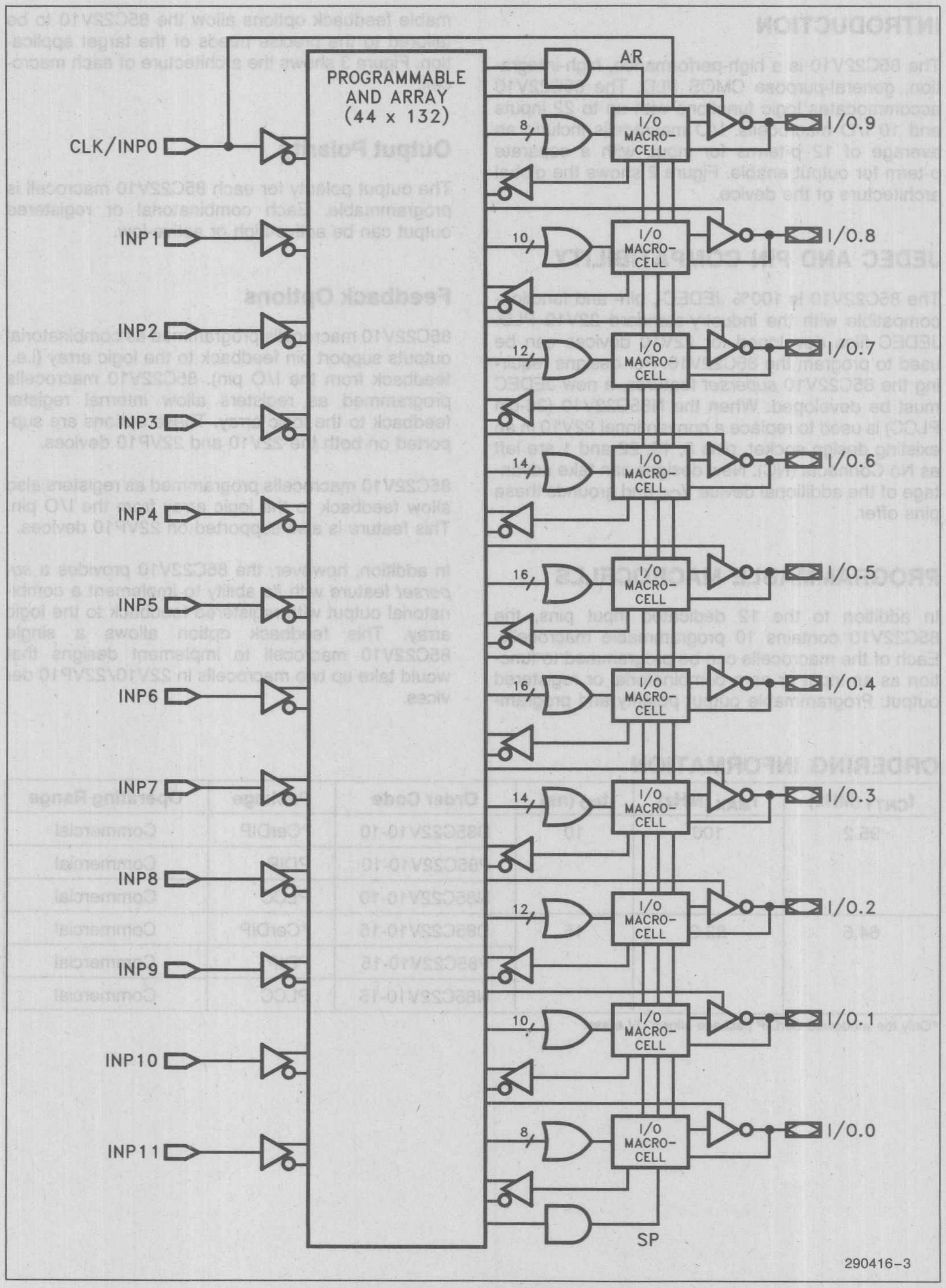


Figure 2. 85C22V10 Global Architecture

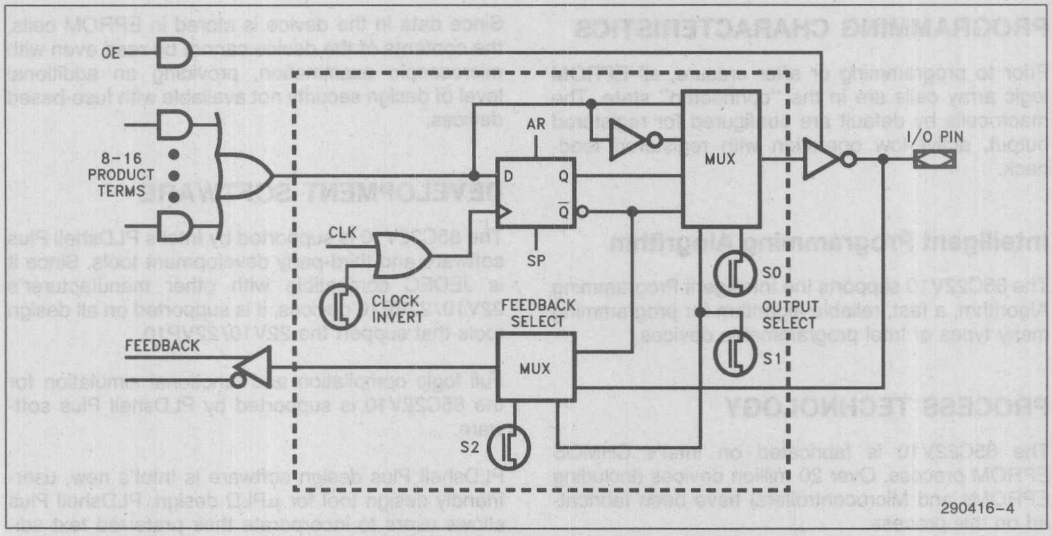


Figure 3. 85C22V10 Macrocell Architecture

Table 1 lists the macrocell configurations:

Table 1. 85C22V10 Macrocell Configurations

S2	S1	S0	Output/Polarity	Feedback
0	0	0	Registered/Active Low	Registered
0	0	1	Registered/Active High	Registered
0	1	0	Combinatorial/Active Low	Pin
0	1	1	Combinatorial/Active High	Pin
1	0	0	**Registered/Active Low	Pin
1	0	1	**Registered/Active High	Pin
1	1	0	*Combinatorial/Active Low	Registered
1	1	1	*Combinatorial/Active High	Registered

*Not available on the 22V10 or 22VP10.
**Not available on the 22V10.

Clock Invert

A clock invert option for each macrocell allows macrocell registers to be independently clocked on the rising or falling edge of the global clock. This *superset* feature allows the 85C22V10 to implement designs that could not be implemented in a 22V10/22VP10 device.

Register Preset/Reset

85C22V10 macrocell registers can be preset or reset using global preset and reset p-terms. Register preset is synchronous and must meet the specified setup time to the clock signal. Register reset is asynchronous and has no setup requirement to the clock. Preset and reset set or reset the register. Output polarity is selected separately.

Programmable Output Enable

Each macrocell contains an output buffer that can place the respective output in a high-impedance state (three-state). The output buffer is controlled by a single p-term per macrocell in the logic array and is asynchronous.

POWER-ON CHARACTERISTICS

85C22V10 inputs and outputs begin responding 1 μs (max.) after V_{CC} power-up (V_{CC} = 4.75V) or after a power-loss/power-up sequence. All macrocells programmed as registers are set to a logic low.

ERASURE CHARACTERISTICS

Erase time for the 85C22V10 is 2½ hours at 12,000 μW/cm^2 with a 2537Å lamp.

Erasure begins upon exposure to light with wavelengths shorter than approximately 4000Å. Sunlight and certain types of fluorescent lamps have wavelengths in the 3000Å to 4000Å range. Erase data indicates that constant exposure to room level fluorescent lighting will erase the device in approximately six years. It would take approximately two weeks of constant exposure to direct sunlight to erase the device.

PROGRAMMING CHARACTERISTICS

Prior to programming or after erasure, all EPROM logic array cells are in the "connected" state. The macrocells by default are configured for registered output, active-low operation with registered feedback.

Intelligent Programming Alogrithm

The 85C22V10 supports the Intelligent Programming Algorithm, a fast, reliable algorithm for programming many types of Intel programmable devices.

PROCESS TECHNOLOGY

The 85C22V10 is fabricated on Intel's CHMOS EPROM process. Over 20 million devices (including EPROMs and Microcontrollers) have been fabricated on this process.

TESTABILITY

The 85C22V10 is completely tested at the factory. Unlike fuse-based PLDs, which have one-time programmable fuse links that limit testing to small-scale sampling, each EPROM cell in the 85C22V10 is tested and erased prior to shipment.

REGISTER PRELOAD

85C22V10 macrocell registers can be preloaded with any pattern to allow testing of all possible logic states. Information on register preload for test purposes is available from Intel.

SECURITY

A single programmable bit, called the security bit or verify protect bit, controls access to the data programmed into the device. Once this security bit is set, the design cannot be copied. The security bit is cleared via UV-erasure along with device contents.

Since data in the device is stored in EPROM cells, the contents of the device cannot be read even with microscopic examination, providing an additional level of design security not available with fuse-based devices.

DEVELOPMENT SOFTWARE

The 85C22V10 is supported by Intel's PLDshell Plus software and third-party development tools. Since it is JEDEC compatible with other manufacturer's 22V10/22VP10 devices, it is supported on all design tools that support the 22V10/22VP10.

Full logic compilation and functional simulation for the 85C22V10 is supported by PLDshell Plus software.

PLDshell Plus design software is Intel's new, user-friendly design tool for μPLD design. PLDshell Plus allows users to incorporate their preferred text editor, programming software, and additional design tools into an easy-to-use, menued design environment that includes Intel's PLDasm logic compiler and simulation software along with disassembly, conversion, and translation utilities. The PLDasm compiler and simulator software accepts industry-standard PDS source files that express designs as Boolean equations, truth tables, or state machines. On-line help, datasheet briefs, technical notes, and error message information, along with waveform viewing/printing capability make the design task as easy as possible. PLDshell Plus software is available from Intel Literature channels or from your local Intel sales representative, order #468810.

Tools that support schematic capture and timing simulation for the 85C22V10 are available. Support under iPLS II is still available. Please refer to the "Development Tools" section of the Programmable Logic handbook.

cations are subject to change without notice.

Supply Voltage (V_{CC})(1) .... −2.0V to +7.0V

Programming Supply
Voltage (V_{PP})(1) .... −2.0V to +13.5V

D.C. Input Voltage (V_I)(1, 2) ... −0.5V to V_{CC} + 0.5V

Storage Temperature (T_{stg}) ..... −65°C to +150°C

Ambient Temperature (T_A)(3) ..... −10°C to +85°C

WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

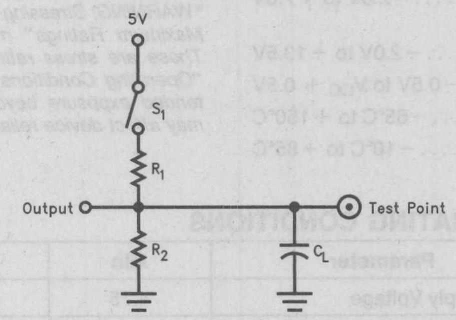
Symbol	Parameter	Min	Max	Units
V_{CC}	Supply Voltage	4.75	5.25	V
V_{IN}	Input Voltage	0	V_{CC}	V
V_O	Output Voltage	0	V_{CC}	V
T_A	Operating Temperature	0	+70	°C
t_R	Input Rise Time		5	ns
t_F	Input Fall Time		5	ns

D.C. CHARACTERISTICS (T_A = 0°C to +70°C, V_{CC} = 5.0V +5%)

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
V_{IH}(4)	High Level Input Voltage	2.0		V_{CC} + 0.3	V	
V_{IL}(4)	Low Level Input Voltage	−0.3		0.8	V	
V_{OH}	TTL High Output Voltage	2.4			V	I_O = −4 mA D.C., V_{CC} = Min
	CMOS High Output Voltage	V_{CC} − 0.3			V	I_O = −100 pH, V_{CC} = Min
V_{OL}	Low Level Output Voltage			0.45	V	I_O = 16 mA D.C., V_{CC} = Min
I_I	Input Leakage Current			10	μA	V_{CC} = Max., GND < V_{IN} < V_{CC}
I_{OZ}	Output Leakage Current			10	μA	V_{CC} = Max., GND < V_{OUT} < V_{CC}
I_{SC}(5)	Output Short Circuit Current			120	mA	V_{CC} = Max., V_{OUT} = 0.5V
I_{CC}	Power Supply Current (See I_{CC} vs. Freq. Graph)		90	130	mA	V_{CC} = Max., V_{IN} = V_{CC} or GND, No Load, f_{IN} = 15 MHz, Device Prog. as a 10-Bit Counter

NOTES:
1. Voltages with respect to GND.
2. Minimum D.C. input is −0.5V. During transitions, the inputs may undershoot to −2.0V or overshoot to +7.0V for periods of less than 20 ns under no load conditions.
3. Under bias. Extended Temperature versions are also available.
4. Absolute values with respect to device GND; all over and undershoots due to system or tester noise are included.
5. Not more than 1 output should be tested at a time. Duration of that test should not exceed 1 second.

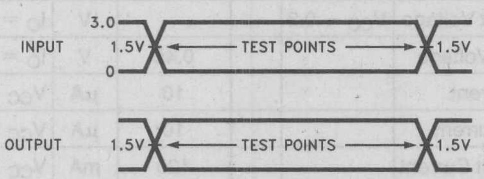
A.C. TESTING LOAD CIRCUIT



290416-5

Specification	S_1	C_L	Commercial R_1	Commercial R_2	Measured Output Value
t_{PD}, t_{CO}	Closed	50 pF	240Ω	160Ω	1.5V
t_{PZX}	Z → H: Open Z → L: Closed				1.5V
t_{PXZ}	H → Z: Open L → Z: Closed	5 pF			H → Z: V_{OH} − 0.5V L → Z: V_{OL} + 0.5V

A.C. TESTING INPUT, OUTPUT WAVEFORM



290416-6

A.C. Testing: Inputs are Driven at 3.0V for a Logic "1" and 0V for a Logic "0". Timing Measurements are made at 1.5V. Outputs are measured at 1.5V. Device input rise and fall times < 3 ns.

CAPACITANCE (T_A = 0°C to 70°C; V_{CC} = 5.0V ±5%)(6)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
C_{IN}	Input Capacitance		5	8	pF	V_{IN} = 0V, f = 1.0 MHz
C_{IO}	I/O Capacitance		6	8	pF	V_{OUT} = 0V, f = 1.0 MHz
C_{CLK}	CLK Capacitance		15	17	pF	V_{OUT} = 0V, f = 1.0 MHz

COMBINATORIAL MODE A.C. CHARACTERISTICS

(T_A = 0°C to +70°C, V_{CC} = 5.0V ±5%)(7)

Symbol	Parameter	85C22V10-10			85C22V10-15			Units
		Min	Typ	Max	Min	Typ	Max	
t_{PD}(8)	Input or I/O to Output Valid—w/10 Outputs Switching	3		10	3		15	ns
t_{PZX}(9)	Input or I/O to Output Enable	3		10	3		15	ns
t_{PXZ}(9)	Input or I/O to Output Disable	3		10	3		15	ns
t_{CLR}	Input or I/O to Asynch. Reset			15			20	ns

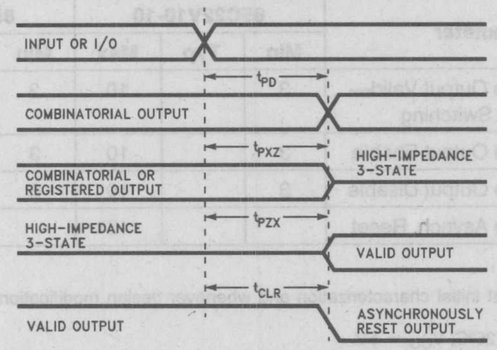
NOTES:
6. These values are evaluated at initial characterization and whenever design modifications occur that may affect capacitance.
7. Typical values are at T_A = +25°C, V_{CC} = 5V.
8. Ten outputs switching.
9. t_{PZX} and t_{PXZ} are measured at ±0.5V from steady state voltage as driven by spec. output load. t_{PXZ} is measured with C_L = 5 pF. Z → H and Z → L are measured at 1.5V on output.

REGISTER MODE—SYNCHRONOUS CLOCK A.C. CHARACTERISTICS

(T_A = 0°C to +70°C, V_{CC} = 5.0V ±5%)(7)

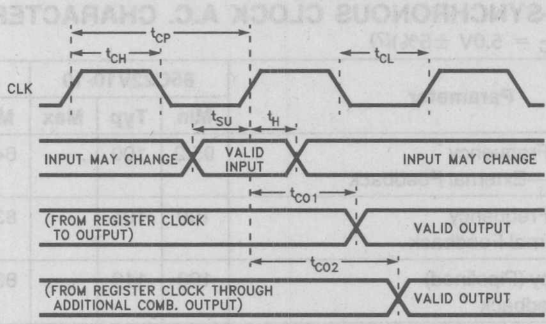
Symbol	Parameter	85C22V10-10			85C22V10-15			Units
		Min	Typ	Max	Min	Typ	Max	
f_{CNT1}(8)	Max. Counter Frequency 1/(t_{SU} + t_{CO})—External Feedback	95.2	100		64.5	70		MHz
f_{CNT2}(8)	Max. Counter Frequency 1/(t_{CNT})—Internal Feedback	100	105		83.3	95		MHz
f_{MAX}(8)	Max. Frequency (Pipelined) 1/t_{CP}—No Feedback	100	110		83.3	95		MHz
t_{SU1}	Input or I/O Setup Time to CLK	3.5			7.5			ns
t_{SU2}	Input or I/O Setup Time to Inverted CLK	4.5			8.5			ns
t_{SP}	Input or I/O Setup Time to Synchronous Preset	4.5			7.5			ns
t_H	Input or I/O Hold Time from CLK	0			0			ns
t_{CO1}	CLK to Output Valid	3		7	2		8	ns
t_{CO1}	Inverted CLK to Output Valid	3		7	2		8	ns
t_{CO2}	CLK to Output Valid Fed Through Combinatorial Macrocell			16			18	ns
t_{CNT}	Register Output Feedback to Register Input—Internal Path			10			12	ns
t_{CL}	CLK Low Time	4			5			ns
t_{CH}	CLK High Time	4			5			ns
t_{CP}	CLK Period	10			12			ns
t_{arw}	Asynchronous Reset Pulse Duration	4			5			ns
t_{arr}	Asynchronous Reset to CLK ↑ Recovery Time	7			9			ns

COMBINATORIAL MODE



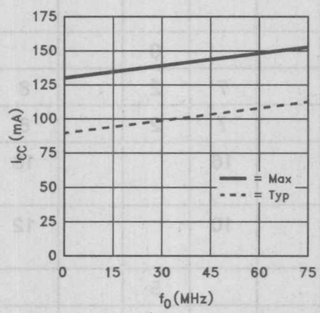
290416–7

SYNCHRONOUS REGISTERED MODE



290416–8

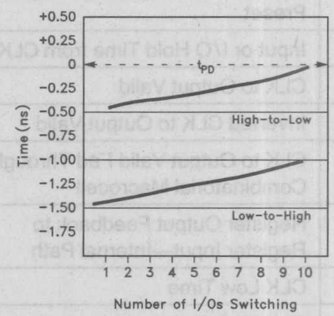
85C22V10 I_{CC} vs Frequency



290416–9

Conditions:
$T_A = 0°$
$V_{CC} = 5.25V$

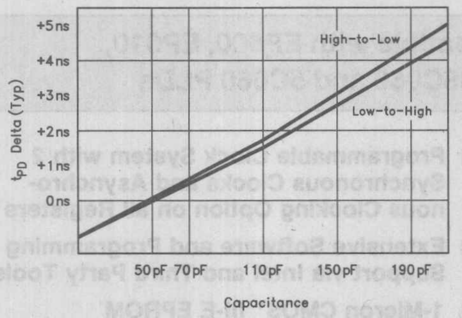
t_{PD} Derating vs Number of Outputs Switching



290416–10

Conditions:
$T_A = 70°C$
$V_{CC} = 4.75V$
$C_L = 50\ pF$

t_{PD} Derating vs Capacitive Loading



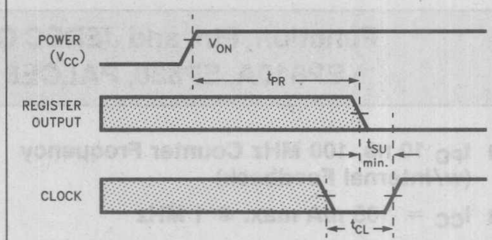
290416-11

Conditions:
$T_A = 70°C$
$V_{CC} = 4.75V$

POWER-UP RESET

Internal power-up reset circuits ensure that all flip-flops will be reset to a logic 0 after the device has powered up. Because V_{CC} rise can vary significantly from one application to another, V_{CC} rise must be monotonic.

POWER-UP RESET

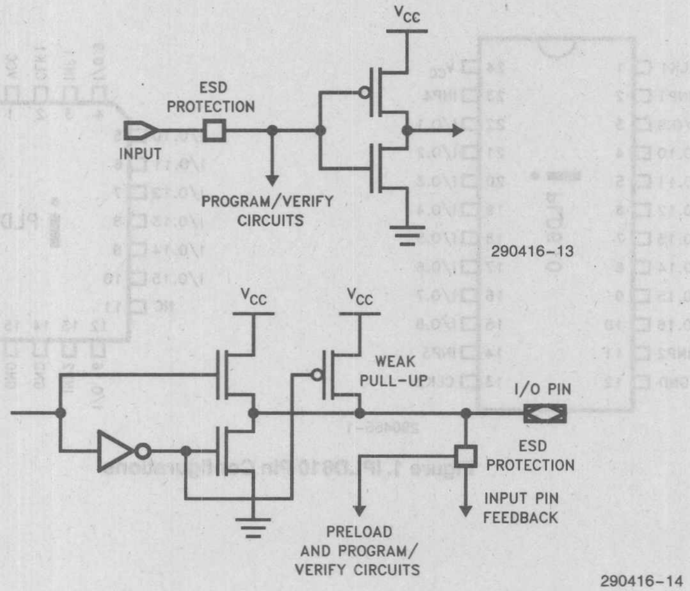


290416-12

POWER-UP RESET CHARACTERISTICS

Parameter Symbol	Parameter Description	Value
t_{PR}	Power-Up Reset Time	1000 ns Max.
V_{ON}	Turn-On Voltage	4.75V

Input/Output Equivalent Schematics



290416-14

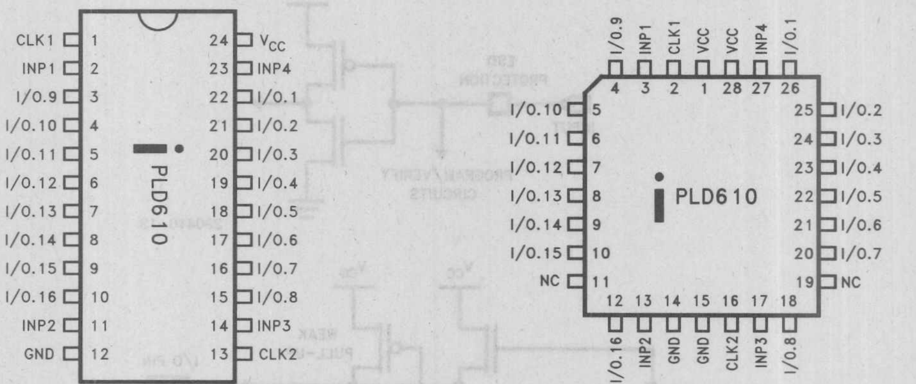
intel®

iPLD610
FAST 16-MACROCELL CMOS PLD

Function, Pin, and JEDEC Compatible with EP600, EP610, EP610A, EP630, PALCE610, 85C060 and 5C060 PLDs

- t_{PD} 10 ns, 100 MHz Counter Frequency (w/Internal Feedback)
- I_{CC} = 105 mA max. @ 1 MHz
- Programmable Low-Power Option for "Standby" Operation; 20 μA Typ. in Standby Mode
- Clocking Speed Same as −7 ns PAL* (74 MHz w/External Feedback)
- 16 Macrocells with Programmable I/O Architecture (Register/Combinatorial). Registers Configurable as D/T/JK/RS Types
- Up to 20 Inputs (4 Dedicated and 16 I/O)
- 8 P-Terms, Selectable SOP Invert, Clear and OE P-Terms for Each Macrocell
- Programmable Clock System with 2 Synchronous Clocks and Asynchronous Clocking Option on all Registers
- Extensive Software and Programming Support via Intel and Third Party Tools
- 1-Micron CMOS* III-E EPROM Technology
- Programmable "Security Bit" Allows Total Protection of Proprietary Designs
- 100% Generically Tested Logic Array
- Available in 300-mil 24-Pin PDIP, CerDIP and 28-Pin PLCC Packages

(See Packaging Specifications Order Number #240800-001, Package Type N and P)



290455–1

290455–2

Figure 1. iPLD610 Pin Configurations

*PAL is a registered trademark of Advanced Micro Devices, Inc.

October 1993
Order Number: 290455-002

INTRODUCTION

The iPLD610 is a high-performance, high-integration, general-purpose CMOS PLD. The iPLD610 PLD (Programmable Logic Device) accommodates logic functions with up to 20 inputs and 16 I/O macrocells. Each I/O macrocell includes 8 product-terms (p-terms) for input, a separate clear p-term, and an output enable/asynchronous clock p-term. The iPLD610 is function-, pin-, and JEDEC-compatible with the EP600, EP610, EP610A, EP630, PALCE610, 85C060 and 5C060 PLDs. With a clocking speed of 74 MHz (w/external feedback) the iPLD610 offers a higher integration, lower power alternative to registered −7 ns PALs/GALs.

The iPLD610 uses CMOS EPROM (floating gate) cells as logic control elements instead of fuses. The CMOS EPROM technology reduces power consumption in comparison to bipolar devices without sacrificing speed performance. In addition, Intel's advanced CMOS III-E EPROM process technology enables higher logic densities to be achieved with superior speed and low-power performance over other comparable devices. Intel's μPLDs add the benefits of "zero" stand-by power not available on other programmable logic devices. EPROM technology allows these devices to be 100% factory tested by programming and erasing all the EPROM logic control elements.

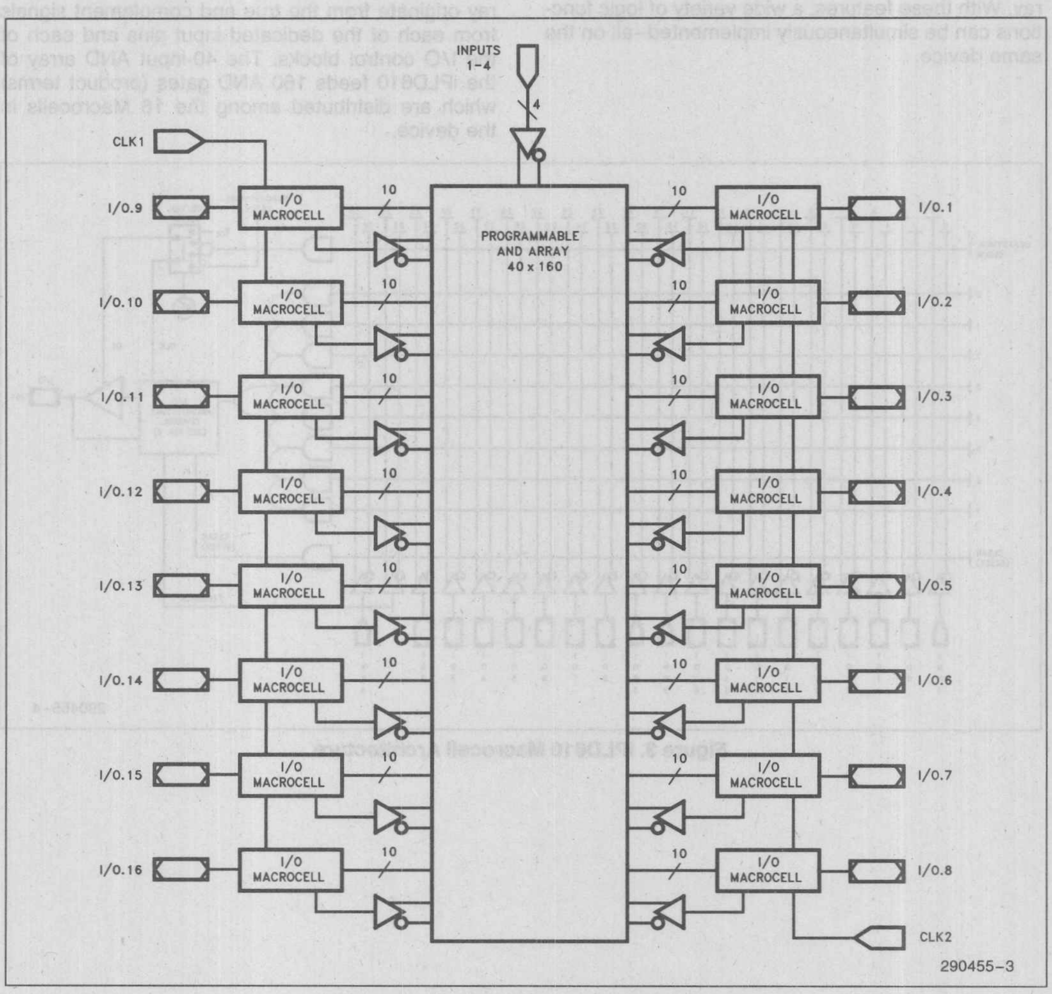


Figure 2. iPLD610 Global Architecture

The architecture of the iPLD610 is based on the "Sum of Products" PLA (Programmable Logic Array) structure with a programmable AND array feeding into a fixed OR array. The device accommodates combinational and sequential logic functions. A programmable I/O architecture provides individual selection of either combinatorial or registered output and feedback signals all with selectable polarity.

A feature unique to the iPLD610 is the ability to individually program the output registers as a D-, T-, SR-, or JK-type Flip-Flop without sacrificing the utilization of programmable AND logic. Each output register can be individually clocked from any of the input or feedback paths available within the AND array. With these features, a wide variety of logic functions can be simultaneously implemented–all on the same device.

ARCHITECTURE DESCRIPTION

Externally, the iPLD610 has 4 dedicated data input pins, 16 I/O pins that may be configured for input, output, or bidirectional operations, and 2 synchronous clock inputs. The iPLD610 is contained in a 24-pin ceramic windowed or OTP plastic (300 mils) or 28-lead OTP J-leaded chip carrier package.

The basic Macrocell architecture for the iPLD610 is shown in Figure 3. The iPLD610 has 16 of these Macrocells (one for each I/O pin). The Macrocell is organized in the familiar sum-of-products structure with a programmable AND array attached to a fixed OR term. The inputs to the programmable AND array originate from the true and complement signals from each of the dedicated input pins and each of the I/O control blocks. The 40-input AND array of the iPLD610 feeds 160 AND gates (product terms) which are distributed among the 16 Macrocells in the device.

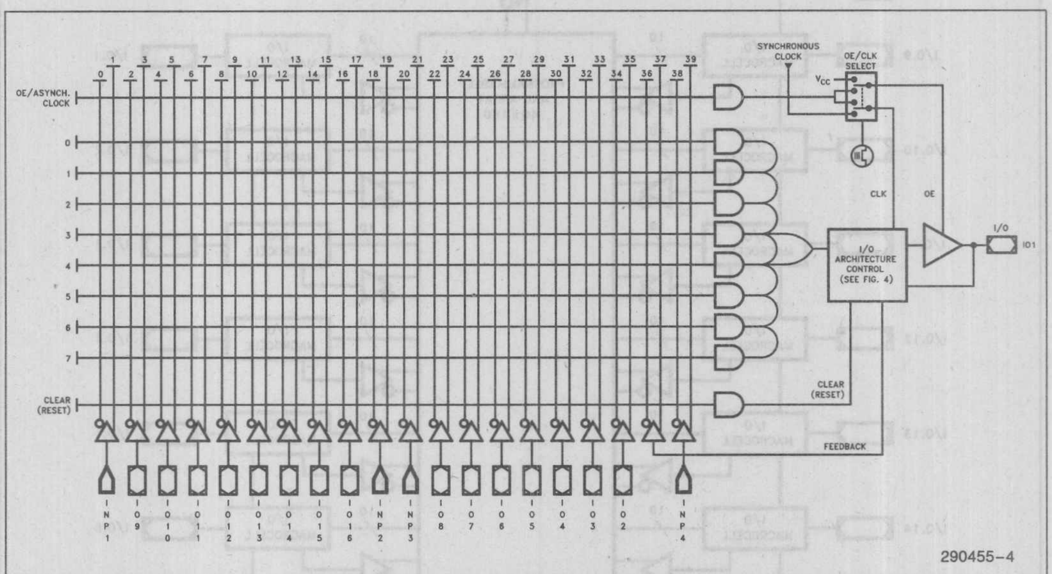


Figure 3. iPLD610 Macrocell Architecture

Each Macrocell contains ten product terms. Eight of the ten product terms (AND gates) are dedicated for the SOP logic implementation. One product term on each Macrocell is used for RESET control to the output register associated with the Macrocell. The final product term is used for OE/Asynchronous Clock implementation.

Within the AND array, there is an EPROM connection at every intersection of an input signal (true and complement) and a product term to a given Macrocell. Before programming an erased device, every EPROM connection is made at every intersection. But during the programming process, these connections are opened so that only the desired connections remain. Therefore, the true or complement of any input signal can be connected to any product term. If both the true and complement connections of any signal are left intact, a logical false results on the output of the AND gate. However, if both the true and complement connections are open, then a logic "don't care" results on the AND gate. Lastly, if all the inputs of a product term are programmed open, then a logical true results on the output of the AND gate.

The iPLD610 has two dedicated clock inputs to provide synchronous clock signals to the internal registers. Each of the clock signals controls half the total registers within the given device. For example, CLK1 provides synchronous clocking to the registers in Macrocells in the left half of the array while CLK2 controls the registers associated with Macrocells in the right half of the array. The advanced I/O architecture allows for any number of the registers to be synchronously clocked (from none to all). Both of the dedicated clock inputs latch the data into a given register when triggered on a positive edge.

MACROCELL ARCHITECTURE SELECTION

The iPLD610 architecture provides each Macrocell with over 50 different possible I/O register configurations. Each I/O pin can be configured for combinatorial or registered output (true or complement) with feedback. In addition, four different types of output registers can be implemented on I/O pin without any additional logic requirements. The feedback mechanism for each register back into the AND array can be programmed to provide for either registered feedback from the Macrocell or input feedback (treating the pin as an input). Another advantage of the advanced I/O capability of the iPLD610 is the ability to individually clock each internal register from asynchronous clock signals.

Invert Select EPROM Bit

The Invert Select EPROM bit is used to invert the product term input into the register. This applies to all inputs including double inputs on the JK and SR registers.

REGISTER SELECTION

The advanced I/O architecture of the iPLD610 allows four different register types along with combinatorial output as illustrated in Figure 4a. The register types include a T, D, JK, or SR Flip-Flop and each Macrocell I/O structure may be independently configured. In addition, all registers have an individual asynchronous RESET control from a dedicated product term derived in the AND array. When this dedicated product term is a logical one, the Macrocell register is immediately cleared to a logical zero independent of the register clock. The RESET function occurs automatically on power-up.

Output Register Configuration

The four different register types shown in Figure 4b–4e are described below.

D- or T-type Flip-Flops

When either a D- or T-type Flip-Flop is configured as part of the I/O structure, all eight of the product terms into the Macrocell are ORed together and fed into the register input.

JK or SR Registers

When either a JK or SR register is configured, the eight product terms are shared among two OR gates (one for the J or S input and the other for the K or R input). The allocation for these product terms for each of the register inputs is optimized by the PLDshell Plus software.

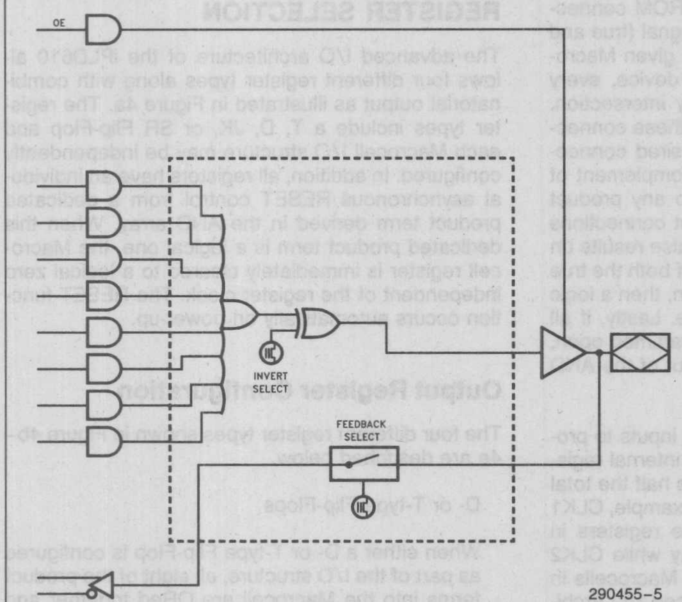
OUTPUT/FEEDBACK

The Output Select Multiplexer allows for either registered, combinatorial or no output.

The Feedback Select Multiplexer EPROM bit enables registered, I/O (using the pin for bidirectional input or just input), or no feedback to the AND array.

The Feedback Select is also important for building equations with more than 8 product terms. The 8-product product term of a Macrocell can be fed back into the AND array and combined with still more signals to create a much larger product term (of more than 8-inputs). If the feedback term is not to be used as an output, the associated Macrocell pin should be left floating (no connect) when assembled onto a circuit board.

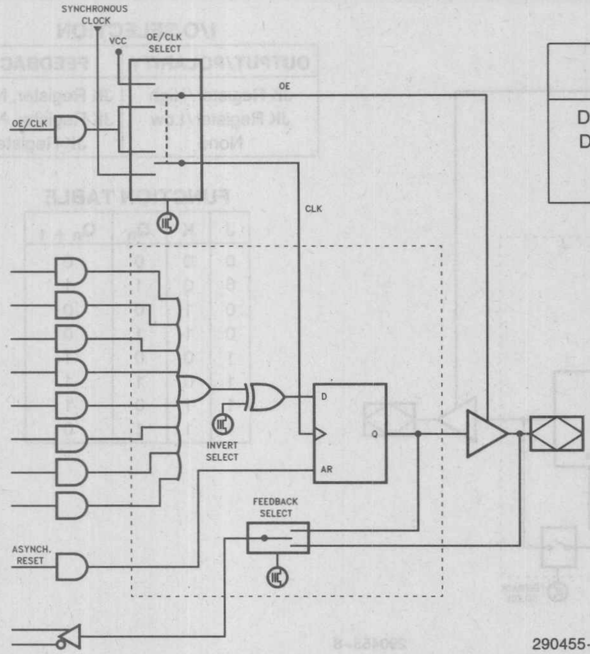
Any I/O pin may be configured as a dedicated input by selecting no output and pin feedback through the appropriate multiplexers.



I/O SELECTION

OUTPUT/POLARITY	FEEDBACK
Combinatorial/High	Pin, None
Combinatorial/Low	Pin, None
None	Pin

Figure 4a. Combinatorial I/O Configuration



I/O SELECTION

OUTPUT/ POLARITY	FEEDBACK
D-Register/High	D-Register, Pin, None
D-Register/Low	D-Register, Pin, None
None	D-Registered
None	Pin

FUNCTION TABLE

D	Q_n	Q_{n+1}
0	0	0
0	1	0
1	0	1
1	1	1

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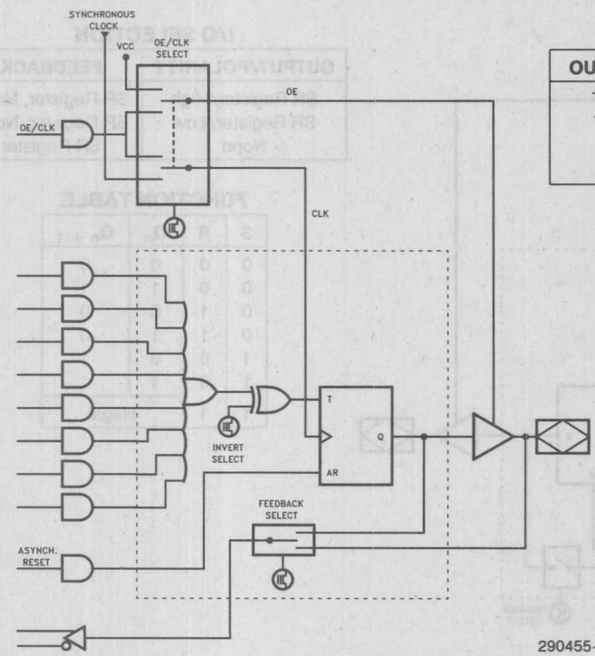
Figure 4b. D-Type Flip-Flop Register Configuration



I/O SELECTION

OUTPUT/POLARITY	FEEDBACK
T-Register/High	T-Register, Pin, None
T-Register/Low	T-Register, Pin, None
None	T-Register
None	Pin

FUNCTION TABLE

T	Q_n	Q_{n+1}
0	0	0
0	1	1
1	0	1
1	1	0

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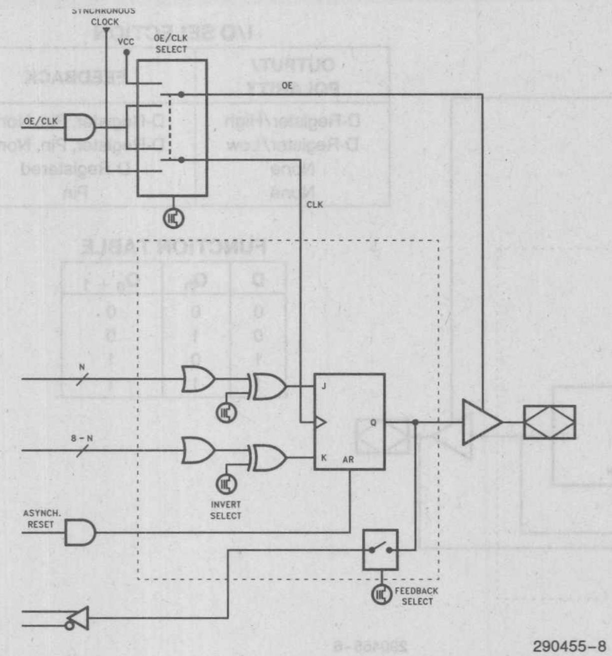
Figure 4c. Toggle Flip-Flop Register Configuration



I/O SELECTION

OUTPUT/POLARITY	FEEDBACK
JK Register/High	JK Register, None
JK Register/Low	JK Register, None
None	JK Register

FUNCTION TABLE

J	K	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

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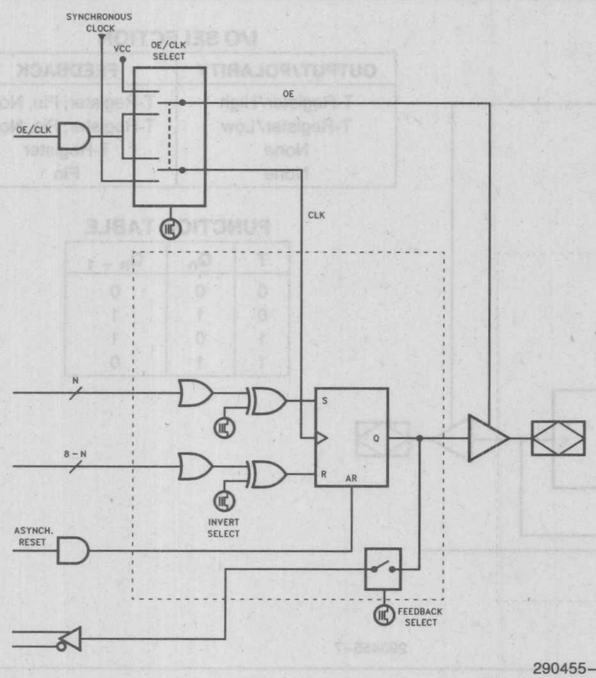
Figure 4d. JK Flip-Flop Register Configuration



I/O SELECTION

OUTPUT/POLARITY	FEEDBACK
SR Register/High	SR Register, None
SR Register/Low	SR Register, None
None	SR Register

FUNCTION TABLE

S	R	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	Illegal	

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Figure 4e. SR Flip-Flop Register Configuration

Output Enable (OE)/Clock Selection

Two modes of operation are provided by the OE/CLK Select Multiplexer as a part of each Macrocell. One mode provides for three-state buffering of outputs while in the other mode, the outputs are always enabled. The operation of the OE/CLK Select Multiplexer sets the mode within a given Macrocell. Therefore, the output mode can be selected individually on every output. Figure 5 illustrates the two modes of OE/CLK operation.

MODE 0: THREE-STATE BUFFERING

In Mode 0, the three-state output buffer is controlled by a single product term originating from the AND array. The output is enabled when the product term is a logical true. Conversely, the output appears as high impedance when the product term is a logical false as shown in Table 1. In Mode 0, the Macrocell Flip-Flop is connected to its associated synchronous clock (either CLK1 or CLK2 depending upon the Macrocell's location within the device). Thus, the Macrocell Flip-Flop may be clocked by its respective synchronous clock but its output will not become valid until the output is enabled.

Table 1. Mode 0 Output Selection

Product Term	Output Buffer
FALSE	Three-State
TRUE	Enabled

MODE 1: OUTPUT BUFFER ENABLED

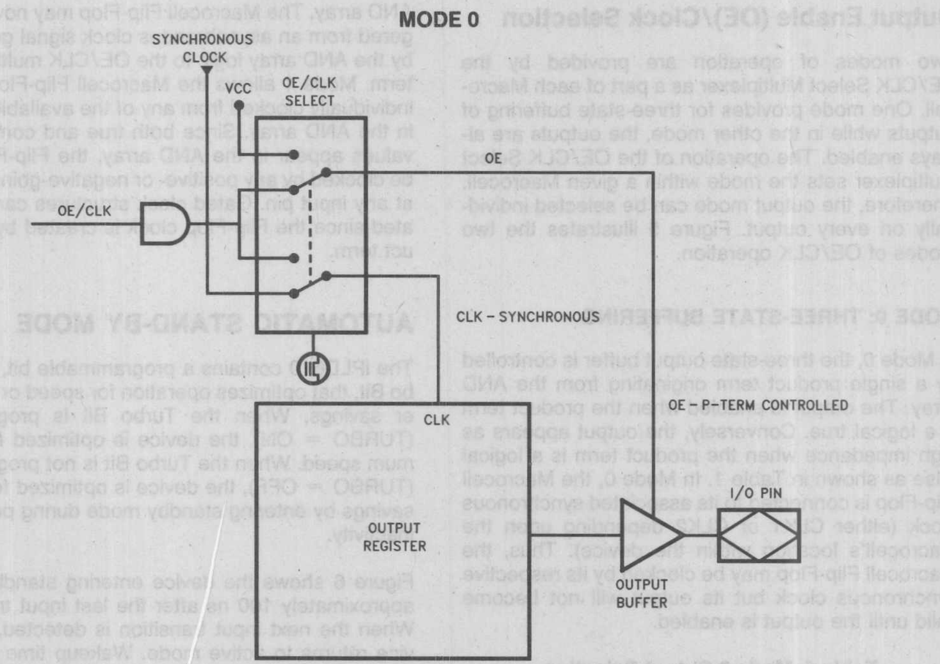
In Mode 1, the Output Buffer is always enabled. In addition, the Macrocell Flip-Flop is connected to the AND array. The Macrocell Flip-Flop may now be triggered from an asynchronous clock signal generated by the AND array logic to the OE/CLK multiplexable term. Mode 1 allows the Macrocell Flip-Flops to be individually clocked from any of the available signals in the AND array. Since both true and complement values appear in the AND array, the Flip-Flop may be clocked by any positive- or negative-going signals at any input pin. Gated clock structures can be created since the Flip-Flop clock is created by a product term.

AUTOMATIC STAND-BY MODE

The iPLD610 contains a programmable bit, the Turbo Bit, that optimizes operation for speed or for power savings. When the Turbo Bit is programmed (TURBO = ON), the device is optimized for maximum speed. When the Turbo Bit is not programmed (TURBO = OFF), the device is optimized for power savings by entering standby mode during periods of inactivity.

Figure 6 shows the device entering standby mode approximately 100 ns after the last input transition. When the next input transition is detected, the device returns to active mode. Wakeup time adds an additional 25 ns to the propagation delay through the device as measured from the first input. No delay will occur if an output is dependent on more than one input and the last of the inputs changes after the device has returned to active mode.

After erasure, the Turbo Bit is unprogrammed (OFF); automatic standby mode is enabled. When the Turbo Bit is programmed (ON), the device never enters standby mode.



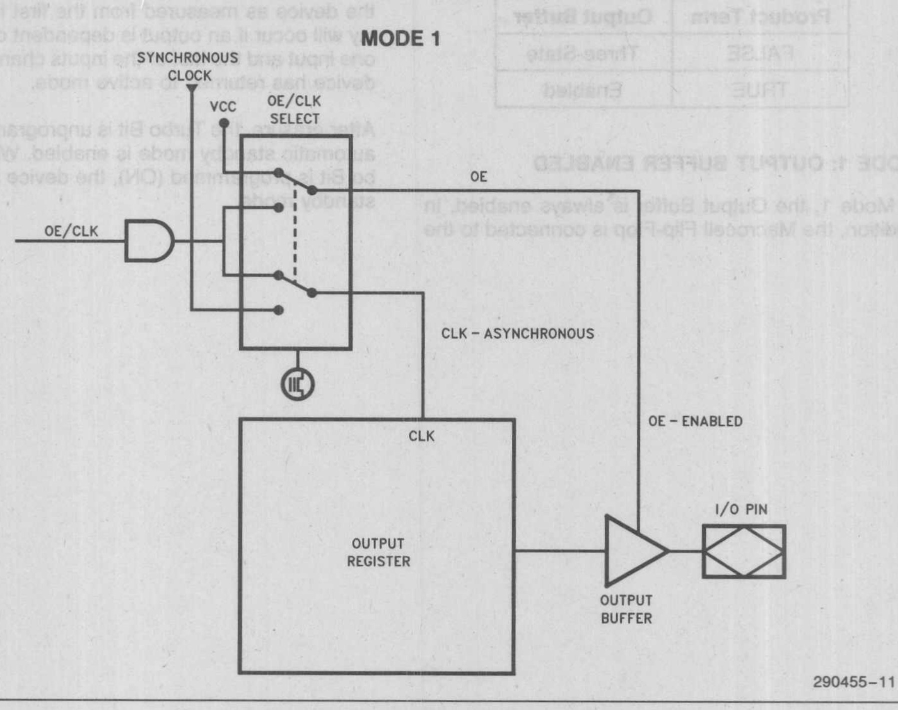


Figure 5. Output Enable/Clock Configuration

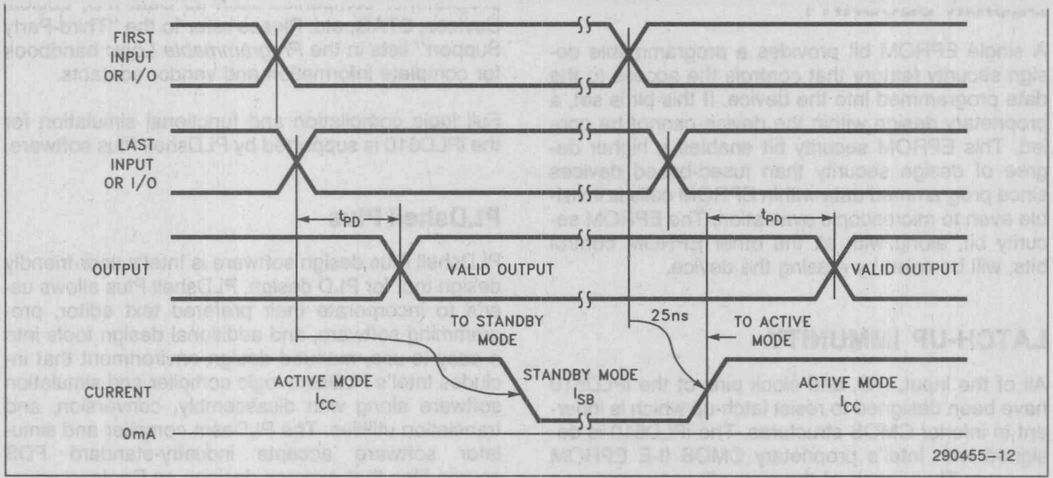


Figure 6. iPLD610 Standby and Active Mode Transitions

Erased-State Configuration

Prior to programming, the I/O structure is configured for combinatorial active low output with input (pin) feedback.

PROGRAMMING CHARACTERISTICS

Initially, all the EPROM control bits of the iPLD610 are connected (in the "1" state). Each of the connected control bits are selectively disconnected by programming the EPROM cells into their "0" state. Programming voltage and waveform specifications are available by request from Intel to support programming of the iPLD610.

Intelligent Programming Algorithm

The iPLD610 supports the Intelligent Programming Algorithm which rapidly programs Intel PLDs using an efficient and reliable method. This method ensures reliability as the incremental program margin of each bit is continually monitored to determine when the bit has been successfully programmed.

FUNCTIONAL TESTING

Since the logical operation of the iPLD610 is controlled by EPROM elements, the device is completely testable. Each programmable EPROM bit controlling the internal logic is tested using application-independent test program patterns. After testing, the devices are erased before shipment to customers. No post-programming tests of the EPROM array are required.

The testability and reliability of EPROM-based programmable logic devices is an important feature over similar devices based on fuse technology. Fuse-based programmable logic devices require a user to perform post-programming tests to insure proper programming. These tests must be done at the device level because of the cummulative error effect. For example, a board containing ten devices each possessing a 2% device fallout translates into an 18% fallout at the board level (it should be noted that programming fallout of fuse-based programmable logic devices is typically 2% or higher).

DESIGN RECOMMENDATIONS

For proper operation, it is recommended that all input and output pins be constrained to the voltage range GND < (V_{IN} or V_{OUT}) < V_{CC}. Unused inputs and I/Os should be tied to V_{CC} or GND to minimize device power consumption. Reserved pins (as indicated in the logic compiler REPORT file) should be left floating (no connect) so that the pin can attain the appropriate logic level. A power supply decoupling capacitor of at least 0.2 μF must be connected directly between V_{CC} and GND pins of the device.

As with all CMOS devices, ESD handling procedures should be used with the iPLD610 to prevent damage to the device during programming, assembly, and test.

DESIGN SECURITY

A single EPROM bit provides a programmable design security feature that controls the access to the data programmed into the device. If this bit is set, a proprietary design within the device cannot be copied. This EPROM security bit enables a higher degree of design security than fused-based devices since programmed data within EPROM cells is invisible even to microscopic evaluation. The EPROM security bit, along with all the other EPROM control bits, will be reset by erasing the device.

LATCH-UP IMMUNITY

All of the input, I/O, and clock pins of the iPLD610 have been designed to resist latch-up which is inherent in inferior CMOS structures. The iPLD610 is designed with Intel's proprietary CMOS II-E EPROM process. Thus, each of the pins will not experience latch-up with currents up to ±100 mA and voltages ranging from −1V to (V_{CC} + 1V). Furthermore, the programming pin is designed to resist latch-up to the 13.5V maximum device limit.

DEVELOPMENT SOFTWARE

Third Party Support

The iPLD610 is supported by third-party logic compilers such as ABEL*, CUPL*, PLDesigner*, Log/IC, etc. Programming support is provided by third-party programmer companies such as Data I/O, Logical Devices, STAG, etc. Please refer to the "Third-Party Support" lists in the *Programmable Logic* handbook for complete information and vendor contacts.

Full logic compilation and functional simulation for the iPLD610 is supported by PLDshell Plus software.

PLDshell Plus

PLDshell Plus design software is Intel's user-friendly design tool for PLD design. PLDshell Plus allows user's to incorporate their prefered text editor, programming software, and additional design tools into a easy-to-use, menued design environment that includes Intel's PLDasm logic compiler and simulation software along with disassembly, conversion, and translation utilities. The PLDasm compiler and simulator software accepts industry-standard PDS source files that express designs as Boolean equations, truth tables, or state machines. On-line help, datasheet briefs, technical notes, and error message information, along with waveform viewing/printing capability make the design task as easy as possible. PLDshell Plus software is available from Intel Literature channels or from your local Intel sales representative.

Tools that support schematic capture and timing simulation for the iPLD610 are available. Please refer to the "Development Tools" section of the Programmable Logic handbook.

*ABEL is a trademark of Data I/O Corp. CUPL is a trademark of Logical Devices, Inc. PLDesigner is a trademark of MINC, Inc. Log/IC is a trademark of ISDATA, Corporation.

ADF PRIMITIVES SUPPORTED

The following ADF primitives are supported by this device:

INP	JOJF
CONF	JONF
COIF	SONF
RONF	SOSF
RORF	TOIF
ROIF	TONF
NORF	TOTF
NOJF	CLKB
NOSF	
NOTF	

ORDERING INFORMATION

f_{CNT1} (MHz)	f_{CNT2} (MHz)	t_{PD} (ns)	Order Code	Package	Operating Range
74	100	10	P PLD610-10	PDIP	Commercial
			N PLD610-10	PLCC	Commercial
			DPLD610-10	*CerDIP	Commercial
50	66	15	P PLD610-15	PDIP	Commercial
			N PLD610-15	PLCC	Commercial
			DPLD610-15	*CerDIP	Commercial
			TDPLD610-15	*CerDIP	Industrial
			TNPLD610-15	PLCC	Industrial
40	40	25	P PLD610-25	PDIP	Commercial
			N PLD610-25	PLCC	Commercial
			DPLD610-25	*CerDIP	Commercial

*Windowed CerDIP package allows UV erase.

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ABSOLUTE MAXIMUM RATINGS*

Symbol	Parameter	Min	Max	Units
V_{CC}	Supply Voltage(1)	−2.0	7.0	V
V_{PP}	Programming Supply Voltage(1)	−2.0	13.5	V
V_I	DC Input Voltage(1)(2)	−0.5	V_{CC} + 0.5	V
t_{stg}	Storage Temperature	−65	+150	°C
t_{amb}	Ambient Temperature(3)	−10	+85	°C

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

***WARNING:** *Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

NOTES:
1. Voltages with respect to ground.
2. Minimum DC input is −0.5V. During transitions, the inputs may undershoot to −2.0V or overshoot to +7.0V for periods less than 20 ns under no load conditions.
3. Under bias. Extended temperature versions are also available.

RECOMMENDED OPERATING CONDITIONS

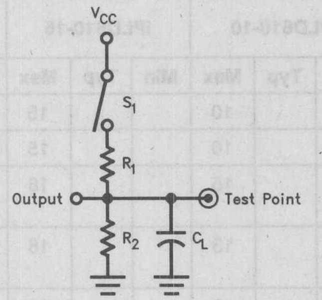
Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage	4.75	5.25	V
V_{IN}	Input Voltage	0	V_{CC}	V
V_O	Output Voltage	0	V_{CC}	V
T_A	Operating Temperature	0	+70	°C
t_R	Input Rise Time		500	ns
t_F	Input Fall Time		500	ns

D.C. CHARACTERISTICS $T_A = 0°C$ to $70°C$, $V_{CC} = 5.0V \pm 5\%$

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
V_{IH}(4)	HIGH Level Input Voltage	2.0		V_{CC} + 0.3	V	
V_{IL}(4)	LOW Level Input Voltage	−0.3		0.8	V	
V_{OH}	HIGH Level Output Voltage	2.4			V	$I_O = -4.0$ mA DC, V_{CC} = Min.
V_{OL}(5)	LOW Level Output Voltage			0.45	V	$I_O = 12.0$ mA DC, V_{CC} = Min.
I_I	Input Leakage Current	−10		10	μA	V_{CC} = Max., GND < V_{IN} < V_{CC}
I_{OZ}	Output Leakage Current	−10		10	μA	V_{CC} = Max., GND < V_{OUT} < V_{CC}
I_{SC}(6)	Output Short Circuit Current	−30		−120	mA	V_{CC} = Max., V_{OUT} = 0.5V
I_{SB}(7)	Standby Current		20	150	μA	V_{CC} = Max., V_{IN} = V_{CC} or GND, Standby Mode
I_{CC}	Power Supply Current (See I_{CC} vs. Freq. Graph)		3	8	mA	V_{CC} = Max, V_{IN} = V_{CC} or GND, No Load, f_{IN} = 1 MHz, Device Prog. as 16-Bit Counter, Turbo = Off
			65	105	mA	Turbo = On, f_{IN} = 1 MHz
I_{CCI}	Industrial Temperature Power Supply Current			150	mA	Turbo = On, f_{IN} = 1 MHz

NOTES:
4. Absolute values with respect to device GND; all over and undershoots due to system or tester noise are included.
5. Maximum DC I_{OL} for the device is 64 mA for CLK1 group I/O. 1–I/O.8 and 64 mA for CLK2 group I/O.9–I/O16.
6. Not more than 1 output should be tested at a time. Duration of that test must not exceed 1 second.
7. In Non-Turbo Mode (TURBO = OFF), device enters standby mode approximately 75 ns after the last input transition. I_{SB} is measured with the window covered (CerDIP).

SWITCHING TEST CIRCUIT



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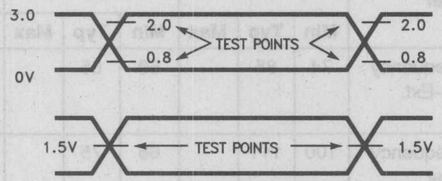
Specification	S_1	C_L	Commercial R_1	Commercial R_2	Measured Output Value
t_{PD}	Closed	30 pF			1.5V
t_{PZX}	Z → H: Open Z → L: Closed	30 pF	200Ω	330Ω	1.5V
t_{PXZ}	H → Z: Open L → Z: Closed	5 pF			H → Z: V_{OH} − 0.5V L → Z: V_{OL} + 0.5V

A.C. TESTING INPUT, OUTPUT WAVEFORM



290455–14

A.C. Testing: Inputs are Driven at 3.0V for a Logic "1" and 0V for a Logic "0". Timing Measurements are made at 2.0V for a Logic "1" and 0.8V for a Logic "0" on inputs. Outputs are measured at a 1.5V point. Device input rise and fall times are less than 3 ns.

CAPACITANCE (T_A = 0°C to +70°C; V_{CC} = 5.0V ±5%)[8]

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
C_{IN}	Input Capacitance		5	8	pF	V_{IN} = 0V, f = 1.0 MHz
C_{IO}	I/OCapacitance		6	8	pF	V_{OUT} = 0V, f = 1.0 MHz
C_{CLK}	CLK Capacitance		8	10	pF	V_{IN} = 0V, f = 1.0 MHz
C_{VPP}	V_{PP} Pin Capacitance		10	12	pF	V_{PP} on CLK2, f = 1.0 MHz

NOTE:
8. These values are evaluated during initial characterization and whenever design modifications occur that may affect capacitance.

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COMBINATORIAL MODE A.C. CHARACTERISTICS

(T_A = 0°C to +70°C, V_{CC} = 5.0V ±5%)(9)

Symbol	Parameter	iPLD610-10			iPLD610-15			iPLD610-25			Non-Turbo(10) Mode	Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
t_{PD1}(11)	Input to Output Valid			10			15			25	+25	ns
t_{PD2}(11)	I/O to Output Valid			10			15			25	+25	ns
t_{PZX}(12)	Input or I/O to Output Enable			15			18			25	+25	ns
t_{PXZ}(12)	Input or I/O to Output Disable			13			18			25	+25	ns
t_{CLR}	Input or I/O to Asynch. Reset			13			18			25	+25	ns

NOTES:
9. Typical values are at T_A = 25°C, V_{CC} = 5V, Active Mode.
10. If device is operated in Non-Turbo Mode (TURBO = OFF), and the device is inactive for approx. 75 ns, increase time by amount shown.
11. Measured with eight outputs switching. See t_{PD} vs. Number of Outputs Switching graph.
12. t_{PZX} and t_{PXZ} are measured at ±0.5V from steady state voltage as driven by spec. output load.
13. Measured with device configured as a 16-bit counter.

REGISTER MODE—SYNCHRONOUS CLOCK A.C. CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = 5.0V ±5%(9)

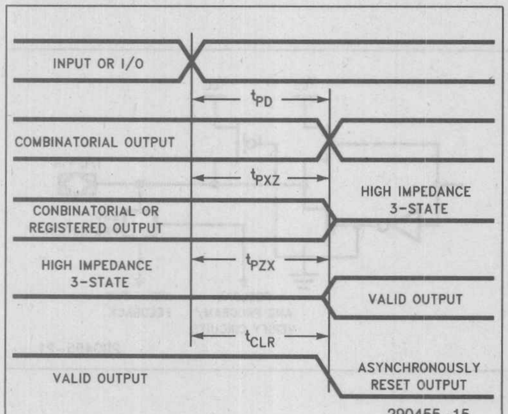
Symbol	Parameter	iPLD610-10			iPLD610-15			iPLD610-25			Non-Turbo(10) Mode	Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
f_{CNT1}(13)	Max. Counter Frequency 1/(t_{SU} + t_{CO1})—Ext. Feedback	74	85		50	66		40	50			MHz
f_{CNT2}(13)	Max. Counter Frequency 1/(t_{CNT})—Internal Feedback	100	111		66	75		40	66			MHz
f_{MAX}	Max. Frequecy (Pipelined) 1/(t_{CP})—No Feedback	111	120		83.3	100		66	80			MHz
t_{SU}	Input or I/O Setup Time to CLK	7			12			15			+25	ns
t_H	Input or I/O Hold Time from CLK	0			0			0				ns
t_{CO1}(13)	CLK High to Output Valid			6.5			8			10		ns
t_{CO2}	CLK High to Output Valid Fed through Comb. Macrocell			14			20			30	+25	ns
t_{CNT}(13)	Macrocell Output Feedback to Macrocell Input—Internal Path			10			15			25	+25	ns
t_{CL}	CLK Low Time	4			5			6				ns
t_{CH}	CLK High Time	4			5			6				ns
t_{CP}	CLK Period	9			12			15				ns

REGISTER MODE—ASYNCHRONOUS CLOCK A.C. CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = 5.0V ±5%(9)

Symbol	Parameter	iPLD610-10			iPLD610-15			iPLD610-25			Non-Turbo(10) Mode	Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
f_{ACNT1}(13)	Max. Counter Frequency $1/(t_{ASU} + t_{ACO1})$—Ext. Feedback	71.4	80		50	66		33.3	40			MHz
f_{ACNT2}(13)	Max. Counter Frequency $1/(t_{ACNT})$—Internal Feedback	100	111		66	75		40	50			MHz
f_{AMAX}	Max. Frequency (Pipelined) $1/(t_{ACP})$—No Feedback	100	111		66	75		50	66			MHz
t_{ASU}	Input or I/O Setup Time to Asynch. CLK	2			4			5			+25	ns
t_{AH}	Input or I/O Hold Time from Asynch. CLK	3			6			8				ns
t_{ACO1}(13)	Asynch. CLK High to Output Valid			12			16			25	+25	ns
t_{ACO2}	Asynch. CLK High to Output Valid Fed through Comb. Macrocell			20			30			45	+25	ns
t_{ACNT}	Macrocell Output Feedback to Macrocell Input—Internal Path			10			15			25	+25	ns
t_{ACL}	Asynch. CLK Low Time	4			6			7				ns
t_{ACH}	Asynch. CLK High Time	4			6			7				ns
t_{ACP}	Asynch. CLK Period	10			15			20				ns

COMBINATORIAL MODE



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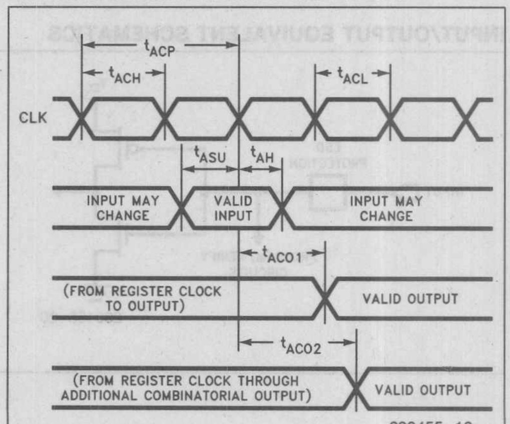
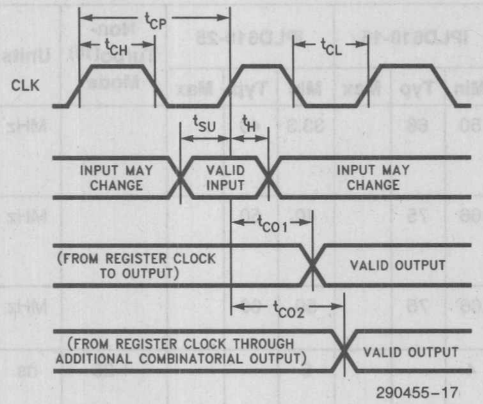
ASYNCHRONOUS REGISTERED MODE

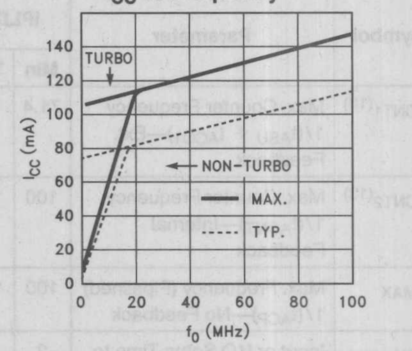


290455-16



290455-17

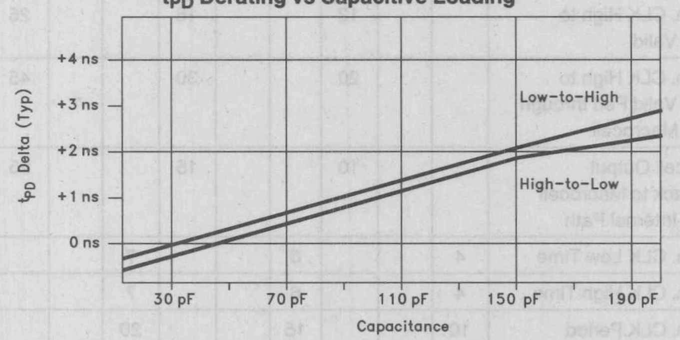
I_{CC} vs Frequency



290455-18

Conditions: $T_A = 0°C$, $V_{CC} = 5.25V$

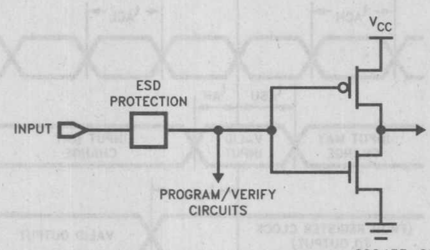
t_{PD} Derating vs Capacitive Loading



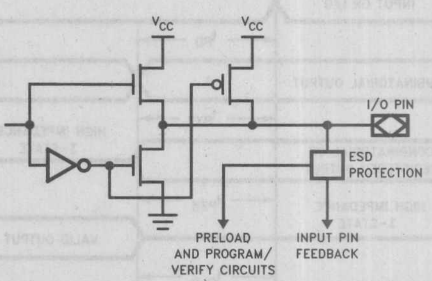
290455-19

Conditions: $T_A = +70°C$; $V_{CC} = 4.75V$

INPUT/OUTPUT EQUIVALENT SCHEMATICS

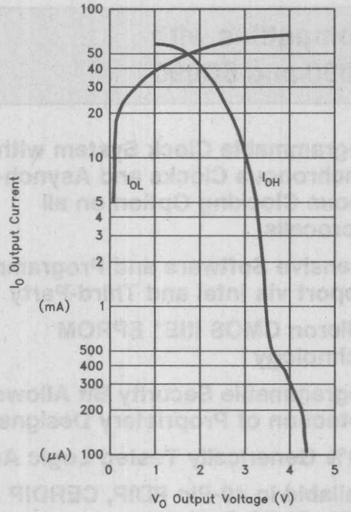


290455-20



290455-21

iPLD610 Output Current in Relation to Voltage

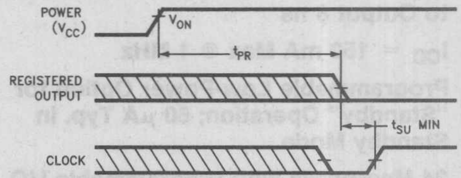


290455-22

CONDITIONS:
$T_A = +80°C$
$V_{CC} = 4.75V$

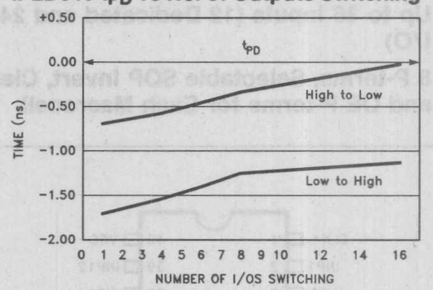
Symbol	Parameter	Value
t_{PR}	Power-Up Reset	1000 ns Max.
V_{ON}	Turn-On Voltage	4.75V

POWER-UP RESET



290455-23

iPLD610 t_{PD} vs No. of Outputs Switching



290455-24

CONDITIONS:
$T_A = 70°C, V_{CC} = 4.75V, C_L = 30\ pF$

Power-Up Reset

Internal power-up reset circuits ensure that all flip-flops will be reset to a logic 0 after the device has powered up. Because V_{CC} rise can vary significantly from one application to another, V_{CC} rise must be monotonic.

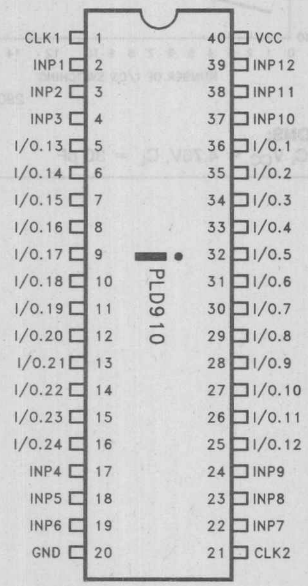
2

intel®

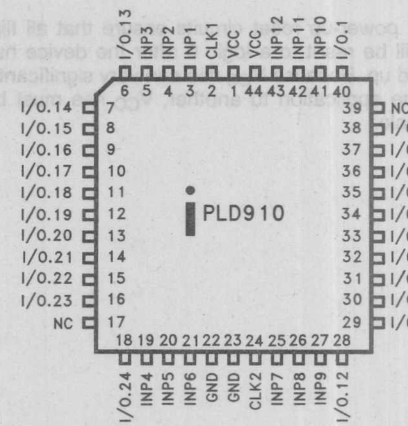
iPLD910
FAST 24-MACROCELL CMOS PLD

Function, Pin, and JEDEC Compatible with EP900, EP910, EP910A, 85C090 and 5C090

- **t_{PD} 12 ns, 62.5 MHz w/Feedback, Clock to Output 8 ns**
- **I_{CC} = 150 mA Max @ 1 MHz**
- **Programmable Low-Power Option for "Standby" Operation; 60 μA Typ. in Standby Mode**
- **24 Macrocells with Programmable I/O Architecture (Register/Combinatorial). Registers Configurable as D/T/JK/RS Types**
- **Up to 36 Inputs (12 Dedicated and 24 I/O)**
- **8 P-terms, Selectable SOP Invert, Clear and OE P-terms for Each Macrocell**
- **Programmable Clock System with 2 Synchronous Clocks and Asynchronous Clocking Option on all Macrocells**
- **Extensive Software and Programming Support via Intel and Third-Party Tools**
- **1-Micron CMOS IIIE* EPROM Technology**
- **Programmable Security Bit Allows Total Protection of Proprietary Designs**
- **100% Generically Tested Logic Array**
- **Available in 40-Pin PDIP, CERDIP and 44-Pin PLCC Packages**
  (See Packaging Spec., Order Number 240800, Package Type N and P)



290456-1



290456-2

Figure 1. iPLD910 Pinout Diagrams

September 1993
Order Number: 290456-002

INTRODUCTION

The iPLD910 is a high-performance, high-integration, general-purpose CMOS PLD. The iPLD910 PLD (Programmable Logic Device) accommodates logic functions with up to 36 inputs and 24 I/O macrocells. Each I/O macrocell includes 8 product-terms (p-terms) for input, a separate clear p-term, and an output enable/asynchronous clock p-term. With a maximum external frequency of 62.5 MHz, the iPLD910 is well suited to high-performance microprocessor-based systems. The iPLD910 is pin- and function-compatible with the EP900, EP910, EP910A, 85C090 and 5C090.

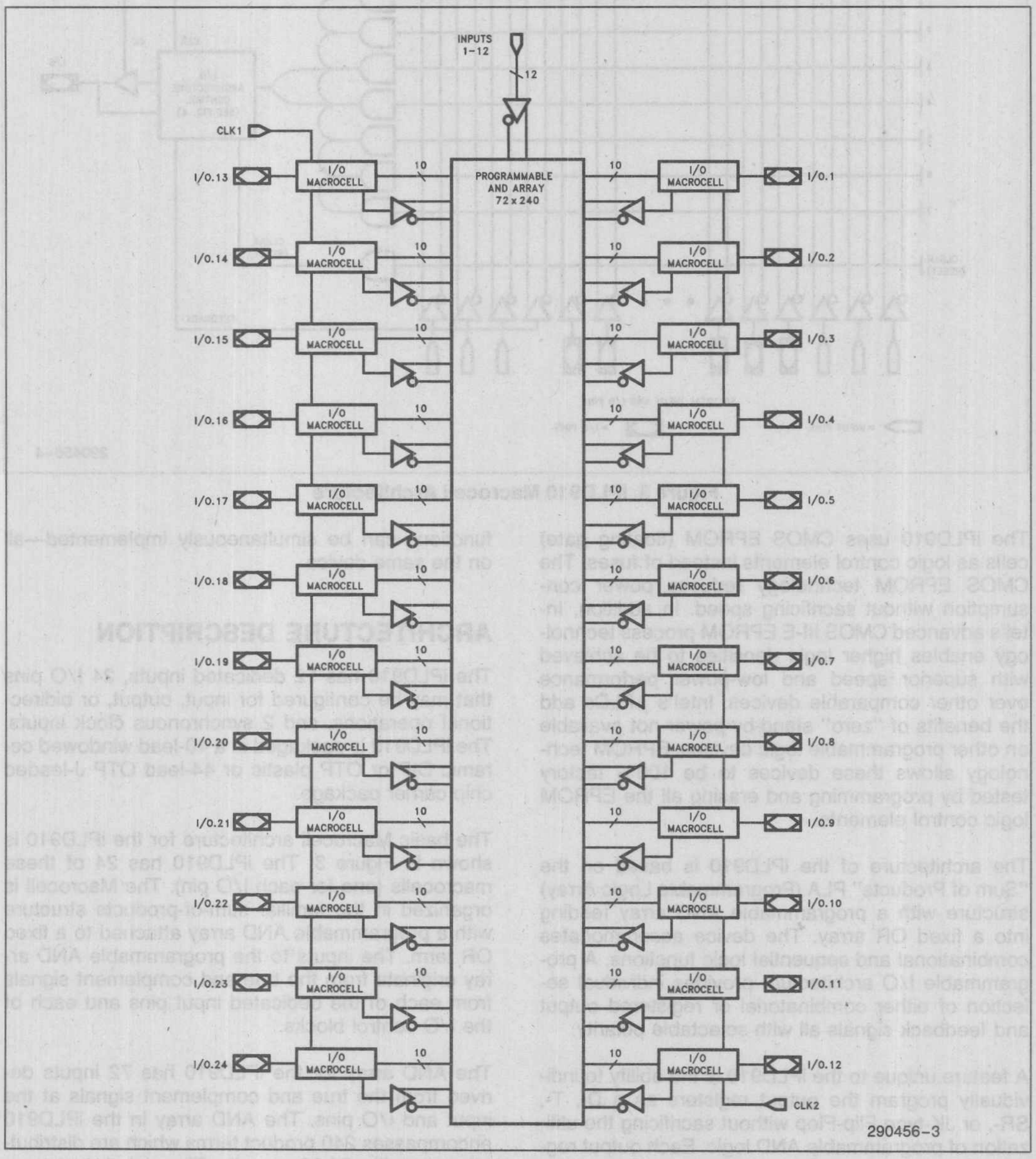


Figure 2. iPLD910 Global Architecture

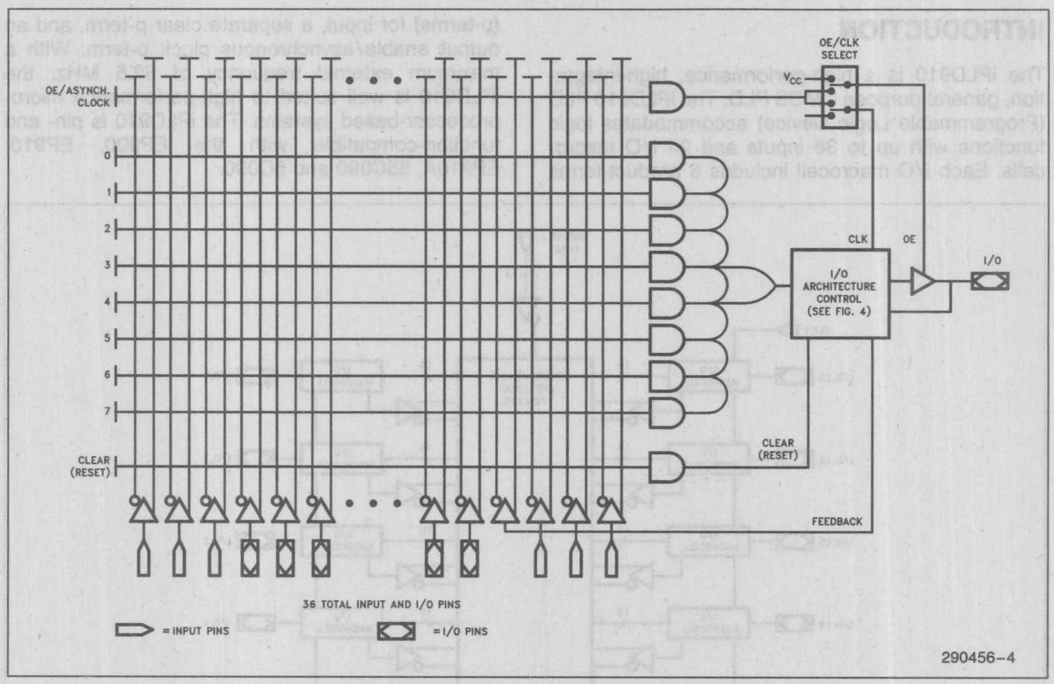


Figure 3. iPLD910 Macrocell Architecture

The iPLD910 uses CMOS EPROM (floating gate) cells as logic control elements instead of fuses. The CMOS EPROM technology reduces power consumption without sacrificing speed. In addition, Intel's advanced CMOS III-E EPROM process technology enables higher logic densities to be achieved with superior speed and low-power performance over other comparable devices. Intel's μPLDs add the benefits of "zero" stand-by power not available on other programmable logic devices. EPROM technology allows these devices to be 100% factory tested by programming and erasing all the EPROM logic control elements.

The architecture of the iPLD910 is based on the "Sum of Products" PLA (Programmable Logic Array) structure with a programmable AND array feeding into a fixed OR array. The device accommodates combinational and sequential logic functions. A programmable I/O architecture provides individual selection of either combinatorial or registered output and feedback signals all with selectable polarity.

A feature unique to the iPLD910 is the ability to individually program the output registers as a D-, T-, SR-, or JK-type Flip-Flop without sacrificing the utilization of programmable AND logic. Each output register can be individually clocked from any of the input or feedback paths available within the AND array. With these features, a wide variety of logic functions can be simultaneously implemented—all on the same device.

ARCHITECTURE DESCRIPTION

The iPLD910 has 12 dedicated inputs, 24 I/O pins that may be configured for input, output, or bidirectional operations, and 2 synchronous clock inputs. The iPLD910 is packaged in a 40-lead windowed ceramic DIP or OTP plastic or 44-lead OTP J-leaded chip carrier package.

The basic Macrocell architecture for the iPLD910 is shown in Figure 3. The iPLD910 has 24 of these macrocells (one for each I/O pin). The Macrocell is organized in the familiar sum-of-products structure with a programmable AND array attached to a fixed OR term. The inputs to the programmable AND array originate from the true and complement signals from each of the dedicated input pins and each of the I/O control blocks.

The AND array for the iPLD910 has 72 inputs derived from the true and complement signals at the input and I/O pins. The AND array in the iPLD910 encompasses 240 product terms which are distributed among the 24 Macrocells. The global device architecture is shown in Figure 2.

Each Macrocell contains ten product terms. Eight of the ten product terms (AND gates) are dedicated for SOP logic implementation. One product term on each Macrocell is used for RESET control to the output register associated with the Macrocell. The final product term is used for OE/Asynchronous Clock implementation.

Within the AND array, there is an EPROM connection at every intersection of an input signal (true and complement) and a product term to a given Macrocell. Before programming an erased device, every EPROM connection is made at every intersection. But during the programming process, these connections are opened so that only the desired connections remain. Therefore, the true or complement of any input signal can be connected to any product term. If both the true and complement connections of any signal are left intact, a logical false results on the output of the AND gate. However, if both the true and complement connections are open, then a logic "don't care" results on the AND gate. Lastly, if all the inputs of a product term are programmed open, then a logical true results on the output of the AND gate.

The iPLD910 has two dedicated clock inputs to provide synchronous clock signals to the internal registers. Each of the clock signals controls half the total registers within the given device. For example, CLK1 provides synchronous clocking to the registers in Macrocells in the left half of the array while CLK2 controls the registers associated with Macrocells in the right half of the array. The advanced I/O architecture allows for any number of the registers to be synchronously clocked (from none to all). Both of the dedicated clock inputs latch the data into a given register when triggered on a positive edge.

MACROCELL ARCHITECTURE SELECTION

The iPLD910 architecture provides each Macrocell with over 50 different possible I/O register configurations. Each I/O pin can be configured for combinatorial or registered output (true or complement) with feedback. In addition, four different types of output registers can be implemented on I/O pin without any additional logic requirements. The feedback mechanism for each register back into the AND array can be programmed to provide for either registered feedback from the Macrocell or input feedback (treating the pin as an input). Another advantage of the advanced I/O capability of the iPLD910 is the ability to individually clock each internal register from asynchronous clock signals.

Invert Select EPROM Bit

The Invert Select EPROM bit is used to invert the product term input into the register. This applies to all inputs including double inputs on the JK and SR registers.

REGISTER SELECTION

The advanced I/O architecture of the iPLD910 allows four different register types along with combinatorial output as illustrated in Figure 4a through e. The register types include a T, D, JK, or SR Flip-Flop and each Macrocell I/O structure may be independently configured. In addition, all registers have an individual asynchronous RESET control from a dedicated product term derived in the AND array. When this dedicated product term is a logical one, the Macrocell register is immediately cleared to a logical zero independent of the register clock. The RESET function occurs automatically on power-up.

Output Register Configuration

The four different register types shown in Figure 4 are described below.

D- or T-type Flip-Flops

When either a D- or T-type Flip-Flop is configured as part of the I/O structure, all eight of the product terms into the Macrocell are ORed together and fed into the register input.

JK or SR Registers

When either a JK or SR register is configured, the eight product terms are shared among two OR gates (one for the J or S input and the other for the K or R input). The allocation for these product terms for each of the register inputs is optimized by the PLDshell Plus software.

OUTPUT/FEEDBACK

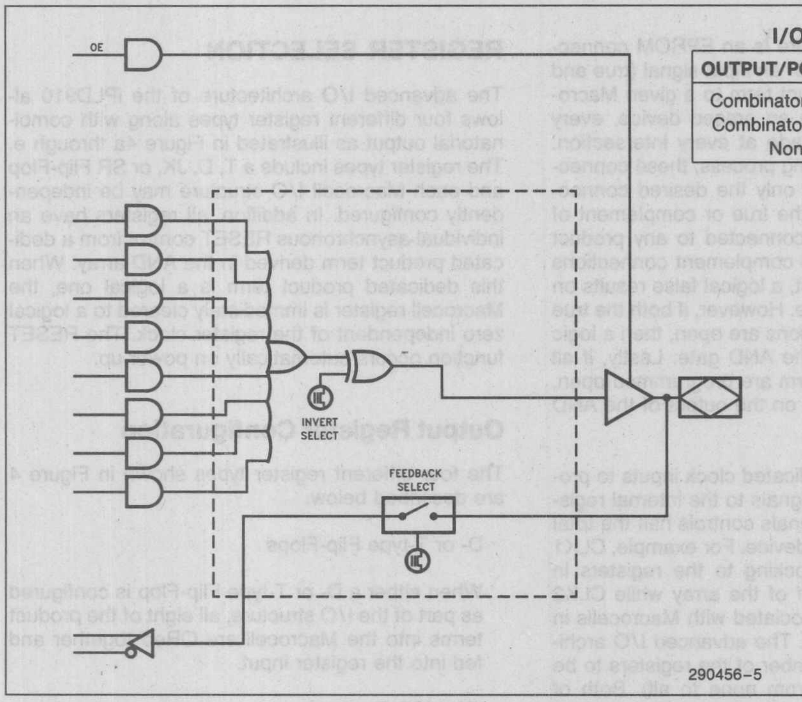
The Output Select Multiplexer allows for either registered, combinatorial or no output.

The Feedback Select Multiplexer EPROM bit enables registered, I/O (using the pin for bidirectional input or just input), or no feedback to the AND array.

The Feedback Select is also important for building equations with more than 8 product terms. The 8-product equations of a Macrocell can be fed back

than 8-inputs). If the feedback product term is not to be used as an output, the associated Macrocell pin should be left floating (no connect) when assembled onto a circuit board.

by selecting no output and pin feedback through the appropriate multiplexers.



I/O SELECTION

OUTPUT/POLARITY	FEEDBACK
Combinatorial/High	Pin, None
Combinatorial/Low	Pin, None
None	Pin (Input)

Figure 4a. Combinatorial I/O Configuration

I/O SELECTION

OUTPUT/ POLARITY	FEEDBACK
D-Register/High	D-Register, Pin, None
D-Register/Low	D-Register, Pin, None
None	D-Registered
None	Pin (Input)

FUNCTION TABLE

D	Q_n	Q_{n+1}
0	0	0
0	1	0
1	0	1
1	1	1

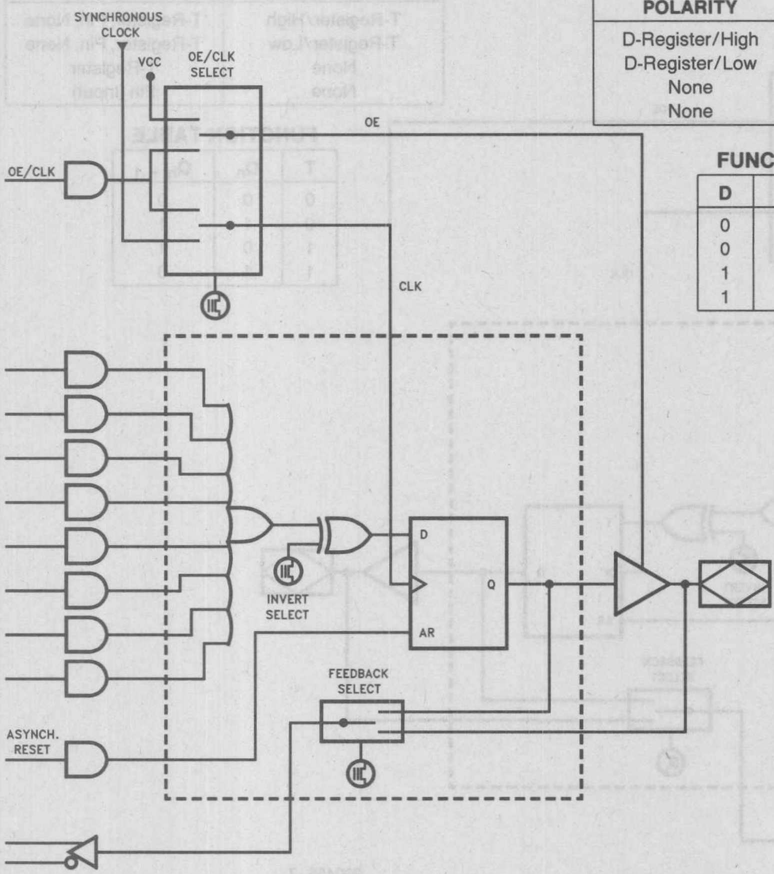
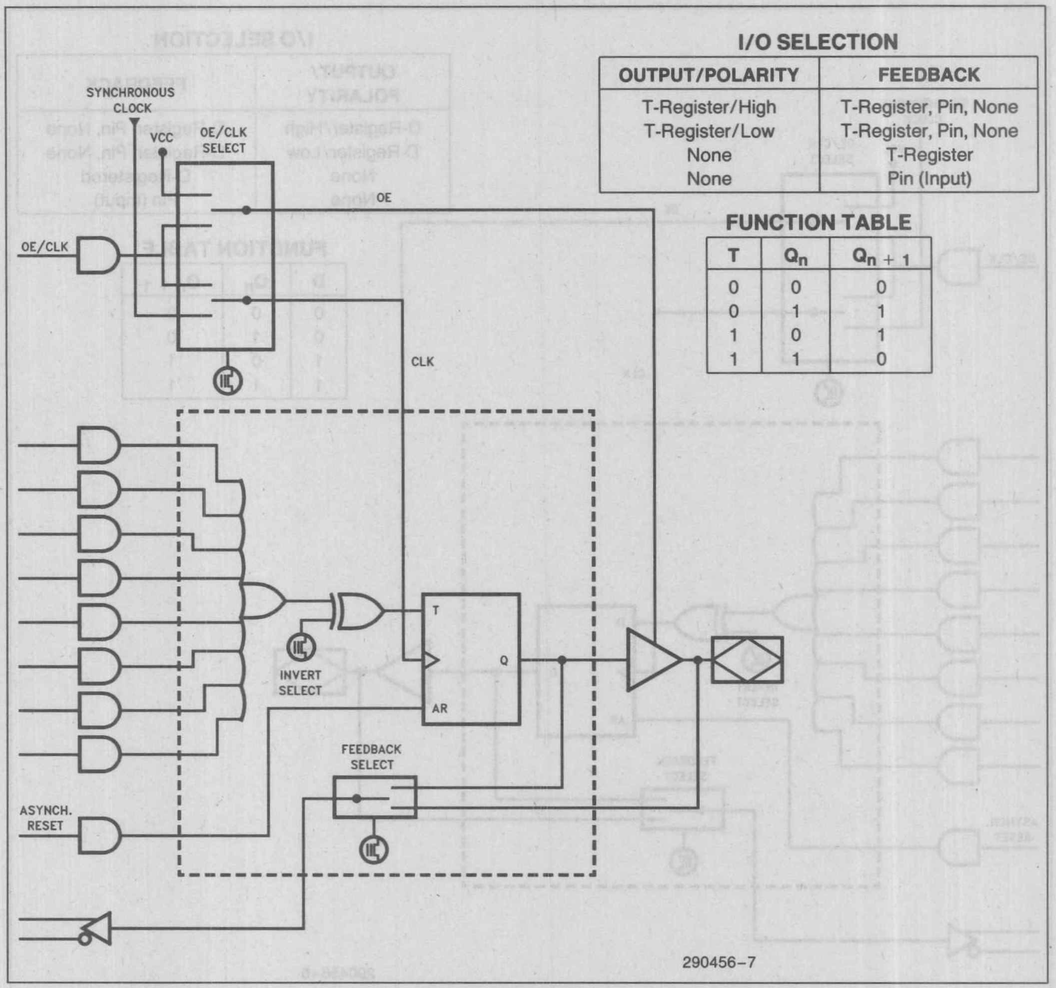


Figure 4b. D-Type Flip-Flop Register Configuration



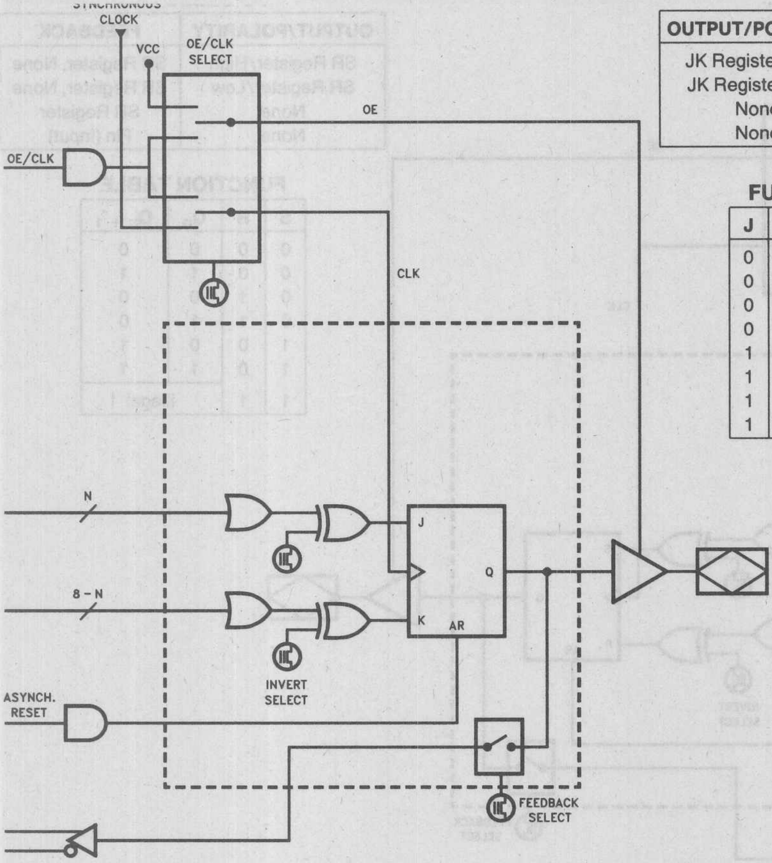
I/O SELECTION

OUTPUT/POLARITY	FEEDBACK
T-Register/High	T-Register, Pin, None
T-Register/Low	T-Register, Pin, None
None	T-Register
None	Pin (Input)

FUNCTION TABLE

T	Q_n	Q_{n+1}
0	0	0
0	1	1
1	0	1
1	1	0

Figure 4c. Toggle Flip-Flop Register Configuration



OUTPUT/POLARITY	FEEDBACK
JK Register/High	JK Register, None
JK Register/Low	JK Register, None
None	JK Register
None	Pin (Input)

FUNCTION TABLE

J	K	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

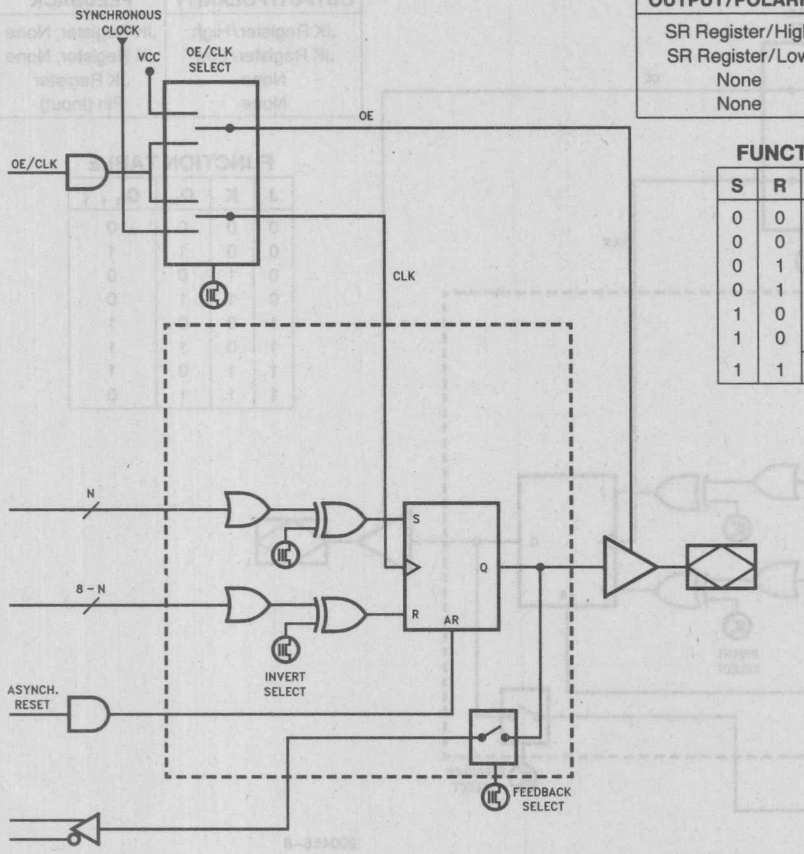
Figure 4d. JK Flip-Flop Register Configuration

I/O SELECTION

OUTPUT/POLARITY	FEEDBACK
SR Register/High	SR Register, None
SR Register/Low	SR Register, None
None	SR Register
None	Pin (Input)

FUNCTION TABLE

S	R	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	Illegal	



290456–9

Figure 4e. SR Flip-Flop Register Configuration

Output Enable (OE)/Clock Selection

Two modes of operation are provided by the OE/CLK Select Multiplexer as a part of each Macrocell. One mode provides for three-state buffering of outputs while in the other mode, the outputs are always enabled. The operation of the OE/CLK Select Multiplexer sets the mode within a given Macrocell. Therefore, the output mode can be selected individually on every output. Figure 5 illustrates the two modes of OE/CLK operation.

MODE 0: THREE-STATE BUFFERING

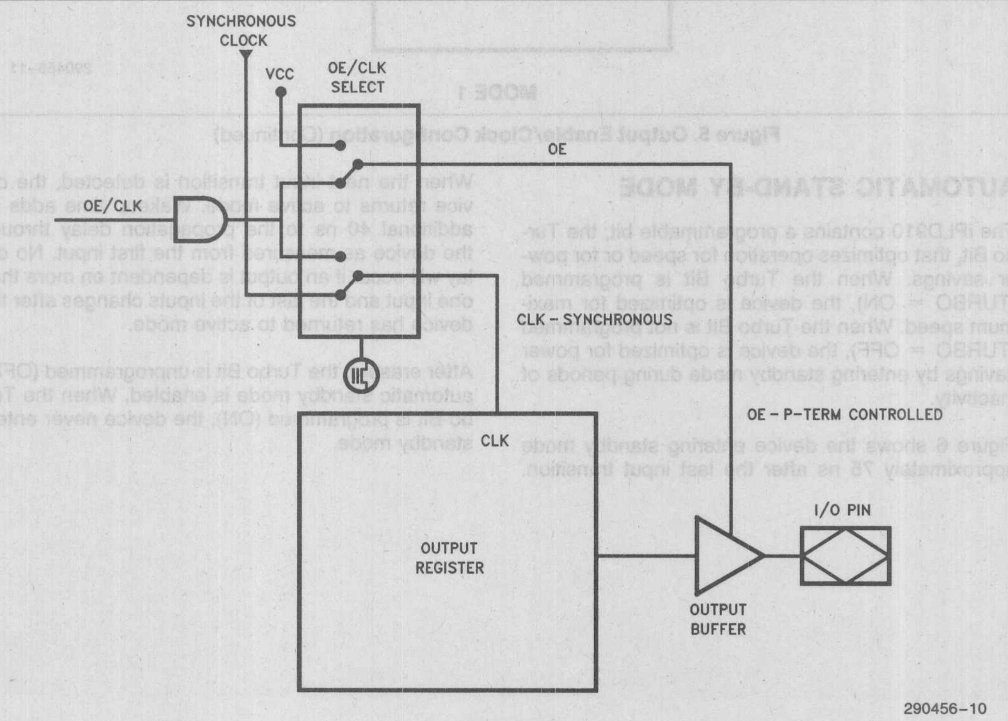
In Mode 0, the three-state output buffer is controlled by a single product term originating from the AND array. The output is enabled when the product term is a logical true. Conversely, the output appears as high impedance when the product term is a logical false as shown in Table 1. In Mode 0, the Macrocell Flip-Flop is connected to its associated synchronous clock (either CLK1 or CLK2 depending upon the Macrocell's location within the device). Thus, the Macrocell Flip-Flop may be clocked by its respective synchronous clock but its output will not become valid until the output is enabled.

Table 1. Mode 0 Output Selection

Product Term	Output Buffer
FALSE	Three-State
TRUE	Enabled

MODE 1: OUTPUT BUFFER ENABLED

In Mode 1, the Output Buffer is always enabled. In addition, the Macrocell Flip-Flop is connected to the AND array. The Macrocell Flip-Flop may now be triggered from an asynchronous clock signal generated by the AND array logic to the OE/CLK multiplexable term. Mode 1 allows the Macrocell Flip-Flops to be individually clocked from any of the available signals in the AND array. Since both true and complement values appear in the AND array, the Flip-Flop may be clocked by positive-or negative-going signals at any input pin. Gated clock structures can be created since the Flip-Flop clock is created by a product term.



MODE 0

Figure 5. Output Enable/Clock Configuration

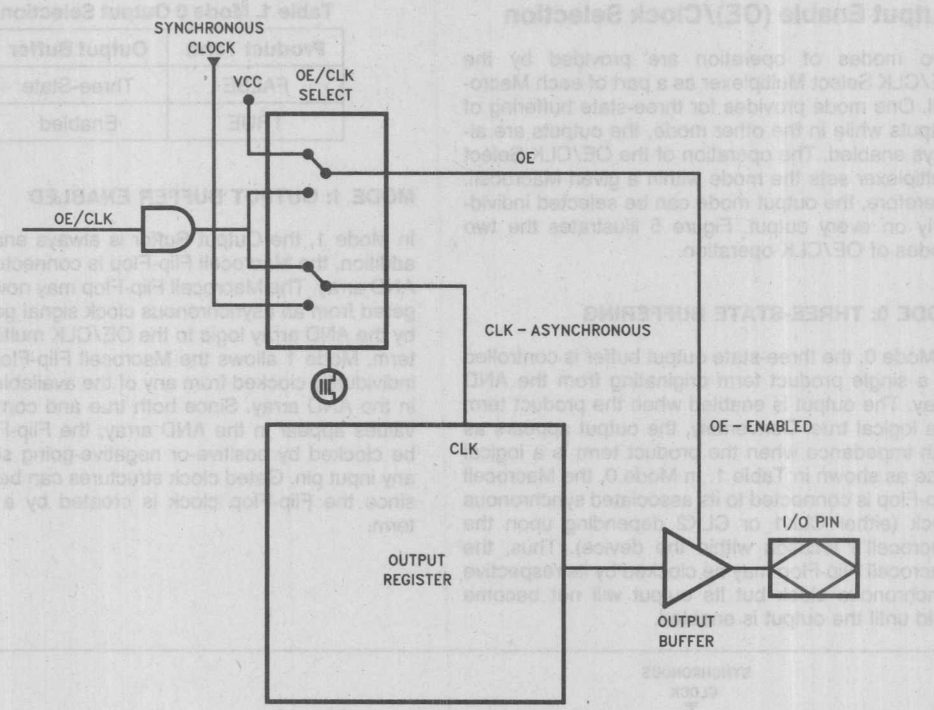


Figure 5. Output Enable/Clock Configuration (Continued)

AUTOMATIC STAND-BY MODE

The iPLD910 contains a programmable bit, the Turbo Bit, that optimizes operation for speed or for power savings. When the Turbo Bit is programmed (TURBO = ON), the device is optimized for maximum speed. When the Turbo Bit is not programmed (TURBO = OFF), the device is optimized for power savings by entering standby mode during periods of inactivity.

Figure 6 shows the device entering standby mode approximately 75 ns after the last input transition. When the next input transition is detected, the device returns to active mode. Wakeup time adds an additional 40 ns to the propagation delay through the device as measured from the first input. No delay will occur if an output is dependent on more than one input and the last of the inputs changes after the device has returned to active mode.

After erasure, the Turbo Bit is unprogrammed (OFF); automatic standby mode is enabled. When the Turbo Bit is programmed (ON), the device never enters standby mode.

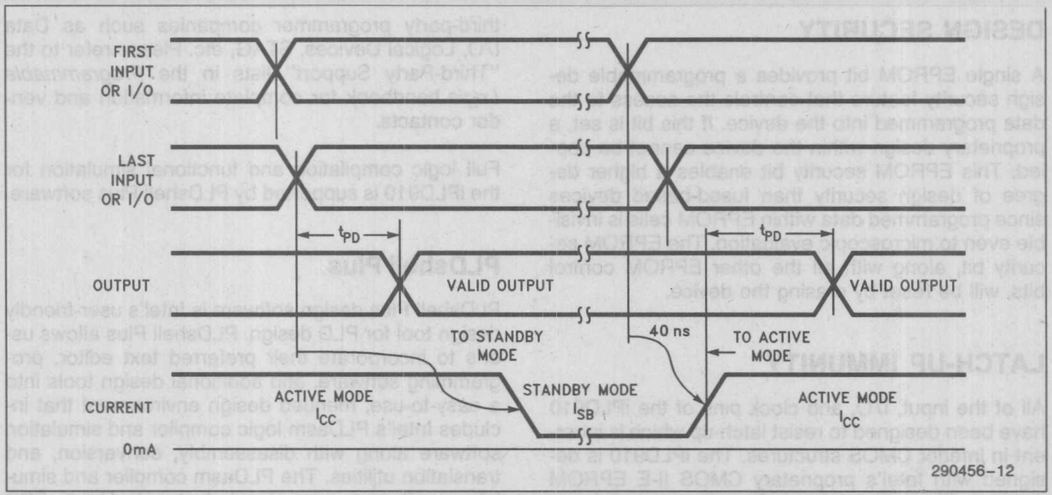


Figure 6. iPLD910 Standby and Active Mode Transitions

Erased-State Configuration

Prior to programming, the I/O structure is configured for combinatorial active low output with input (pin) feedback.

PROGRAMMING CHARACTERISTICS

Initially, all the EPROM control bits of the iPLD910 are connected (in the "1" state). Each of the connected control bits are selectively disconnected by programming the EPROM cells into their "0" state. Programming voltage and waveform specifications are available by request from Intel to support programming of the iPLD910.

Intelligent Programming Algorithm

The iPLD910 supports the Intelligent Programming Algorithm which rapidly programs Intel PLDs while ensuring programming reliability as the incremental program margin of each bit is continually monitored to determine when the bit has been successfully programmed.

FUNCTIONAL TESTING

Since the logical operation of the iPLD910 is controlled by EPROM elements, the device is completely testable. Each programmable EPROM bit controlling the internal logic is tested using application-independent test program patterns. After testing, the devices are erased before shipment to customers. No post-programming tests of the EPROM array are required.

The testability and reliability of EPROM-based programmable logic devices is an important feature over similar devices based on fuse technology. Fuse-based programmable logic devices require a user to perform post-programming tests to insure proper programming. These tests must be done at the device level because of the cummulative error effect. For example, a board containing ten devices each possessing a 2% device fallout translates into an 18% fallout at the board level (it should be noted that programming fallout of fuse-based programmable logic devices is typically 2% or higher).

DESIGN RECOMMENDATIONS

For proper operation, it is recommended that all input and output pins be constrained to the voltage range GND < (V_{IN} or V_{OUT}) < V_{CC}. Unused inputs and I/Os should be tied to V_{CC} or GND to minimize device power consumption. Reserved pins (as indicated in the logic compiler REPORT file) should be left floating (no connect) so that the pin can attain the appropriate logic level. A power supply decoupling capacitor of at least 0.2 μF must be connected directly between V_{CC} and GND pins of the device.

As with all CMOS devices, ESD handling procedures should be used with the iPLD910 to prevent damage to the device during programming, assembly and test.

DESIGN SECURITY

A single EPROM bit provides a programmable design security feature that controls the access to the data programmed into the device. If this bit is set, a proprietary design within the device cannot be copied. This EPROM security bit enables a higher degree of design security than fused-based devices since programmed data within EPROM cells is invisible even to microscopic evaluation. The EPROM security bit, along with all the other EPROM control bits, will be reset by erasing the device.

LATCH-UP IMMUNITY

All of the input, I/O, and clock pins of the iPLD910 have been designed to resist latch-up which is inherent in inferior CMOS structures. The iPLD910 is designed with Intel's proprietary CMOS II-E EPROM process. Thus, each of the pins will not experience latch-up with currents up to ± 100 mA and voltages ranging from $-1V$ to $(V_{CC} + 1V)$. Furthermore, the programming pin is designed to resist latch-up to the 13.5V maximum device limit.

DEVELOPMENT SOFTWARE

Third Party Support

The PLD910 is also supported by third-party logic compilers such as ABEL*, CUPL*, PLDesigner*, Log/IC, etc. Programming support is provided by third-party programmer companies such as Data I/O, Logical Devices, STAG, etc. Please refer to the "Third-Party Support" lists in the *Programmable Logic* handbook for complete information and vendor contacts.

Full logic compilation and functional simulation for the iPLD910 is supported by PLDshell Plus software.

PLDshell Plus

PLDshell Plus design software is Intel's user-friendly design tool for PLD design. PLDshell Plus allows user's to incorporate their preferred text editor, programming software, and additional design tools into a easy-to-use, menued design environment that includes Intel's PLDasm logic compiler and simulation software along with disassembly, conversion, and translation utilities. The PLDasm compiler and simulator software accepts industry-standard PDS source files that express designs as Boolean equations, truth tables, or state machines. On-line help, datasheet briefs, technical notes, and error message information, along with waveform viewing/printing capability make the design task as easy as possible. PLDshell Plus software is available from Intel Literature channels or from your local Intel sales representative.

Tools that support schematic capture and timing simulation for the iPLD910 are available. Please refer to the "Development Tools" section of the Programmable Logic handbook.

*ABEL is a trademark of Data I/O Corporation.

CUPL is a trademark of Logical Devices, Inc.

PLDesigner is a trademark of MINC, Inc.

Log/IC is a trademark of ISDATA, Corporation.

ADF PRIMITIVES SUPPORTED

The following ADF primitives are supported by this device:

INP	JOJF
CONF	JONF
COIF	SONF
RONF	SOSF
RORF	TOIF
ROIF	TONF
NORF	TOTF
NOJF	CLKB
NOSF	
NOTF	

ORDERING INFORMATION

f_{CNT1} (MHz)	f_{MAX} (MHz)	t_{PD} (ns)	Order Code	Package	Operating Range
62.5	100	12	P PLD910-12	PDIP	Commercial
			N PLD910-12	PLCC	Commercial
			DPLD910-12	*CerDIP	Commercial
50	83.3	15	P PLD910-15	PDIP	Commercial
			N PLD910-15	PLCC	Commercial
			DPLD910-15	*CerDIP	Commercial
			TDPLD910-15	*CerDIP	Industrial
			TDPLD910-15	*PLCC	Industrial
33.3	50	25	P PLD910-25	PDIP	Commercial
			N PLD910-25	PLCC	Commercial
			DPLD910-25	*CerDIP	Commercial

Commercial: 0°C to +70°C
Industrial: −40°C to +85°C
*Windowed package allows UV erase.

ABSOLUTE MAXIMUM RATINGS*

Symbol	Parameter	Min	Max	Units
V_{CC}	Supply Voltage(1)	−2.0	7.0	V
V_{PP}	Programming Supply Voltage(1)	−2.0	13.5	V
V_I	DC Input Voltage(1)(2)	−0.5	$V_{CC}+0.5$	V
t_{stg}	Storage Temperature	−65	+150	°C
t_{amb}	Ambient Temperature(3)	−10	+85	°C

NOTES:
1. Voltages with respect to ground.
2. Minimum DC input is −0.5V. During transitions, the inputs may undershoot to −2.0V or overshoot to +7.0V for periods less than 20 ns under no load conditions.
3. Under bias. Extended temperature versions are also available.

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

RECOMMENDED OPERATING CONDITIONS

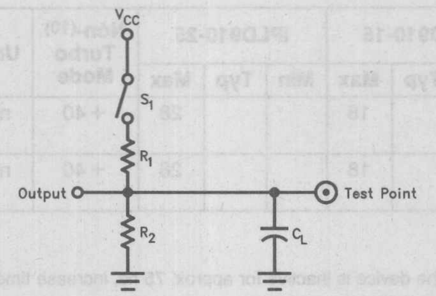
Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage	4.75	5.25	V
V_{IN}	Input Voltage	0	V_{CC}	V
V_O	Output Voltage	0	V_{CC}	V
T_A	Operating Temperature	0	+70	°C
t_R	Input Rise Time		500	ns
t_F	Input Fall Time		500	ns

D.C. CHARACTERISTICS $T_A = 0°C$ to $+70°C$, $V_{CC} = 5.0V \pm 5\%$

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}(4)	High Level Input Voltage	2.0		$V_{CC} + 0.3$	V	
V_{IL}(4)	Low Level Input Voltage	−0.3		0.8	V	
V_{OH}	High Level Output Voltage	2.4			V	$I_O = -4.0$ mA D.C., V_{CC} = min.
V_{OL}(5)	Low Level Output Voltage			0.45	V	$I_O = 12.0$ mA D.C., V_{CC} = min.
I_I	Input Leakage Current	−10		+10	µA	V_{CC} = max., GND < V_{IN} < V_{CC}
I_{OZ}	Output Leakage Current	−10		+10	µA	V_{CC} = max., GND < V_{OUT} < V_{CC}
I_{SC}(6)	Output Short Circuit Current	−30		−120	mA	V_{CC} = max., V_{OUT} = 0.5V
I_{SB}(7)	Standby Current		60	150	µA	V_{CC} = max., $V_{IN} = V_{CC}$ or GND, Standby Mode
I_{CC}	Power Supply Current (See I_{CC} vs. Freq. Graph)		4	12	mA	V_{CC} = max., $V_{IN} = V_{CC}$ or GND, No Load, f_{IN} = 1 MHz, Device Prog. as Two 12-Bit Counters, Turbo = Off
			120	150	mA	Turbo = On, f_{IN} = 1 MHz
I_{CCI}	Power Supply Current Industrial Temperature			180	mA	Turbo = On, f_{IN} = 1 MHz

NOTES:
4. Absolute values with respect to device GND; all over and undershoots due to system or tester noise are included.
5. Maximum DC I_{OL} for the device is 96 mA for CLK1 group I/O.1-I/O.12 and 96 mA for CLK2 group I/O.13-I/O.24.
6. Not more than 1 output should be tested at a time. Duration of that test should not exceed 1 second.
7. In Non-Turbo Mode (TURBO = OFF), device enters standby mode approximately 75 ns after the last input transition.

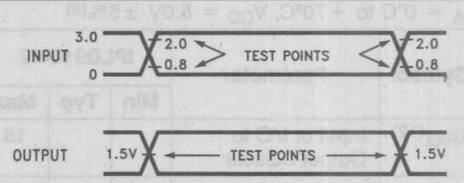
A.C. TESTING LOAD CIRCUIT



290456–13

C_L = 30 pF

A.C. TESTING INPUT, OUTPUT WAVEFORM



290456–14

A.C. Testing: Inputs are driven at 3.0V for a Logic "1" and 0V for a Logic "0". Timing Measurements are made at 2.0V for a Logic "1" and 0.8V for a Logic "0" on inputs. Outputs are measured at a 1.5V point. Device input rise and fall times are less than 3 ns.

SWITCHING TEST CIRCUIT

Specification	S_1	C_L	Commercial		Measured Output Value
			R_1	R_2	
t_{PD}	Closed	30 pF	200Ω	330Ω	1.5V
t_{PZX}	Z → H: Open Z → L: Closed				1.5V
t_{PXZ}	H → Z: Open L → Z: Closed	5 pF			H → Z: V_{OH} − 0.5V L → Z: V_{OL} + 0.5V

CAPACITANCE T_A = 0°C to +70°C; V_{CC} = 5.0V ±5%(8)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V, f = 1.0 MHz		5	8	pF
C_{IO}	I/O Capacitance	V_{OUT} = 0V, f = 1.0 MHz		6	8	pF
C_{CLK}	CLK Capacitance	V_{OUT} = 0V, f = 1.0 MHz		8	10	pF
C_{VPP}	V_{PP} Pin Capacitance	V_{PP} on CLK2, f = 1.0 MHz		10	12	pF

NOTES:
8. These values are evaluated at initial characterization and whenever design modifications occur that may affect capacitance.

COMBINATORIAL MODE A.C. CHARACTERISTICS

T_A = 0°C to +70°C, V_{CC} = 5.0V ±5%(9)

Symbol	Parameter	iPLD910-12			iPLD910-15			iPLD910-25			Non-(10) Turbo Mode	Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
t_{PD}(11)	Input or I/O to Output Valid w/ 8 Outputs Switching			12			15			25	+40	ns
t_{PZX}(12)	Input or I/O to Output Enable			15			18			28	+40	ns

COMBINATORIAL MODE A.C. CHARACTERISTICS (Continued)

$T_A = 0°C$ to $+70°C$, $V_{CC} = 5.0V \pm 5\%$(9)

Symbol	Parameter	iPLD910-12			iPLD910-15			iPLD910-25			Non-(10) Turbo Mode	Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
t_{PXZ}(12)	Input or I/O to Output Disable			15			18			28	+40	ns
t_{CLR}	Input or I/O to Asynch. Reset			15			18			28	+40	ns

NOTES:
9. Typical values are at $T_A = 25°C$, $V_{CC} = 5V$, Active Mode.
10. If device is operated in Non-Turbo Mode (TURBO = OFF) and the device is inactive for approx. 75 ns, increase time by amount shown.
11. Measured with eight outputs switching. See t_{PD} vs. Number of Outputs Switching graph.
12. t_{PZX} and t_{PXZ} are measured at $\pm 0.5V$ from steady state voltage as driven by spec. output load.

REGISTER MODE—SYNCHRONOUS CLOCK A.C. CHARACTERISTICS

$T_A = 0°C$ to $70°C$, $V_{CC} = 5.0V \pm 5\%$(9)

Symbol	Parameter	iPLD910-12			iPLD910-15			iPLD910-25			Non-(10) Turbo Mode	Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
f_{CNT1}(13)	Max. Counter Frequency $1/(t_{SU} + t_{CO})$—Ext. Feedback	62.5	75		50	66		33	40			MHz
f_{CNT2}(13)	Max. Counter Frequency $1/(t_{CNT})$—Internal Feedback	76.9	85		66.6	75		40	50			MHz
f_{MAX}	Max. Frequency (Pipelined) $1/(t_{CW})$—No Feedback	100	110		83.3	100		50	66			MHz
t_{SU}	Input or I/O Setup Time to CLK	8			11			16			+40	ns
t_H	Input or I/O Hold Time from CLK	0			0			0				ns
t_{CO1}(13)	CLK High to Output Valid			8			9			14		ns
t_{CO2}	CLK High to Output Valid Fed Through Comb. Macrocell			17			20			30	+40	ns
t_{CNT}(13)	Macrocell Output Feedback to Macrocell Input—Internal Path			13			15			25	+40	ns
t_{CL}	CLK Low Time	4			5			8				ns
t_{CH}	CLK High Time	4			5			8				ns
t_{CP}	CLK Period	10			12			20				ns

NOTE:
13. Measured with device configured as 24-bit counter.

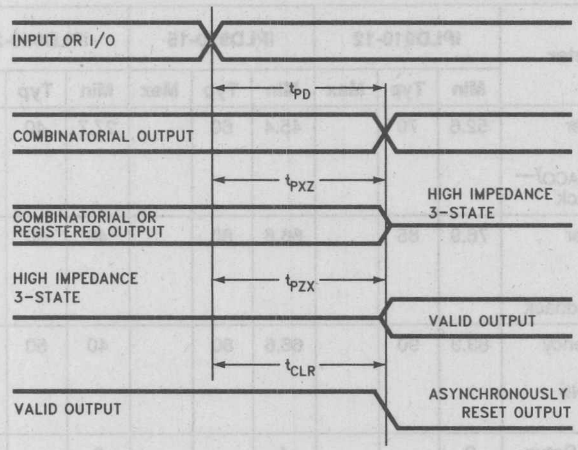
REGISTER MODE—ASYNCHRONOUS CLOCK A.C. CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = 5.0V ±5%(9)

Symbol	Parameter	iPLD910-12			iPLD910-15			iPLD910-25			Non-(10) Turbo Mode	Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
f_{ACNT1}(13)	Max. Counter Frequency $1/(t_{ASU} + t_{ACO})$—Ext. Feedback	52.6	70		45.4	60		27.7	40			MHz
f_{ACNT2}(13)	Max. Counter Frequency $1/(t_{ACNT})$—Internal Feedback	76.9	85		66.6	80		40	50			MHz
f_{AMAX}	Max. Frequency (Pipelined) $1/(t_{ACW})$—No Feedback	83.3	90		66.6	80		40	50			MHz
t_{ASU}	Input or I/O Setup to Asynch. CLK	3			4			8			+40	ns
t_{AH}	Input or I/O Hold from Asynch. CLK	6			7			8				ns
t_{ACO1}	Asynch. CLK High to Output Valid			16			18			28	+40	ns
t_{ACO2}	Asynch. CLK High to Output Valid Fed Through Comb. Macrocell			26			29			44	+40	ns
t_{ACNT}(13)	Macrocell Output Feedback to Macrocell Input—Internal Path			13			15			25	+40	ns
t_{ACL}	Asynch. CLK Low Time	5			6			10				ns
t_{ACH}	Asynch. CLK High Time	5			6			10				ns
t_{ACP}	Asynch. CLK Period	12			15			25				ns

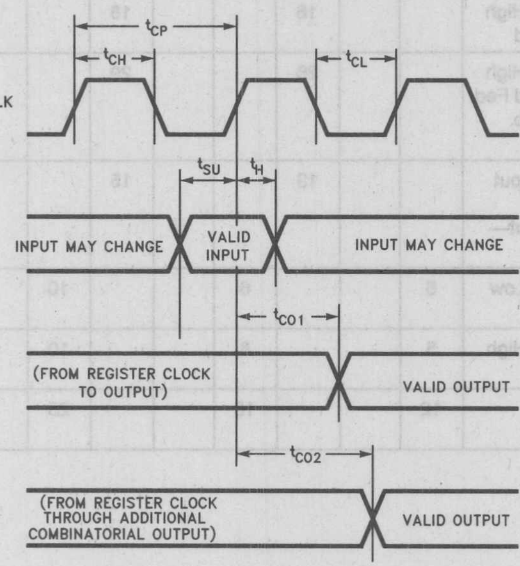
2

COMBINATORIAL MODE



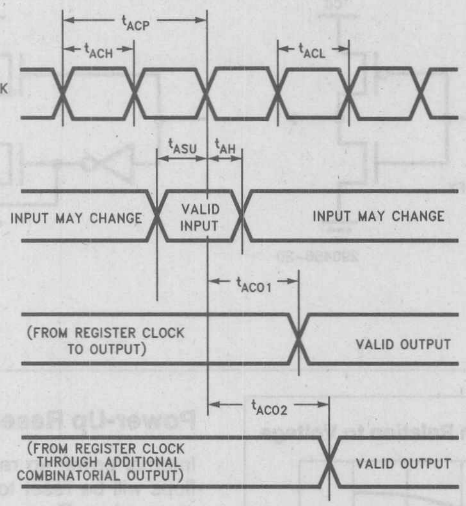
290456-15

SYNCHRONOUS REGISTERED MODE

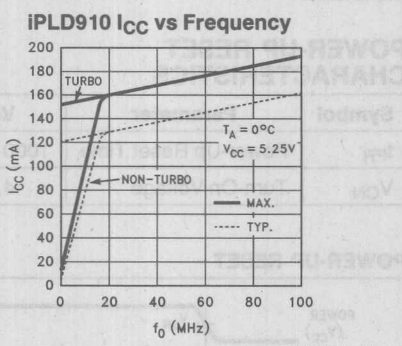


290456-16

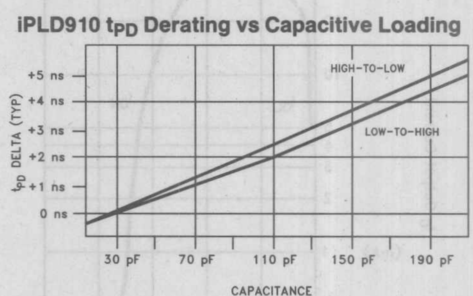
ASYNCHRONOUS REGISTERED MODE



290456-17

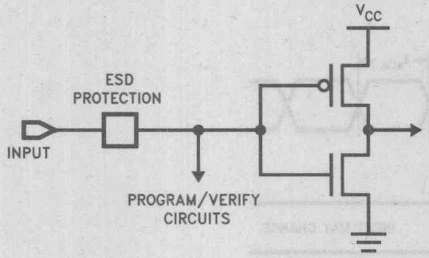


290456-18

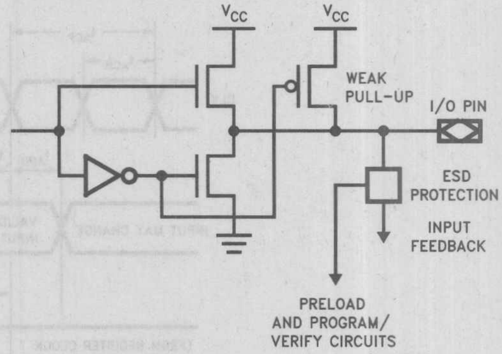


290456-19

Input/Output Equivalent Schematics

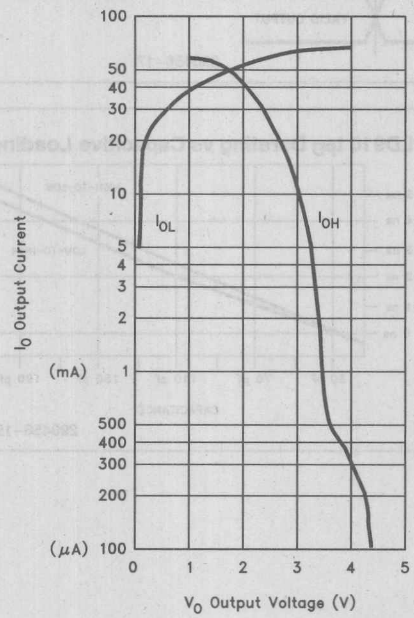


290456-20



290456-21

iPLD910 Output Current in Relation to Voltage



290456-22

CONDITIONS:
$T_A = +70°C$
$V_{CC} = 4.75V$

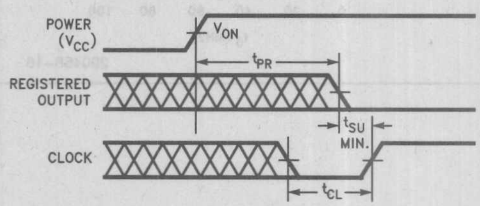
Power-Up Reset

Internal power-up reset circuits ensure that all flip-flops will be reset to a logic 0 after the device has powered-up. Because V_{CC} rise can vary significantly from one application to another, V_{CC} rise must be monotonic.

POWER-UP RESET CHARACTERISTICS

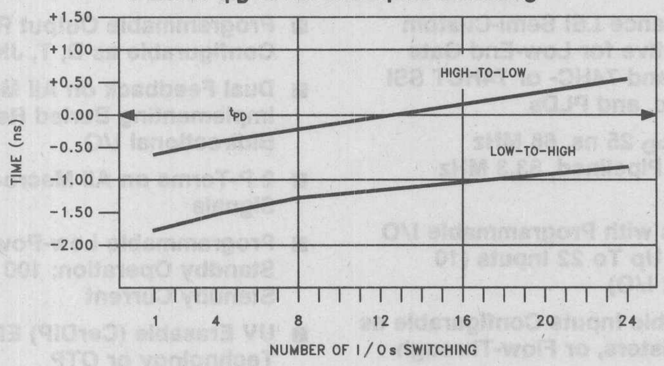
Symbol	Parameter	Value
t_{PR}	Power-Up Reset Time	1000 ns Max.
V_{ON}	Turn-On Voltage	4.75V

POWER-UP RESET



290456-23

iPLD910 t_{PD} vs No. of Outputs Switching



290456–24

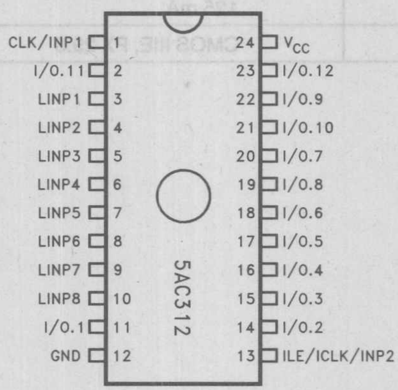
CONDITIONS:
$T_A = 70°C$, $V_{CC} = 4.75V$, Spec. Load

PACKAGE/TECHNOLOGY SPECIFICATIONS

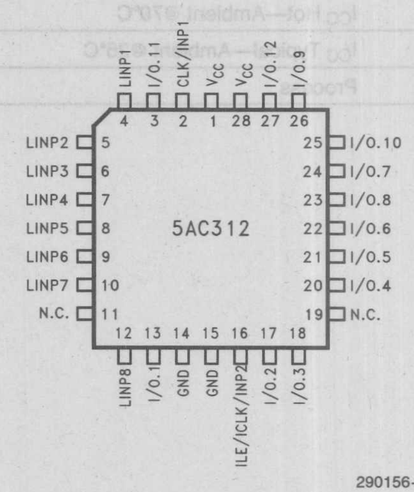
Description	Specification
θ_{JA}—Junction-to-Ambient Thermal Resistance	44.5°C/W-CerDIP 51°C/W-PDIP 55°C/W-PLCC
θ_{JC}—Junction-to-Case Thermal Resistance	17°C/W-CerDIP 29°C/W-PDIP 16°C/W-PLCC
I_{CC} Hot—Ambient @70°C	125 mA
I_{CC} Typical—Ambient @25°C	125 mA
Process	CMOS IIIE, PX 29.5

5AC312
1-MICRON CMOS 12-MACROCELL PLD

- **High-Performance LSI Semi-Custom Logic Alternative for Low-End Gate Arrays, TTL, and 74HC- or 74HCT SSI and MSI Logic, and PLDs**
- **High Speed t_{PD} 25 ns, 66 MHz Performance Pipelined, 33.3 MHz w/Feedback**
- **12 Macrocells with Programmable I/O Architecture; Up To 22 Inputs (10 Dedicated, 12 I/O)**
- **8 Programmable Inputs Configurable as Latches, Registers, or Flow-Through**
- **Flow-Through Input or Global CLK Pin; 1 Flow-Through Input or Global ILE/ICLK Pin**
- **Programmable AND, Allocatable OR Design Allows up to 16 P-Terms per Macrocell**
- **Software-Supported P-Term Allocation Between Adjacent Macrocells**
- **Programmable Output Registers Configurable as D, T, JK, or SR Types**
- **Dual Feedback on All Macrocells for Implementing Buried Registers with Bidirectional I/O**
- **2 P-Terms on All Macrocell Control Signals**
- **Programmable Low-Power Option for Standby Operation; 100 μA Typical Standby Current**
- **UV Erasable (CerDIP) EPROM Technology or OTP**
- **100% Generically Tested EPROM Logic Control Array**
- **Programmable Security Bit Allows 100% Protection of Proprietary Designs**
- **Available in 24-Pin 300-mil CerDIP/PDIP and 28-Pin PLCC Packages**
  (See Packaging Spec., Order Number 240800, Package Type D, P and N)



290156-1



290156-2

Figure 1. Pin Configurations

October 1993
Order Number: 290156-005

INTRODUCTION

The Intel 5AC312 CMOS PLD (Programmable Logic Device) represents an innovative approach to overcoming the primary limitations of standard PLDs. Due to a proprietary I/O architecture and macrocell structure, the 5AC312 is capable of implementing high performance logic functions more effectively than previously possible. It can be used as an alternative to low-end gate arrays, multiple programmable logic devices or LS-, HC- or HCT SSI and MSI logic devices. Input and macrocell features for the 5AC312 are a superset of features offered by other PLD-type products.

The 5AC312 uses advanced CMOS EPROM cells as logic control elements instead of poly-silicon fuses. This technology allows the 5AC312 to operate at levels necessary in high performance systems while significantly reducing the power consumption. Its programmable stand-by function reduces power consumption to almost "zero" in applications where a slight speed loss is traded for power savings.

ARCHITECTURE DESCRIPTION

The architecture of the 5AC312 is based on the familiar "Sum-Of-Products" programmable AND, fixed OR structure, though the 5AC312 macrocell contains a number of significant functional enhancements. This device can implement both combinational and sequential logic functions through a highly flexible macrocell and I/O structure. The 5AC312 has been designed to effectively implement both combinational-register and register-combinational-register forms of logic to easily accommodate state machine designs.

Figure 2 shows a global view of the 5AC312 architecture. The 5AC312 contains a total of 12 I/O macrocells, 8 user-programmable input structures, and 2 additional inputs that can be programmed to serve as either combinatorial inputs or clock inputs. Each of the eight inputs can be individually configured as a latch, register, or flow-through input. Input latches/registers can be synchronously or asynchronously clocked.

Each macrocell is further sub-divided into 16 Product Terms with 8 Product Terms dedicated to the control signals OE, PRESET, ASYNCH. CLK and CLEAR, and 8 Product Terms available for the general data array (see Figure 3).

The basic macrocell architecture of the 5AC312 includes a user-programmable AND array and a user-configurable OR array. The inputs to the programmable AND array originate from the true and complement signals from the programmable input structure, the dedicated inputs, and the 24 feedback paths from the 12 I/O macrocells.

PROGRAMMABLE INPUTS

Figure 4 shows a block diagram of the 5AC312 input architecture. This device contains 8 user-program-

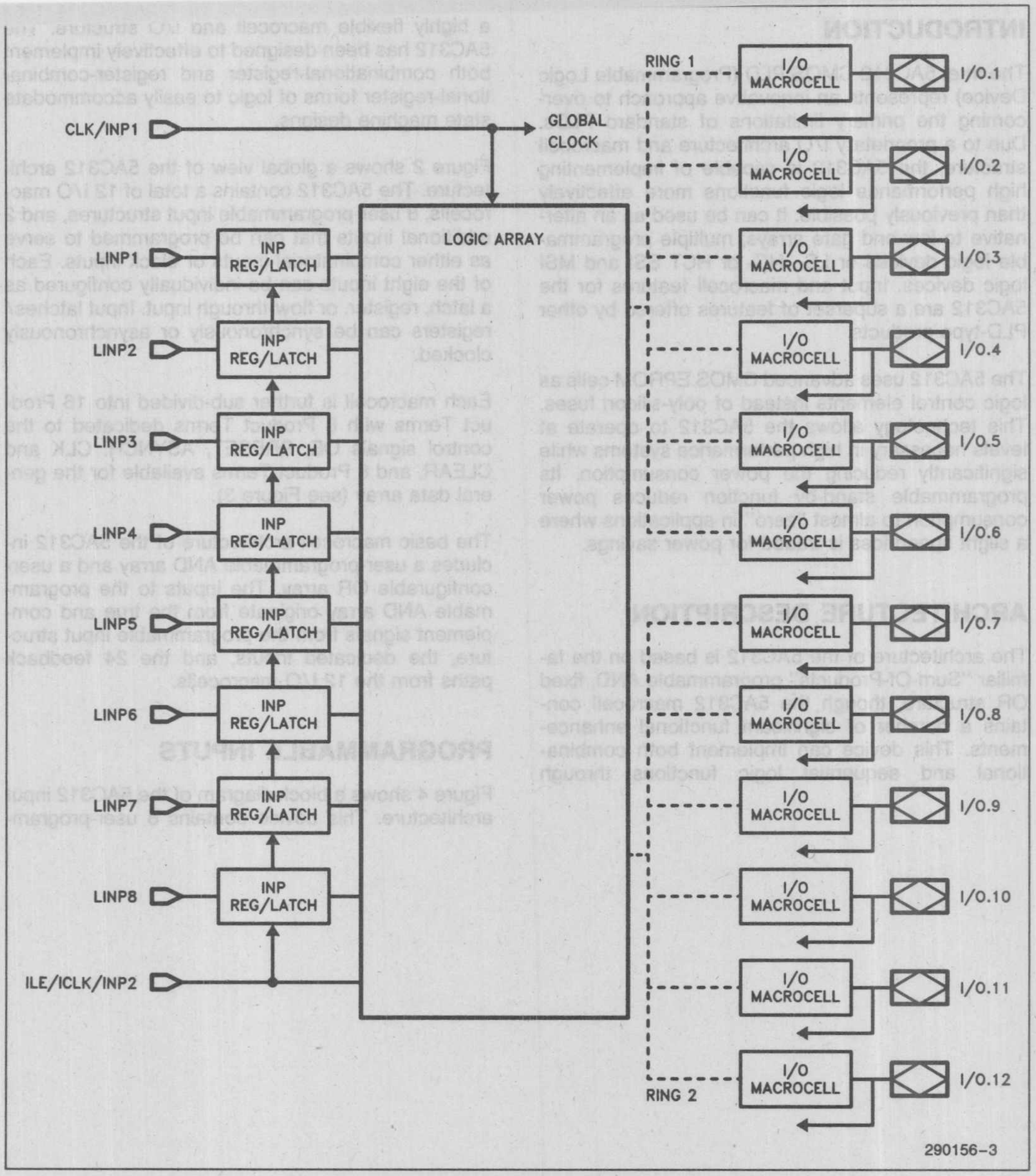
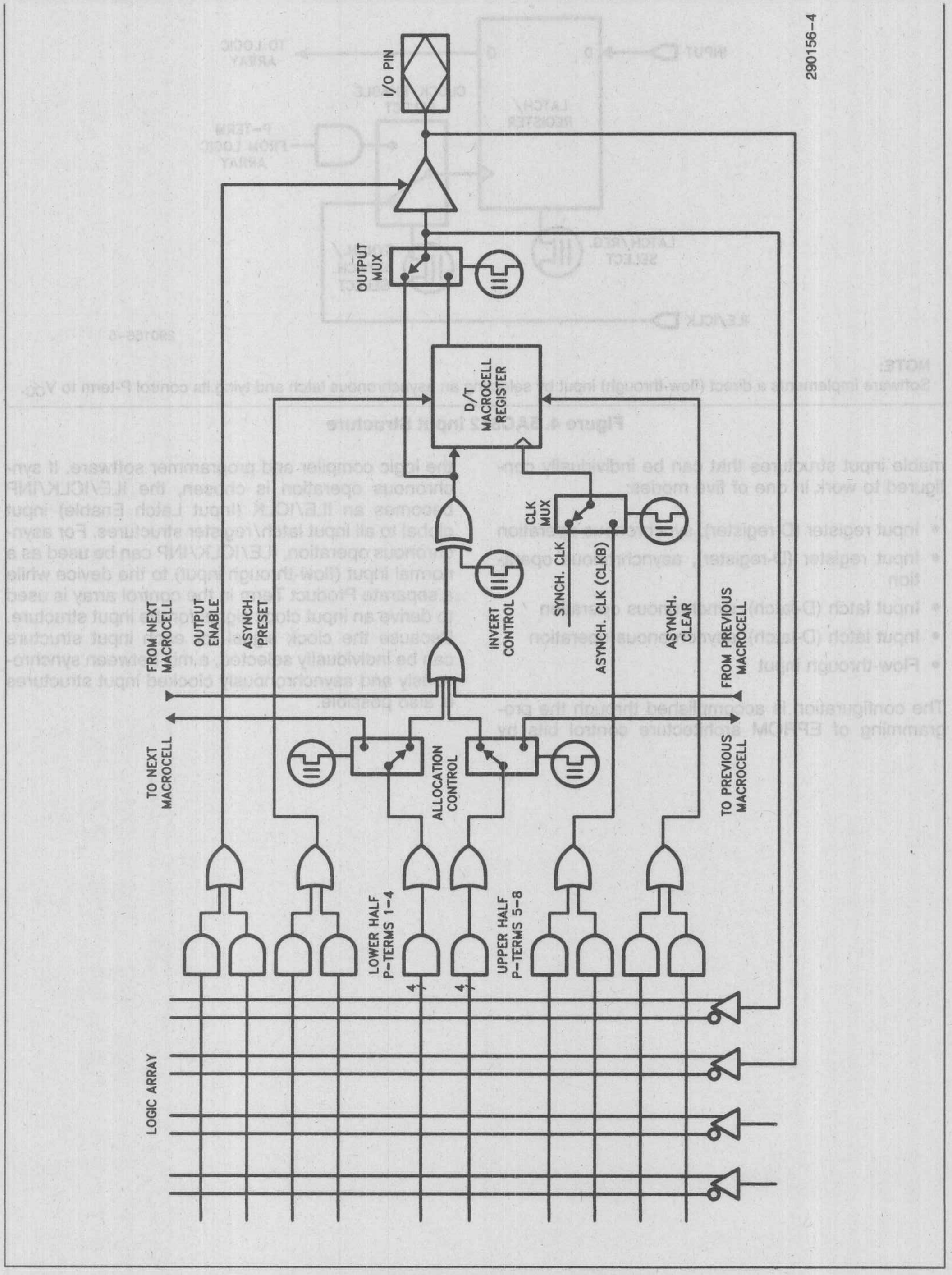
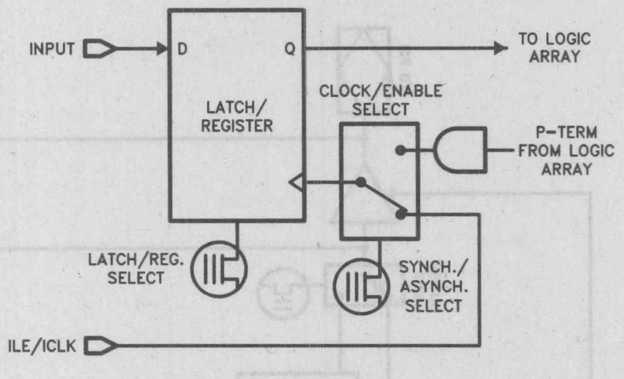


Figure 2. 5AC312 Architecture



290156-4

Figure 3. 5AC312 Basic Macrocell Structure



NOTE:
Software implements a direct (flow-through) input by selecting an asynchronous latch and tying its control P-term to V_{CC}.

Figure 4. 5AC312 Input Structure

mable input structures that can be individually configured to work in one of five modes:

- Input register (D-register), synchronous operation
- Input register (D-register), asynchronous operation
- Input latch (D-latch), synchronous operation
- Input latch (D-latch), asynchronous operation
- Flow-through input

The configuration is accomplished through the programming of EPROM architecture control bits by the logic compiler and programmer software. If synchronous operation is chosen, the ILE/ICLK/INP becomes an ILE/ICLK (Input Latch Enable) input global to all input latch/register structures. For asynchronous operation, ILE/ICLK/INP can be used as a normal input (flow-through input) to the device while a separate Product Term in the control array is used to derive an input clock signal for the input structure. Because the clock signal for each input structure can be individually selected, a mix between synchronously and asynchronously clocked input structures is also possible.

MACROCELLS

Each of 12 macrocells in the 5AC312 contains 8 p-terms (Product Terms) to support logic functions. These 8 p-terms are subdivided into 2 groups each containing 4 p-terms. This grouping of p-terms supports the proprietary p-term allocation scheme.

Register Configuration

Each macrocell can be configured as a D, T, RS, or JK register. The 8 p-terms for control functions are organized so that 2 p-terms support *each of the four* control signals. Control signals in the 5AC312 are: Output Enable (OE), asynchronous I/O register preset (PRESET), asynchronous clock for I/O registers (ASYNCH. CLK), and asynchronous I/O register reset (CLEAR). Availability of 2 p-terms per control signal is another feature that increases the efficiency of the device by reducing the need to use intermediate macrocells sometimes needed to implement control functions.

CLK is a global clock signal that can be used to synchronously clock any or all macrocell registers. It can be used as an input to the logic array at the same time as a macrocell clock. When CLK is not used as a synchronous clock, it functions only as a dedicated input to the logic array.

Combinatorial Configuration

The macrocell register can be bypassed to implement combinatorial logic functions. When configured to provide combinatorial logic, only the OE control signal is used.

Invert Select Bit

An invert select EPROM bit is used to invert the product term input into each macrocell register, including double inputs on JK and SR registers. This invert option allows the highest possible logic utilization by use of DeMorgan's logic inversion.

LOGIC ARRAY

Each intersecting point in the logic array contains a programmable EPROM connection. Initially (erased state), all connections are complete, i.e., both true and complement states of all signals are connected to each p-term.

Connections are opened during programming. When both the true and complement connections exist, a logical false results on the output of the AND gate. If both the true and complement connections of a signal are programmed "open", then a logic "don't care" results for that signal. If all connections for a p-term are programmed open, then a logical true results on the output of the AND gate.

PRODUCT TERM ALLOCATION

Product Term allocation is defined as taking logic resources (p-terms) away from macrocells where they are not used to support demand for more than 8 Product Terms in other areas of the chip. In the 5AC312, this allocation can occur in increments of 4 p-terms between adjacent macrocells.

The 12 macrocells available in the 5AC312 are grouped into two "rings" with 6 macrocells per ring. Product Terms can be allocated in a "shift register" mode inside a ring; allocation of Product Terms between the rings is not supported. The two rings are shown in Figure 2 and listed in Table 1.

Example:

The logic function in macrocell 4 requires 16 p-terms. In this case, the iPLS II software allocates 4 p-terms from the previous macrocell in Ring 1 (macrocell 3) and 4 p-terms from the next macrocell in Ring 1 (macrocell 5) to accumulate a total of 16 p-terms (8 + 4 + 4). This implementation leaves macrocells 3 and 5 with a remainder of 4 p-terms each. These remaining p-terms in macrocells 3 and 5 can also be allocated away to or can be supplemented with p-terms from their respective previous/next macrocells in Ring 1.

Applying this scheme to the 5AC312 it becomes clear that any macrocell inside the device can support logic functions requiring between 0 and 16 Product Terms. Product Terms allocated away from a macrocell do not affect that macrocell's output structure. If all Product Terms are allocated "away" from a macrocell, the input to that macrocell's I/O control block is tied to GND. This polarity can be changed by programming the invert select EPROM bit. The I/O register as well as all secondary controls to this I/O control block are still available and can be used if needed.

The Product Term allocation scheme described above is automatically supported by iPLS II V2.0 and is transparent to the user. Users can still use explicit pin assignments, but should assign pins in a way that does not conflict with p-term allocation. Software support allows the control signals on macrocells to be used to implement simple logic functions even when all the input p-terms have been allocated to adjacent macrocells.

Table 1. Product Term Allocation Rings

Ring 1			Ring 2		
Current Macro-cell	Next Macro-cell	Previous Macro-cell	Current Macro-cell	Next Macro-cell	Previous Macro-cell
1	2	6	7	8	12
2	3	1	8	9	7
3	4	2	9	10	8
4	5	3	10	11	9
5	6	4	11	12	10
6	1	5	12	7	11

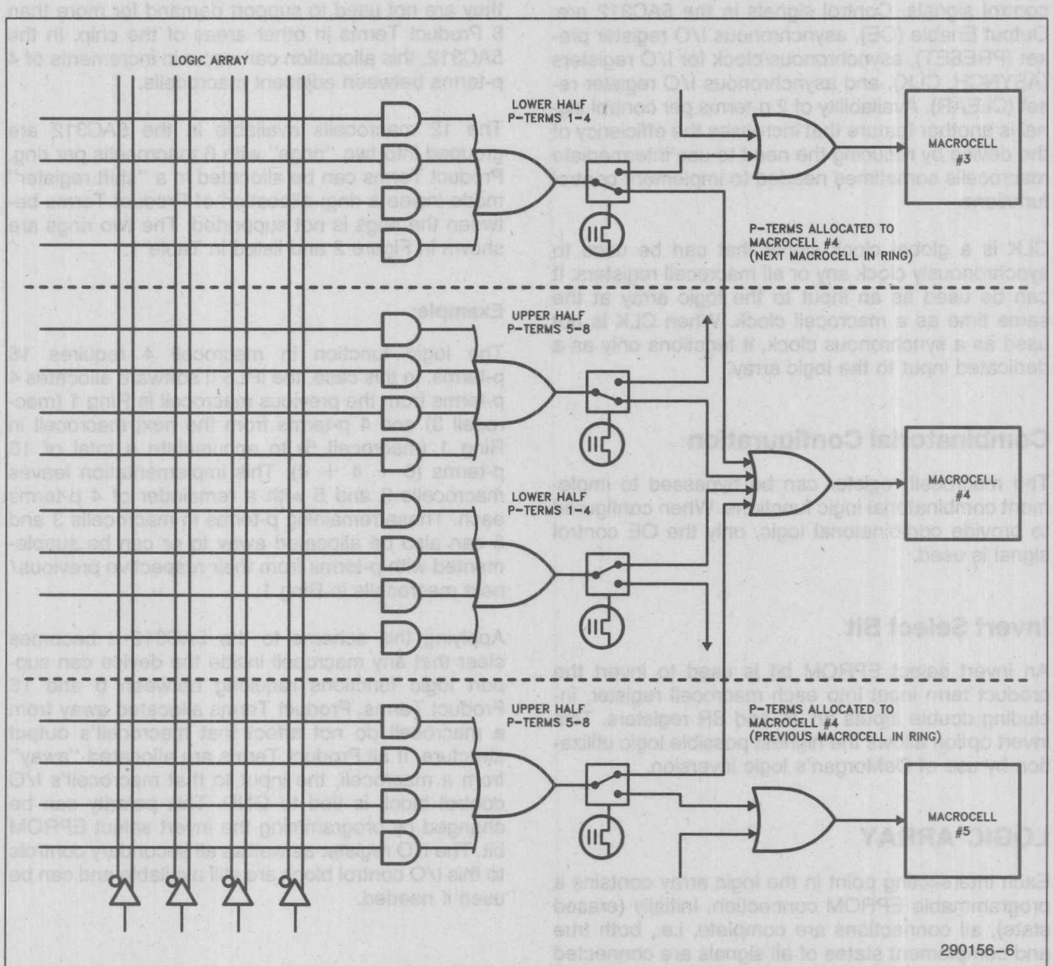


Figure 5. Product Term Allocation (8 + 4 + 4)

DUAL-FEEDBACK/BURIED LOGIC

Macrocell output can be fed back to the logic array on either one of the two feedback paths. If the pin feedback is used (connected after the output buffer), bidirectional I/O can be implemented. If the internal feedback path is used to implement a buried register or buried logic function, the pin feedback is still available for use as an input. The availability of dual feedbacks on the 5AC312 enhances resource efficiency over single feedback devices.

AUTOMATIC STANDBY MODE

The 5AC312 contains a programmable bit, the Turbo Bit, that optimizes operation for speed or for power savings. When the Turbo Bit is programmed (TURBO = ON), the device is optimized for maximum speed. When the Turbo Bit is not programmed (TURBO = OFF), the device is optimized for power savings by entering standby mode during periods of inactivity.

approximately 100 ns after the last input or I/O transition. When the next input or I/O transition is detected, the device returns to active mode. Wakeup time adds an additional 20 ns to the propagation delay through the device as measured from the first transition. No delay will occur if an output is dependent on more than one input and the last of the inputs changes after the device has returned to active mode.

After erasure, the Turbo Bit is unprogrammed (OFF); automatic standby mode is enabled. When the Turbo Bit is programmed (ON), the device never enters standby mode.

POWER-ON CHARACTERISTICS

Macrocell registers of the 5AC312 experience a reset to their inactive state (logic low) upon V_{CC} power-up. Using the PRESET function available to each macrocell, any particular register preset can be achieved after power-up. 5AC312 inputs and outputs begin responding within 10 μs (6 μs typical) after V_{CC} power-up or after a power-loss/power-up sequence. Input registers are not reset on power-up and are indeterminate. Input latches reflect the state of the input pins on power-up.

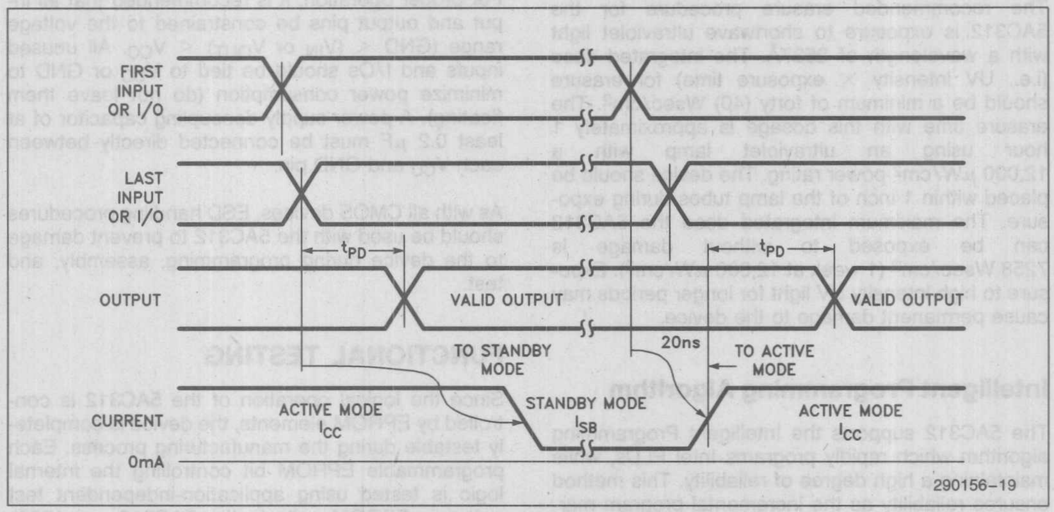


Figure 6. 5AC312 Standby and Active Mode Transitions

After erasure and prior to programming, all macrocells are configured as combinatorial, inverted outputs with output buffers three-stated. Inputs are configured as synchronous registers.

ERASURE CHARACTERISTICS

> Erasure time for the 5AC312 is 1 hour at 12,000 $\mu W/cm^2$ with a 2537Å UV lamp.

Erasure characteristics of the device are such that erasure begins to occur upon exposure to light with wavelengths shorter than approximately 4000Å. It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000Å–4000Å range. Data shows that constant exposure to room level fluorescent lighting could erase the typical 5AC312 in approximately six years, while it would take approximately two weeks to erase the device when exposed to direct sunlight. If the device is to be exposed to these lighting conditions for extended periods of time, conductive opaque labels should be placed over the device window to prevent unintentional erasure.

The recommended erasure procedure for the 5AC312 is exposure to shortwave ultraviolet light with a wavelength of 2537Å. The integrated dose (i.e., UV intensity × exposure time) for erasure should be a minimum of forty (40) $Wsec/cm^2$. The erasure time with this dosage is approximately 1 hour using an ultraviolet lamp with a 12,000 $\mu W/cm^2$ power rating. The device should be placed within 1 inch of the lamp tubes during exposure. The maximum integrated dose the 5AC312 can be exposed to without damage is 7258 $Wsec/cm^2$ (1 week at 12,000 $\mu W/cm^2$). Exposure to high intensity UV light for longer periods may cause permanent damage to the device.

Intelligent Programming Algorithm

The 5AC312 supports the Intelligent Programming algorithm which rapidly programs Intel PLDs, while maintaining a high degree of reliability. This method ensures reliability as the incremental program margin of each bit has been verified in the programming process. (Programming information for the 5AC312 is available from Intel by request.)

A Security Bit provides a programmable security option to protect the data programmed in the device. Once this bit is set during programming, subsequent attempts to read the device architecture information are prevented. This method provides a higher degree of design security than fuse-based devices, since programmed EPROM cells are invisible even to microscopic examination. The Security Bit (also called the Verify Protect Bit), along with all the other EPROM cells, is reset by erasing the device.

LATCH-UP IMMUNITY

All of the input, I/O, and clock pins of the device have been designed to resist latch-up which is inherent in inferior CMOS structures. The 5AC312 is designed with Intel's proprietary 1-micron CMOS EPROM process. Thus, each of the pins will not experience latch-up with currents up to ±100 mA and voltages ranging from $-0.5V$ to ($V_{CC} + 0.5V$). The programming pin is designed to resist latch-up to the 13.5 maximum device limit.

DESIGN RECOMMENDATIONS

For proper operation, it is recommended that all input and output pins be constrained to the voltage range (GND < (V_{IN} or V_{OUT}) < V_{CC}. All unused inputs and I/Os should be tied to V_{CC} or GND to minimize power consumption (do not leave them floating). A power supply decoupling capacitor of at least 0.2 μF must be connected directly between each V_{CC} and GND pin.

As with all CMOS devices, ESD handling procedures should be used with the 5AC312 to prevent damage to the device during programming, assembly, and test.

FUNCTIONAL TESTING

Since the logical operation of the 5AC312 is controlled by EPROM elements, the device is completely testable during the manufacturing process. Each programmable EPROM bit controlling the internal logic is tested using application-independent test patterns. EPROM cells in the 5AC312 are 100% tested for programming and erase. After testing, the devices are erased before shipments to the customers. No post-programming tests of the EPROM array are required.

The testability and reliability of EPROM-based programmable logic devices are important features over similar devices based on fuse technology. Fuse-based programmable logic devices require a user to perform post-programming tests to insure device functionality. During the manufacturing process, tests on these parts can only be performed in very restricted manners to prevent pre-programming of the array.

SOFTWARE SUPPORT

Full logic compilation and functional simulation for the 5AC312 is supported by PLDshell Plus software. The GUPI Logic-IID provides programming support on Intel programmers.

PLDshell Plus design software is Intel's user-friendly design tool for μPLD design. PLDshell Plus allows users to incorporate their preferred text editor, programming software, and additional design tools into a easy-to-use, menued design environment that includes Intel's PLDasm logic compiler and simulation software along with disassembly, conversion and translation utilities. The PLDasm compiler and simulator software accepts industry-standard PDS source files that express designs as Boolean equations, truth tables, or state machines. On-line help, datasheet briefs, technical notes, and error message information, along with waveform viewing/printing capability make the design task as easy as possible. PLDshell Plus software is available from Intel Literature channels or from your local Intel sales representative.

Tools that support schematic capture and timing simulation for the 5AC312 are available. Please refer to the "Development Tools" section of the Programmable Logic handbook.

The 5AC312 is also supported by third-party logic compilers such as ABEL*, CUPL*, PLDesigner*, Log/IC*, etc. Programming support is provided by third-party programmer companies such as Data I/O, Logical Devices, STAG, etc. Please refer to the "Third-Party Support" lists in the *Programmable Logic* handbook for complete information and vendor contacts.

ORDERING INFORMATION

t_{PD} (ns)	t_{CO} (ns)	f_{MAX} (MHz)	Order Code	Package	Operating Range
25	15	66	D5AC312-25	†CERDIP	Commercial
			P5AC312-25	PDIP	
			N5AC312-25	PLCC	
30	18	50	D5AC312-30	†CERDIP	Commercial
			P5AC312-30	PDIP	
			N5AC312-30	PLCC	
30	18	50	TN5AC312-30	PLCC	Industrial

†Windowed package allows UV erase.

*ABEL is a trademark of Data I/O, Corporation. CUPL is a trademark of Logical Devices, Inc. PLDesigner is a trademark of MINC, Inc. Logic/IC is a trademark of ISDATA, Inc.

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage (V_{CC}) (1) .... −2.0V to +7.0V

Programming Supply
Voltage (V_{PP}) (1) .... −2.0V to +13.5V

D.C. Input Voltage (V_I)(1, 2) .... −0.5V to V_{CC} + 0.5V

Storage Temperature (T_{stg}) ..... −65°C to +150°C

Ambient Temperature (T_{amb}) (3) .. −10°C to +85°C

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

***WARNING:** *Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

NOTES:
1. Voltages with respect to GND.
2. Minimum D.C. input is −0.5V. During transitions, the inputs may undershoot to −2.0V or overshoot to +7V for periods of less than 20 ns under no load conditions.
3. Under bias. Extended temperature range versions are available.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage	4.75	5.25	V
V_{IN}	Input Voltage	0	V_{CC}	V
V_O	Output Voltage	0	V_{CC}	V
T_A	Operating Temperature	0	+70	°C
t_R	Input Rise Time		500	ns
t_F	Input Fall Time		500	ns

D.C. CHARACTERISTICS T_A = 0°C to +70°C, V_{CC} = 5.0V ±5%

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}(4)	High Level Input Voltage	2.0		V_{CC} + 0.3	V	
V_{IL}(4)	Low Level Input Voltage	−0.3		0.8	V	
V_{OH}(5)	High Level Output Voltage	2.4			V	I_O = −4.0 mA D.C., V_{CC} = min.
V_{OL}	Low Level Output Voltage			0.45	V	I_O = 8.0 mA D.C., V_{CC} = min.
I_I	Input Leakage Current			±10	µA	V_{CC} = max., GND < V_{IN} < V_{CC}
I_{OZ}	Output Leakage Current			±10	µA	V_{CC} = max., GND < V_{OUT} < V_{CC}
I_{SC}(6)	Output Short Circuit Current	−30		−90	mA	V_{CC} = max., V_{OUT} = 0.5V
I_{SB}(7)	Standby Current		100	300	µA	V_{CC} = max., V_{IN} = V_{CC} or GND, Standby Mode

D.C. CHARACTERISTICS $T_A = 0°C$ to $+70°C$, $V_{CC} = 5.0V \pm 5\%$ (Continued)

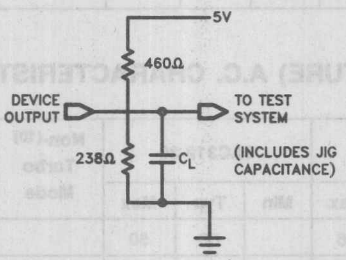
Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
I_{CC}	Power Supply Current (See I_{CC} vs Freq. Graph)		10		mA	V_{CC} = max., $V_{IN} = V_{CC}$ or GND, No Load, Input Freq. = 1 MHz Active Mode (Turbo = Off), Device Prog. as 12-Bit Ctr.

NOTES:
4. Absolute values with respect to device GND; all over and undershoots due to system or tester noise are included. Do not attempt to test these values without suitable equipment.
5. I_O at CMOS levels (3.84V) = −2 mA.
6. Not more than 1 output should be tested at a time. Duration of that test must not exceed 1 second.
7. With Turbo Bit Off, device automatically enters standby mode approximately 100 ns after last input transition.

CAPACITANCE

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
C_{IN}	Input Capacitance			8	pF	V_{IN} = 0V, f = 1.0 MHz
C_{OUT}	I/O Capacitance			15	pF	V_{OUT} = 0V, f = 1.0 MHz
C_{CLK}	ILE/ICLK/INP2 Capacitance			12	pF	V_{IN} = 0V, f = 1.0 MHz
C_{VPP}	V_{PP} Pin (CLK/INP1)			25	pF	V_{IN} = 0V, f = 1.0 MHz

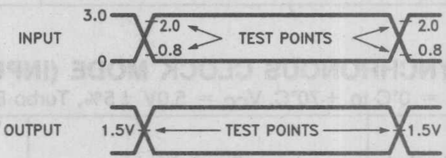
A.C. TESTING LOAD CIRCUIT



290156-7

C_L = 30 pF

A.C. TESTING INPUT, OUTPUT WAVEFORM



290156-8

A.C. Testing: Inputs are driven at 3.0V for a Logic "1" and 0V for a Logic "0". Timing Measurements are made at 2.0V for a Logic "1" and 0.8V for a Logic "0" on inputs. Outputs are measured at a 1.5V point. Device input rise and fall times < 6 ns.

A.C. CHARACTERISTICS $T_A = 0°C$ to $+70°C$, $V_{CC} = 5.0V \pm 5\%$, Turbo Bit "On"(8)

Symbol	From	To	5AC312-25			5AC312-30			Non-(10) Turbo Mode	Unit
			Min	Typ	Max	Min	Typ	Max		
t_{PD}	Input or I/O	Comb. Output		20	25		25	30	+20	ns
t_{PZX}(9)	Input or I/O	Output Enable		20	25		25	30	+20	ns
t_{PXZ}(9)	Input or I/O	Output Disable		20	25		25	30	+20	ns
t_{CLR}	Asynch. Reset	Q Reset		20	25		25	30	+20	ns
t_{SET}	Asynch. Set	Q Set		20	25		25	30	+20	ns

NOTES:
8. Typical values are at T_A = 25°C, V_{CC} = 5V, Active Mode.
9. t_{PZX} and t_{PXZ} are measured at ±0.5V from steady-state voltage as driven by spec. output load. t_{PXZ} is measured with C_L = 5 pF.
10. If device is operated with Turbo Bit Off (Non-Turbo Mode) and the device has been inactive for approximately 100 ns, increase time by amount shown.

$T_A = 0°C$ to $+70°C$, $V_{CC} = 5.0V \pm 5\%$, Turbo Bit On(8)

Symbol	Parameter	5AC312-25			5AC312-30			Non-(10) Turbo Mode	Unit
		Min	Typ	Max	Min	Typ	Max		
f_{MAX}	Max. Frequency (Pipelined) $1/t_{SU}$—No Feedback		80	66		66	50		MHz
f_{CNT1}	Max. Count Frequency $1/(t_{SU} + t_{CO})$—External Feedback		40	33.3		33	26.3		MHz
f_{CNT2}	Max. Count Frequency $1/t_{CNT}$—Internal Feedback		40	33.3		35	28.5		MHz
t_{SU1}	Input Setup Time to CLK ↑	15	12		20	18		+20	ns
t_{SU2}	I/O Setup Time to CLK ↑	15	12		20	18		+20	ns
t_H	I or I/O Hold after CLK ↑	0			0				ns
t_{CO}	CLK ↑ to Output Valid		10	15		12	18		ns
t_{CNT}	Macrocell Output Feedback to Macrocell Input—Internal Path		25	30		30	35	+20	ns
t_{CH}	CLK High Time	7			9				ns
t_{CL}	CLK Low Time	7			9				ns
t_{CW}	Minimum Clock Period	15			20				ns

SYNCHRONOUS CLOCK MODE (INPUT STRUCTURE) A.C. CHARACTERISTICS

$T_A = 0°C$ to $+70°C$, $V_{CC} = 5.0V \pm 5\%$, Turbo Bit On(8)

Symbol	Parameter	5AC312-25			5AC312-30			Non-(10) Turbo Mode	Unit
		Min	Typ	Max	Min	Typ	Max		
f_{MAXI}	Max. Frequency $(1/t_{CWI})$		80	66		66	50		MHz
t_{SUIR}	Input Register/Latch Setup Time before ILE/ICLK ↓	5			5				ns
t_{ESUI}(11)	Input Latch Setup Time before ILE ↑	5			5				ns
t_{COI}	ICLK ↓ to Comb. Output		30	35		35	40	+20	ns
t_{EOI}	ILE ↑ to Comb. Output		30	35		35	40	+20	ns
t_{HI}	Input Hold after ICLK/ILE ↓	7			10				ns
t_{EHI}	Input Hold after ILE ↓	7			10				ns
t_{CHI}	ILE/ICLK High Time	7			9				ns
t_{CLI}	ILE/ICLK Low Time	7			9				ns
t_{CWI}	Minimum Input Clock Period	15			20				ns

NOTE:

11. This specification must be met to guarantee t_{EOI}. When ILE goes high before data is valid, use t_{PD} instead of t_{EOI}.

$T_A = 0°C$ to $+70°C$, $V_{CC} = 5.0V \pm 5\%$, Turbo Bit On(8)

Symbol	Parameter	5AC312-25			5AC312-30			Non-(10) Turbo Mode	Unit
		Min	Typ	Max	Min	Typ	Max		
f_{AMAXI}	Max. Frequency Input Register $1/(t_{ACLI} + t_{ACHI})$		80	66		66	50		MHz
t_{ASUIR}	Input Register/Latch Setup Time to Asynch. ILE/ICLK	0			0				ns
t_{AESUI}(11)	Input Latch Setup Time before Asynch. ILE	0			0				ns
t_{ACOI}	Asynch. ICLK to Comb. Output		40	48		45	55	+20	ns
t_{AEOI}	Asynch. ILE ↑ to Comb. Output		40	48		45	55	+20	ns
t_{AHI}	Input Register/Latch Hold after Asynch. ILE/ICLK	20	14		25	20		+20	ns
t_{AEHI}	Input Hold after Asynch. ILE	20	14		25	20			ns
t_{ACHI}	Asynch. ICLK High Time	7			9			+20	ns
t_{ACLI}	Asynch. ICLK Low Time	7			9			+20	ns
t_{ACWI}	Minimum Input Clock Period	15			20			+20	ns

ASYNCHRONOUS CLOCK MODE MACROCELLS A.C. CHARACTERISTICS

$T_A = 0°C$ to $+70°C$, $V_{CC} = 5.0V \pm 5\%$, Turbo Bit On(8)

Symbol	Parameter	5AC312-25			5AC312-30			Non-(10) Turbo Mode	Unit
		Min	Typ	Max	Min	Typ	Max		
f_{AMAX}	Max. Frequency (Pipelined) $1/(t_{ACL} + t_{ACH})$—No Feedback		80	66		66	50		MHz
f_{ACNT1}	Max. Frequency $1/(t_{ASU} + t_{ACO})$—External Feedback		35	28.5		33	23.8		MHz
f_{ACNT2}	Max. Frequency $1/t_{ACNT}$—with Feedback		40	33.3		35	30		MHz
t_{ASU1}	Input Setup Time to Asynch. Clock	10			12			+20	ns
t_{ASU2}	I/O Setup Time to Asynch. Clock	10			12			+20	ns
t_{AH}	Input or I/O Hold after Asynch. Clock	5	0		5	0			ns
t_{ACO}	Asynch. CLK to Output Valid		20	25		25	30	+20	ns
t_{ACNT}	Register Output Feedback to Register Input—Internal Path		25	30		30	35	+20	ns
t_{ACH}	Asynch. CLK High Time	7			9			+20	ns
t_{ACL}	Asynch. CLK Low Time	7			9			+20	ns
t_{ACW}	Minimum Asynch. CLK Period	15			20			+20	ns

INPUT-CLOCK-TO-MACROCELL-CLOCK A.C. CHARACTERISTICS

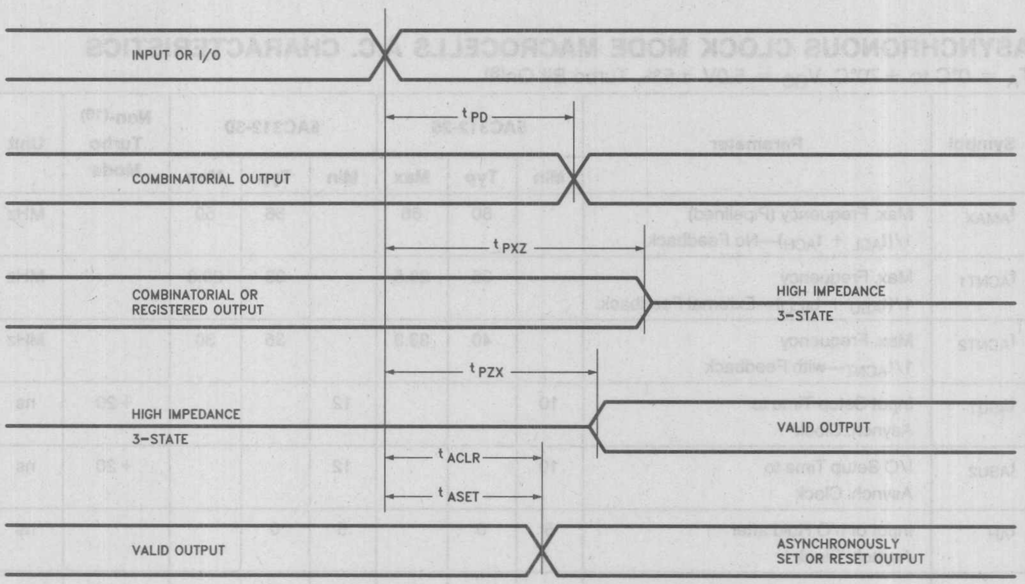
$T_A = 0°C$ to $+70°C$, $V_{CC} = 5.0V \pm 5\%$, Turbo Bit On(8)

Symbol	Parameter	5AC312-25			5AC312-30			Non-(10) Turbo Mode	Unit
		Min	Typ	Max	Min	Typ	Max		
t_{C1C2}(12)	Synchronous ILE/ICLK to Synchronous Macrocell CLK	25			30			+20	ns
	Synchronous ILE/ICLK to Asynchronous Macrocell CLK	15			18			+20	ns
	Asynchronous ILE/ICLK to Synchronous Macrocell CLK	35			40			+20	ns
	Asynchronous ILE/ICLK to Asynchronous Macrocell CLK	25			35			+20	ns

NOTE:
12. Times for SETUP, HOLD, and OUTPUT VALID are shown in previous tables.

SWITCHING WAVEFORMS

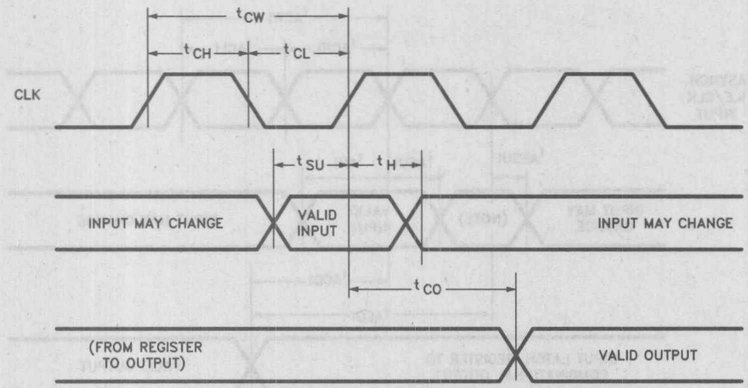
COMBINATORIAL MODE



290156–9

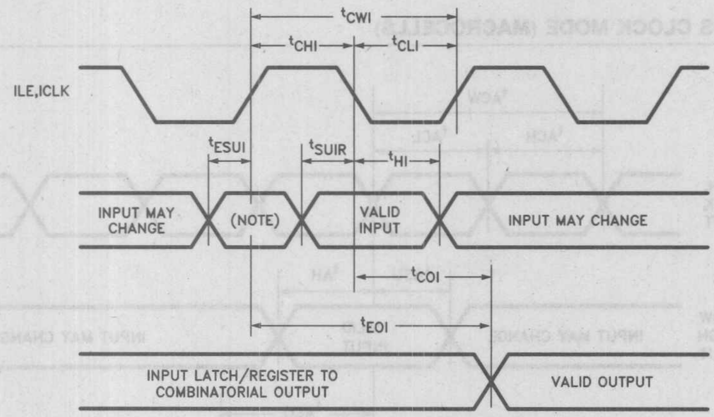
SWITCHING WAVEFORMS (Continued)

SYNCHRONOUS CLOCK MODE (MACROCELLS)



290156-10

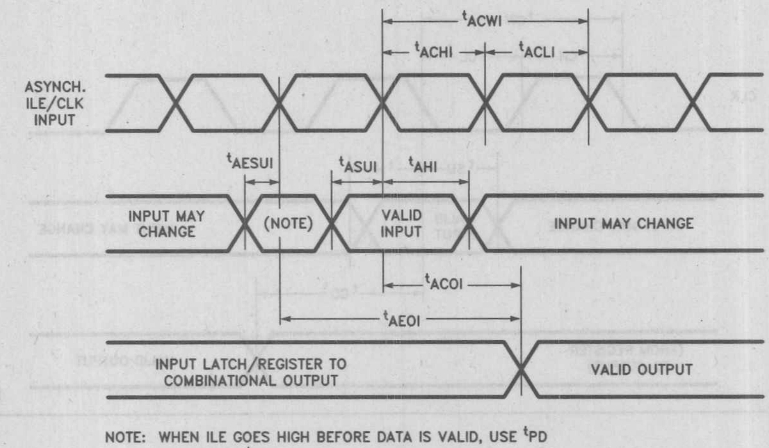
SYNCHRONOUS CLOCK MODE (INPUT STRUCTURE)



NOTE: WHEN ILE GOES HIGH BEFORE DATA IS VALID, USE t_{PD} INSTEAD OF t_{EOI}.

290156-11

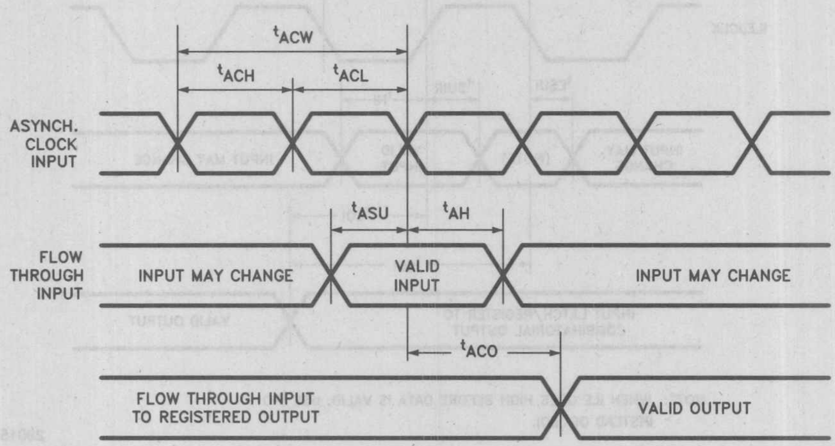
ASYNCHRONOUS CLOCK MODE (INPUT STRUCTURE)



NOTE: WHEN ILE GOES HIGH BEFORE DATA IS VALID, USE t_{PD} INSTEAD OF t_{AEOI}.

290156–13

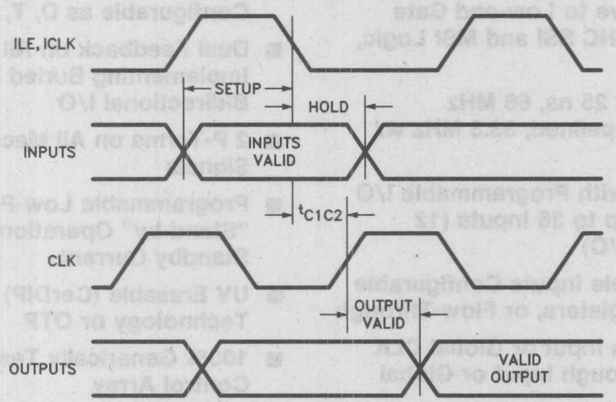
ASYNCHRONOUS CLOCK MODE (MACROCELLS)



290156–12

SWITCHING WAVEFORMS (Continued)

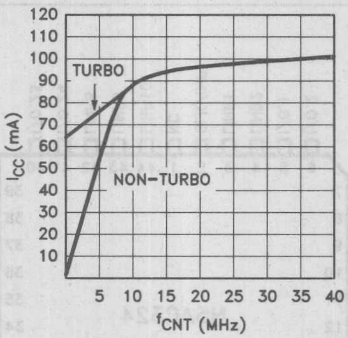
INPUT CLOCK-TO-MACROCELL CLOCK TIMING (CLOCKED PIPELINED DATA)



290156-18

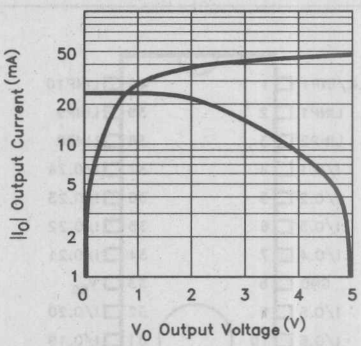
CLOCK, SETUP, HOLD, and OUTPUT VALID times are dependent on synchronous/asynchronous clocking and are listed in the specification tables.

5AC312 Current in Relation to Frequency



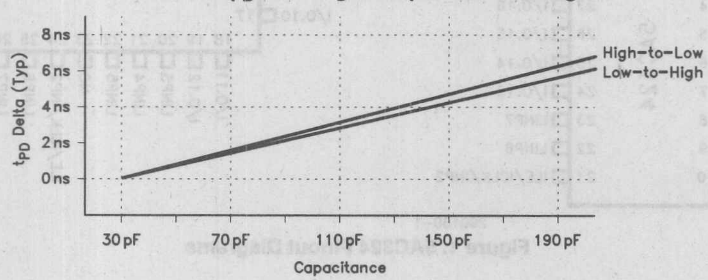
Conditions: $T_A = +25°C$, $V_{CC} = 5.25V$ 290156-20

5AC312 Output Drive Current in Relation to Voltage



Conditions: $T_A = +25°C$ 290156-16

5AC312 t_{PD} Derating vs Capacitive Loading



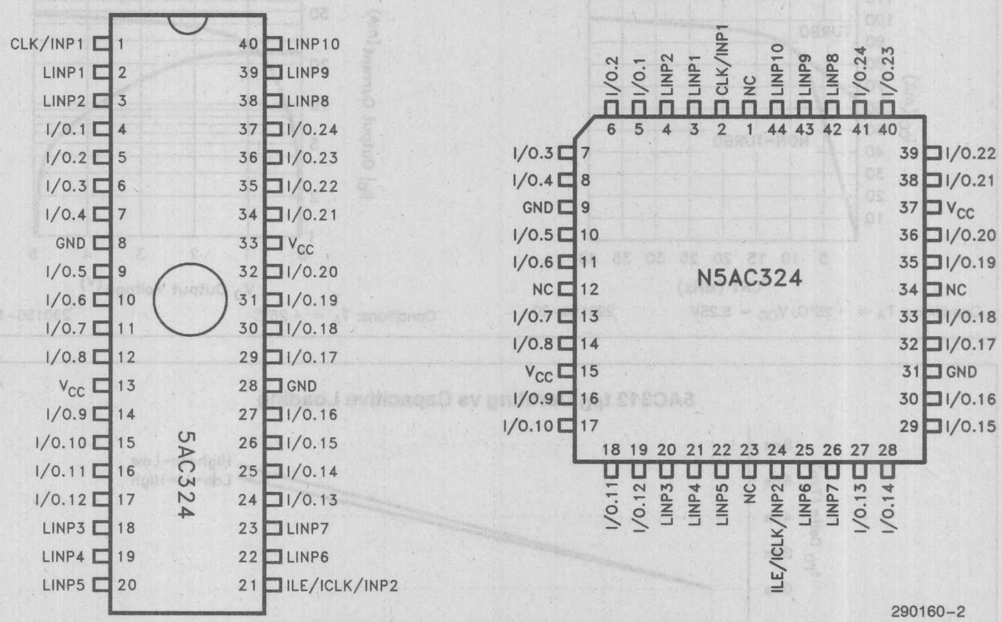
$T_A = +25°C$
$V_{CC} = 5.0V$

290156-21

intel®

5AC324
1-MICRON CMOS 24-MACROCELL PLD

- **High-Performance LSI Semi-Custom Logic Alternative to Low-end Gate Arrays, TTL, 74HC SSI and MSI Logic, and PLDs**
- **High Speed t_{PD} 25 ns, 66 MHz Performance Pipelined, 33.3 MHz w/ Feedback**
- **24 Macrocells with Programmable I/O Architecture; Up to 36 Inputs (12 Dedicated, 24 I/O)**
- **10 Programmable Inputs Configurable as Latches, Registers, or Flow-Through**
- **1 Flow-Through Input or Global CLK Pin; 1 Flow-Through Input or Global ILE/ICLK Pin**
- **Programmable AND, Allocatable OR Design Allows up to 16 P-Terms per Macrocell**
- **Software-Supported P-Term Allocation Between Adjacent Macrocells**
- **Programmable Output Registers Configurable as D, T, JK, or SR Types**
- **Dual Feedback on All Macrocells for Implementing Buried Registers with Bidirectional I/O**
- **2 P-Terms on All Macrocell Control Signals**
- **Programmable Low-Power Option for "Stand-by" Operation; 150 μA Typical Standby Current**
- **UV Erasable (CerDIP) EPROM Technology or OTP**
- **100% Generically Tested EPROM Logic Control Array**
- **JEDEC Pinout**
- **Available in 40-pin CerDIP/PDIP and 44-Pin PLCC Packages**
  (See Packaging Spec., Order Number 240800, Package Type D, P, and N)



290160-1

290160-2

Figure 1. 5AC324 Pinout Diagrams

INTRODUCTION

The Intel 5AC324 CMOS PLD (Programmable Logic Device) is a high integration device that overcomes the primary limitations of standard PLDs. Due to a proprietary I/O architecture and macrocell structure, the 5AC324 is capable of implementing high performance logic functions more effectively than previously possible. The 5AC324 can be used as an alternative to low-end gate arrays, multiple programmable logic devices, or LS-, HC-, or HCT SSI and MSI logic devices. Input and macrocell features for the 5AC324 are a superset of features offered on other PLD-type products.

The 5AC324 uses advanced CMOS EPROM cells as logic control elements instead of poly-silicon fuses. This technology allows the device to operate at levels necessary in high performance systems while significantly reducing power consumption. Its programmable standby mode reduces power to near zero in applications where a slight speed loss is traded for power savings.

ARCHITECTURE DESCRIPTION

The architecture of the 5AC324 is based on the familiar "Sum-Of-Products" programmable AND, fixed OR structure. This structure is then surrounded by powerful, programmable macrocells and inputs. The 5AC324 can implement both combinatorial and sequential logic functions through a highly flexible macrocell and I/O structure. The architecture of the device supports both combinatorial-register and register-combinatorial-register forms of logic to easily accomodate state machine designs.

Figure 2 shows a global view of the 5AC324 architecture. The 5AC324 contains a total of 24 I/O programmable macrocells, 10 programmable input structures, and two clock inputs that can be programmed to function either as combinatorial inputs or clock inputs for the input structures and macrocells.

Each of the ten programmable inputs can be individually configured as a latch, register or flow-through

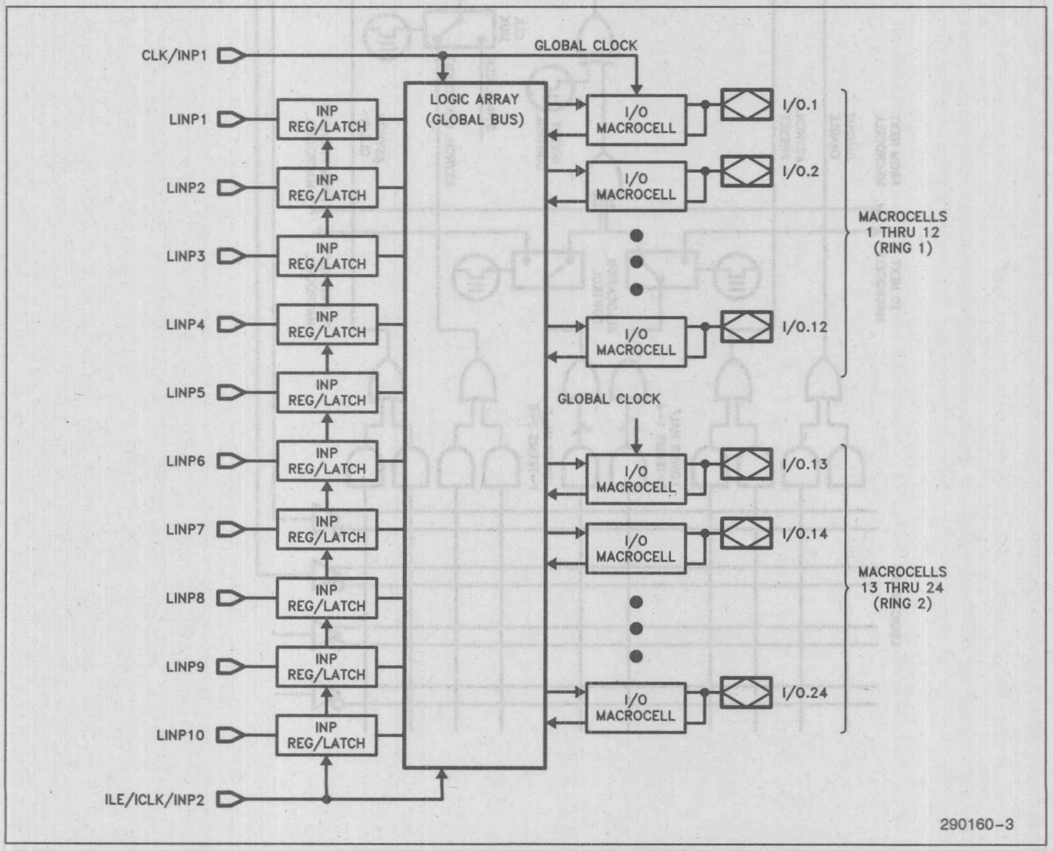


Figure 2. 5AC324 Global Architecture

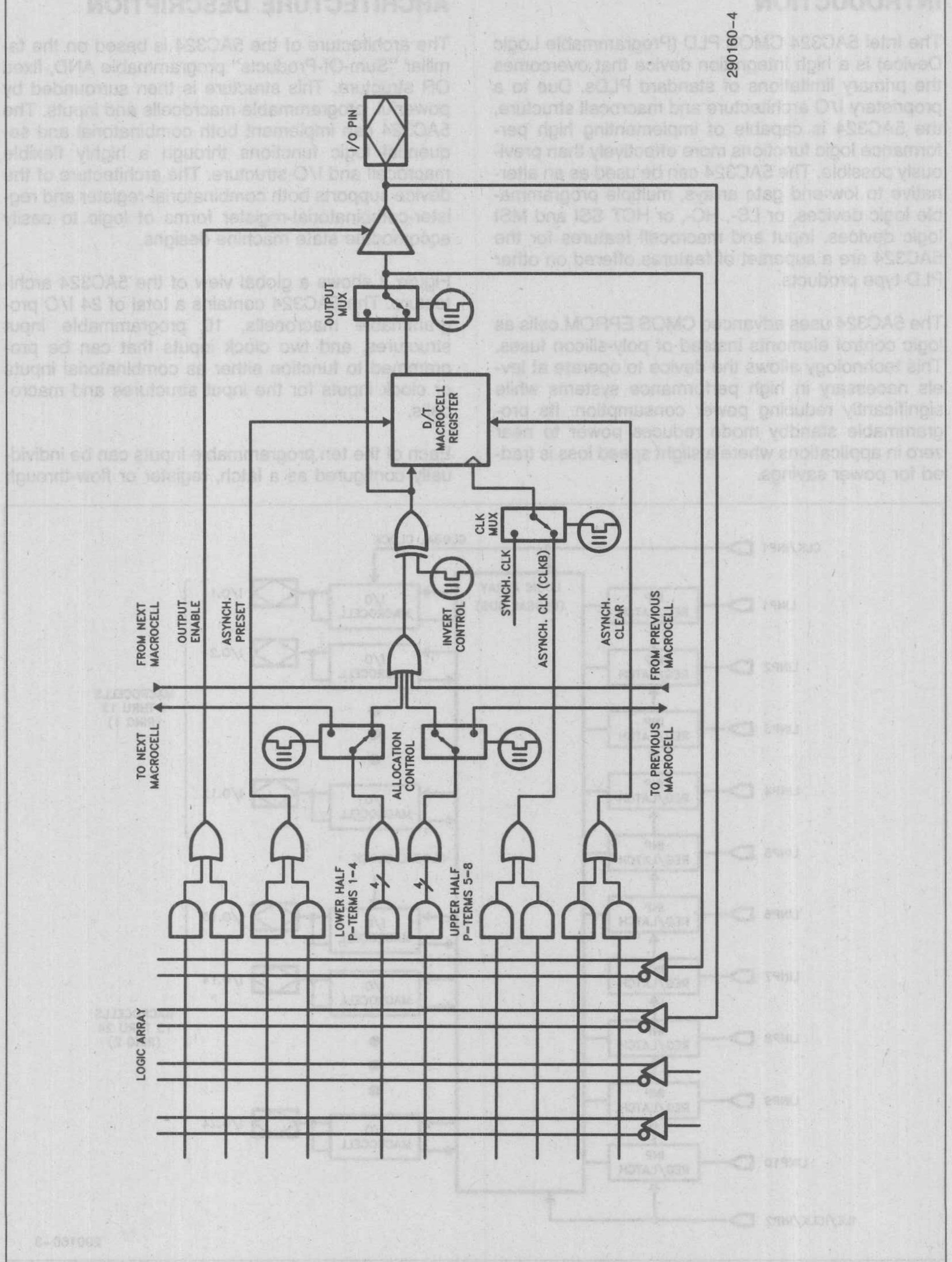


Figure 3. 5AC324 Macrocell Architecture

input. Input latches/registers can be synchronously or asynchronously clocked.

Figure 3 shows the basic architecture of each of the 24 macrocells in the 5AC324. Each macrocell contains 16 p-terms (product terms), with 8 p-terms available for the global array and 8 p-terms dedicated to the four control signals: OE, PRESET, CLEAR, and ASYNCH. CLK. The 8 p-terms from the logic array are organized as a user-programmable AND array and a user-configurable OR array. The inputs to the AND array originate from the true and complement signals from the programmable input structure, the dedicated inputs, and the 48 feedback paths from the 24 I/O macrocells to the global bus. This global bus simplifies designing with the device by eliminating the need to partition a circuit to fit into a local/global internal bus structure.

PROGRAMMABLE INPUTS

Figure 4 shows a block diagram of the 5AC324 input structure. The device contains 10 user-programmable inputs that can be individually configured to operate in one of five modes:

- input register (D-register), synchronously clocked
- input register (D-register), asynchronously clocked
- input latch, (D-latch), synchronously clocked
- input latch, (D-latch), asynchronously clocked
- Flow-through input

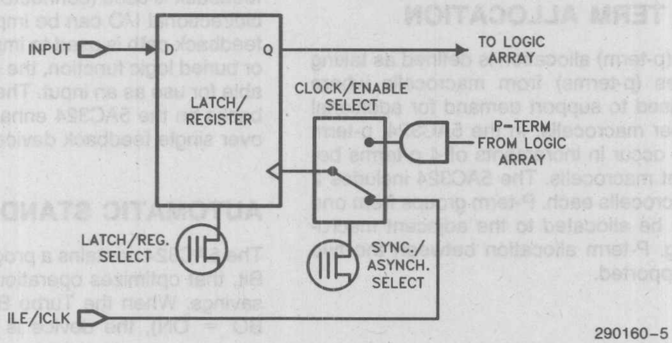
Configuration is accomplished through the programming of EPROM architecture control bits via the logic compiler and programmer software. If synchronous operation is selected, the ILE/ICLK pin is used as a global latch/clock to all input latch/register structures. For asynchronous operation, a separate product term in the array is used to derive the ILE/ICLK signal for each input structure. Because the clock signal for each programmable input can be individually selected, a mix between synchronously and asynchronously clocked inputs is possible. Software can configure each input structure as a flow-through input by selecting a latch and tying the ILE p-term to VCC. Data is latched/clocked on the falling edge of ILE/ICLK (synchronous mode). ILE/ICLK can function as an input to the logic array at the same time as it is used to synchronously clock the input registers.

MACROCELLS

Each of the 24 macrocells in the device contains 8 p-terms to support logic functions and 8 p-terms for control signals. The 8 p-terms for logic functions are subdivided into 2 groups, each with 4 p-terms. This grouping of p-terms supports the proprietary p-term allocation scheme in the 5AC324. Each macrocell also provides dual feedbacks to the logic array, which results in more efficient macrocell/pin usage than possible with single feedbacks.

Register Configuration

Each macrocell can be configured as a D, T, RS, or JK register. The 8 p-terms for control functions are organized so that 2 p-terms support each of the 4 control signals: Output Enable (OE), asynchronous I/O preset (PRESET), asynchronous I/O reset (CLEAR), and asynchronous I/O register clock (ASYNCH. CLK). Availability of 2 p-terms per control signal is another feature that increases the efficiency of the device by reducing the need to use intermediate macrocells sometimes needed to implement control functions.



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NOTE:
Software implements a direct (flow-through) input by selecting an asynchronous latch and tying its control P-term to V_{CC}.

Figure 4. 5AC324 Programmable Input Structure

synchronously clock any or all macrocell registers. When CLK is not used as a synchronous clock, it functions only as a dedicated input to the logic array. CLK can be used as an input to the logic array at the same time as it is used as a macrocell clock.

Combinatorial Configuration

The macrocell register can be bypassed to implement combinatorial logic functions. When configured to provide combinatorial logic, only the OE control signal is used.

Invert Select Bit

An invert select EPROM bit is used to invert the product term input into each macrocell register, including double inputs on JK and SR registers. This invert option allows the highest possible logic utilization by use of DeMorgan's logic inversion.

LOGIC ARRAY

Each intersecting point in the logic array contains a programmable EPROM connection. Initially (erased state), all connections are complete, i.e., both true and complement states of all signals are connected to each p-term.

Connections are opened during programming. When both the true and complement connections exist, a logical false results on the output of the AND gate. If both the true and complement connections of a signal are programmed "open", then a logic "don't care" results for that signal. If all connections for a p-term are programmed open, then a logical true results on the output of the AND gate.

PRODUCT TERM ALLOCATION

Product Term (p-term) allocation is defined as taking logic resources (p-terms) from macrocells where they are not used to support demand for additional p-terms in other macrocells. In the 5AC324, p-term allocation can occur in increments of 4 p-terms between adjacent macrocells. The 5AC324 includes 2 rings of 12 macrocells each. P-term groups from one macrocell can be allocated to the adjacent macrocell in the ring. P-term allocation between the two rings is not supported.

EXAMPLE:

Figure 5 shows a p-term allocation example. In this example, the logic function in macrocell 4 requires 16 p-terms. In this case, software allocates 4 p-terms from the previous macrocell in Ring 1 (macrocell 5) and 4 p-terms from the next macrocell (macrocell 3) to accumulate a total of 16 p-terms (8 + 4 + 4). This implementation leaves macrocells 3 and 5 with a remainder of 4 p-terms. These remaining p-terms can also be allocated away to, or supplemented with p-terms from, their adjacent macrocells in Ring 1 (macrocells 2 and 6).

With this scheme, any macrocell inside the device can support logic functions requiring between 0 and 16 p-terms. P-terms allocated away do not affect that macrocell's output structure. The input to the macrocell can be tied to VCC or GND, even when all p-terms have been allocated away. Thus the register and all control signals are still available for use if needed.

Figure 6 shows adjacent macrocells in the 5AC324. Table 1 shows the previous and next macrocells for each macrocell in the device, along with the corresponding allocation ring. P-term allocation is implemented automatically in the development software and is transparent to the user. Users can still use explicit pin assignment, but should assign pins in a way that does not conflict with p-term allocation.

Software support allows the control signals on macrocells to be used to implement simple logic functions even when all the input p-terms have been allocated to adjacent macrocells.

DUAL-FEEDBACK/BURIED LOGIC

Macrocell output can be fed back to the logic array on either one of the two feedback paths. If the pin feedback is used (connected after the output buffer), bidirectional I/O can be implemented. If the internal feedback path is used to implement a buried register or buried logic function, the pin feedback is still available for use as an input. The availability of dual feedbacks on the 5AC324 enhances resource efficiency over single feedback devices.

AUTOMATIC STAND-BY MODE

The 5AC324 contains a programmable bit, the Turbo Bit, that optimizes operation for speed or for power savings. When the Turbo Bit is programmed (TURBO = ON), the device is optimized for maximum

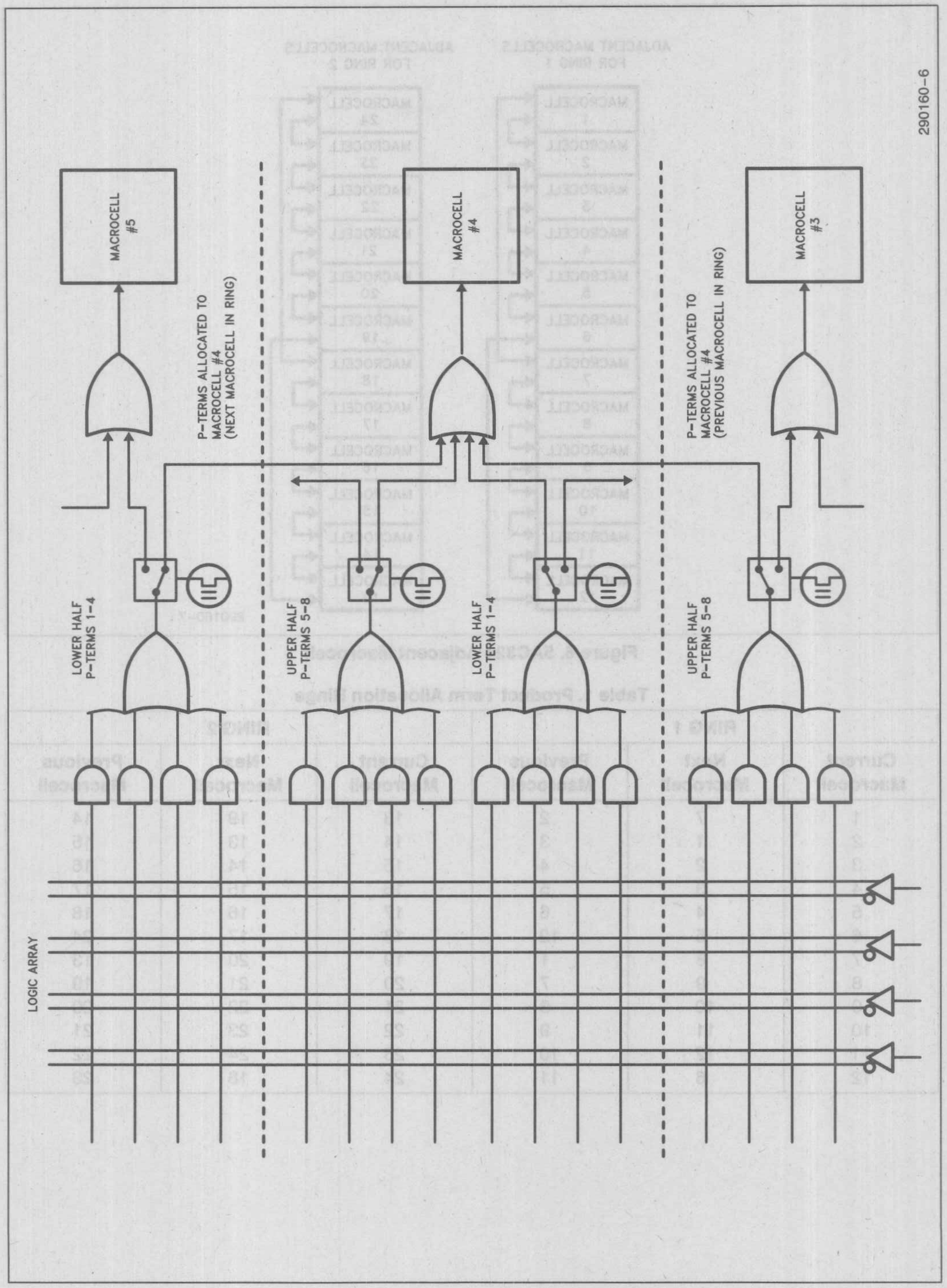


Figure 5. P-Term Allocation Example (8 + 4 + 4)

2

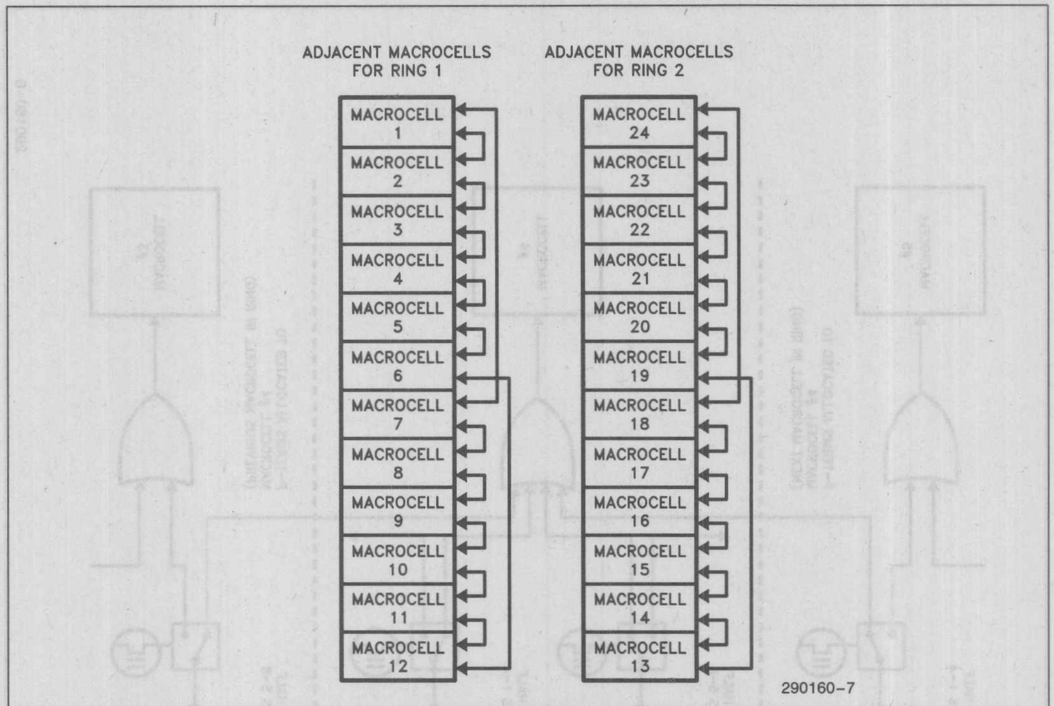


Figure 6. 5AC324 Adjacent Macrocell

Table 1. Product Term Allocation Rings

RING 1			RING 2		
Current Macrocell	**Next Macrocell**	**Previous Macrocell**	**Current Macrocell**	**Next Macrocell**	**Previous Macrocell**
1	7	2	13	19	14
2	1	3	14	13	15
3	2	4	15	14	16
4	3	5	16	15	17
5	4	6	17	16	18
6	5	12	18	17	24
7	8	1	19	20	13
8	9	7	20	21	19
9	10	8	21	22	20
10	11	9	22	23	21
11	12	10	23	24	22
12	6	11	24	18	23

speed. When the Turbo Bit is not programmed (TURBO = OFF), the device is optimized for power savings by entering standby mode during periods of inactivity.

Figure 7 shows the device entering standby mode approximately 100 ns after the last input or I/O transition. When the next input or I/O transition is detected, the device returns to active mode. Wakeup time adds an additional 20 ns to the propagation delay through the device as measured from the first transition. No delay will occur if an output is dependent on more than one input and the last of the inputs changes after the device has returned to active mode.

After erasure, the Turbo Bit is unprogrammed (OFF); automatic standby mode is enabled. When the Turbo Bit is programmed (ON), the device never enters standby mode.

POWER-ON CHARACTERISTICS

On V_{CC} power-up, the 5AC324 registers are reset to a logic low. Input latch/register output (to the logic array) are also set to a logic low. 5AC324 inputs and outputs begin responding approximately 20 μS after V_{CC} power-up or after a power-loss/power-up sequence. After power-up, macrocells can be preset to a logic high via the PRESET control signal for each macrocell.

ERASED STATE CONFIGURATION

After erasure and prior to programming, all macrocells are configured as combinatorial outputs with output buffers three-stated. Inputs are configured as synchronous registers.

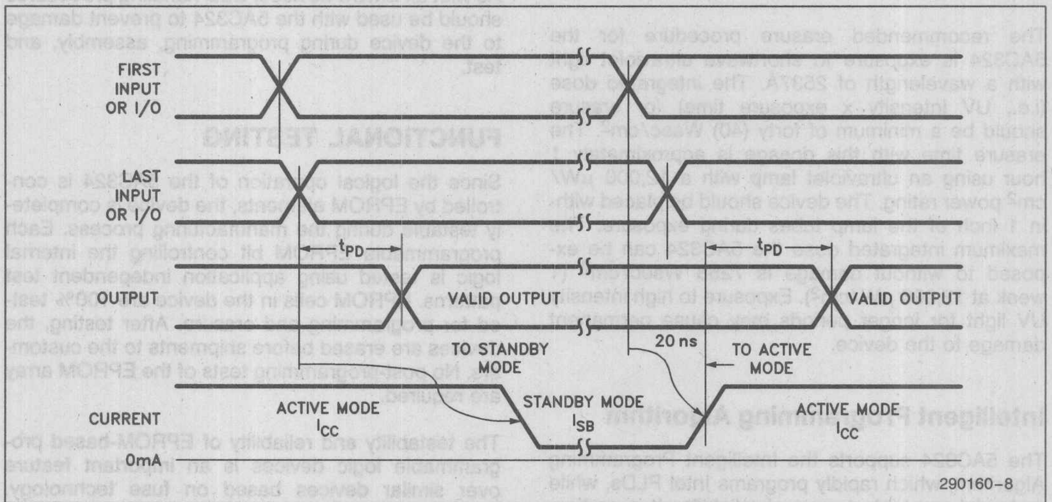


Figure 7. 5AC324 Standby and Active Mode Transitions

ERASURE CHARACTERISTICS

Erasure time for the 5AC324 is 1 hour at 12,000 $\mu W/cm^2$ with a 2537Å UV lamp.

Erasure characteristics of the device are such that erasure begins to occur upon exposure to light with wavelengths shorter than approximately 4000Å. It should be noted that sunlight and certain types of flourescent lamps have wavelengths in the 3000Å-4000Å range. Data shows that constant exposure to room level flourescent lighting could erase the typical 5AC324 in approximately six years, while it would take approximately two weeks to erase the device when exposed to direct sunlight. If the device is to be exposed to these lighting conditions for extended periods of time, conductive opaque labels should be placed over the device window to prevent unintentional erasure.

The recommended erasure procedure for the 5AC324 is exposure to shortwave ultraviolet light with a wavelength of 2537Å. The integrated dose (i.e., UV intensity x exposure time) for erasure should be a minimum of forty (40) $Wsec/cm^2$. The erasure time with this dosage is approximately 1 hour using an ultraviolet lamp with a 12,000 $\mu W/cm^2$ power rating. The device should be placed within 1 inch of the lamp tubes during exposure. The maximum integrated dose the 5AC324 can be exposed to without damage is 7258 $Wsec/cm^2$ (1 week at 12,000 $\mu W/cm^2$). Exposure to high intensity UV light for longer periods may cause permanent damage to the device.

Intelligent Programming Algorithm

The 5AC324 supports the Intelligent Programming Algorithm, which rapidly programs Intel PLDs, while maintaining a high degree of reliability. It is particularly suited for production programming environments. This method ensures reliability as the incremental programming margin of each bit has been verified during programming. Programming voltage and waveform specifications are available by request from Intel to support programming the device.

LATCH-UP IMMUNITY

All of the input, I/O, and clock pins of the device have been designed to resist latch-up which is inherent in inferior CMOS structures. The 5AC324 is designed with Intel's proprietary 1-micron CMOS EPROM process. Thus, each of the pins will not experience latch-up with currents up to ±100 mA and voltages ranging from −0.5V to (V_{CC} + 0.5V). The programming pin is designed to resist latch-up to the 13.5V maximum device limit.

DESIGN RECOMMENDATIONS

For proper operation, it is recommended that all input and output pins be constrained to the voltage range GND ≤ (V_{IN} or V_{OUT}) ≤ V_{CC}. All unused inputs and I/Os should be tied high or low to minimize power consumption (do not leave them floating). A power supply decoupling capacitor of at least 0.2μF must be connected directly between each V_{CC} and GND pin.

As with all CMOS devices, ESD handling procedures should be used with the 5AC324 to prevent damage to the device during programming, assembly, and test.

FUNCTIONAL TESTING

Since the logical operation of the 5AC324 is controlled by EPROM elements, the device is completely testable during the manufacturing process. Each programmable EPROM bit controlling the internal logic is tested using application independent test patterns. EPROM cells in the device are 100% tested for programming and erasure. After testing, the devices are erased before shipments to the customers. No post-programming tests of the EPROM array are required.

The testability and reliability of EPROM-based programmable logic devices is an important feature over similar devices based on fuse technology. Fuse-based programmable logic devices require a user to perform post-programming tests to insure device functionality. During the manufacturing process, tests on fuse-based parts can only be performed in very restricted ways in order to avoid preprogramming the array.

ADF PRIMITIVES SUPPORTED

The following ADF primitives are supported by this device:

INP	NOTF
LINP	JOJF
RINP	JONF
CONF	SONF
COCF	SOSF
COIF	TOIF
RONF	TONF
ROIF	TOTF
RORF	CLKB
NOCF	LINB
NORF	
NOJF	
NOSF	

SOFTWARE SUPPORT

Full logic compilation and functional simulation for the 5AC324 is supported by PLDshell Plus software. The GUPI 40D44J provides programming support on Intel programmers.

PLDshell Plus design software is Intel's user-friendly design tool for μPLD design. PLDshell Plus allows users to incorporate their preferred text editor, programming software, and additional design tools into an easy-to-use, menued design environment that includes Intel's PLDasm logic compiler and simulation software along with disassembly, conversion, and translation utilities. The PLDasm compiler and simulator software accepts industry-standard PDS source files that express designs as Boolean equations, truth tables, or state machines. On-line help, datasheet briefs, technical notes, and error message information, along with waveform viewing/printing capability make the design task as easy as possible. PLDshell Plus software is available from Intel Literature channels or from your local Intel sales representative.

Tools that support schematic capture and timing simulation for the 5AC324 are available. Please refer to the "Development Tools" section of the Programmable Logic handbook.

The 5AC324 is also supported by third-party logic compilers such as ABEL†, CUPL†, PLDesigner†, Log/IC, etc. Programming support is provided by third-party programmer companies such as Data I/O, Logical Devices, STAG, etc. Please refer to the "Third-Party Support" lists in the *Programmable Logic* handbook for complete information and vendor contacts.

ORDERING INFORMATION

t_{PD} (ns)	t_{CO} (ns)	f_{MAX} (MHz)	Order Code	Package	Operating Range
25	17.8	66	N5AC324-25	PLCC	Commercial
			P5AC324-25	PDIP	
			D5AC324-25	*CERDIP	
30	20	50	N5AC324-30	PLCC	Commercial
			P5AC324-30	PDIP	
			D5AC324-30	*CERDIP	
30	20	50	TN5AC324-30	PLCC	Industrial

*Windowed package allows UV erase.

†ABEL is a trademark of Data I/O Corporation. CUPL is a trademark of Logical Devices, Inc. PLDesigner is a trademark of MINC, Inc. Log/IC is a trademark of ISDATA, Inc.

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage (V_{CC})(1) .... −2.0V to +7.0V

Programming Supply Voltage (V_{PP})(1) .... −2.0V to +13.5V

D.C. Input Voltage (V_I)(1,2) .... −0.5V to V_{CC} +0.5V

Storage Temperature (T_{stg}) ..... −65°C to +150°C

Ambient Temperature (T_{amb})(3) ... −10°C to +85°C

NOTES:

1. Voltage with respect to GND.
2. Minimum D.C. input is −0.5V. During transitions, the inputs may undershoot to −2.0V or overshoot to +7.0V less than 20 ns under no load conditions.
3. Under bias. Extended Temperature versions are also available.

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

**WARNING:* Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage	4.75	5.25	V
V_{IN}	Input Voltage	0	V_{CC}	V
V_O	Output Voltage	0	V_{CC}	V
T_A	Operating Temperature	0	+70	°C
t_R	Input Rise Time		500	ns
t_F	Input Fall Time		500	ns

D.C. CHARACTERISTICS (T_A = 0°C to +70°C, V_{CC} = 5.0V ±5%)

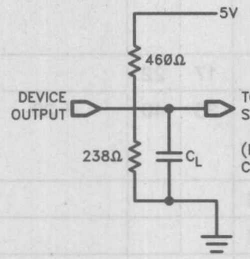
Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}(4)	High Level Input Voltage	2.0		V_{CC} +0.3	V	
V_{IL}(4)	Low Level Input Voltage	−0.3		0.8		
V_{OH}(5)	High Level Output Voltage	2.4			V	I_O = −4.0 mA D.C., V_{CC} = min.
V_{OL}	Low Level Output Voltage			0.45	V	I_O = 8.0 mA D.C., V_{CC} = min.
I_I	Input Leakage Current			±10	μA	V_{CC} = max., GND < V_{IN} < V_{CC}
I_{OZ}	Output Leakage Current			±10	μA	V_{CC} = max., GND < V_{OUT} < V_{CC}
I_{SC}(6)	Output Short Circuit Current	−30		−90	mA	V_{CC} = max., V_{OUT} = 0.5V

D.C. CHARACTERISTICS (T_A = 0°C to +70°C, V_{CC} = 5.0V ±5%) (Continued)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
I_{SB}(7)	Standby Current		150	500	μA	V_{CC} = max., V_{IN} = V_{CC} or GND, Standby Mode
I_{CC}	Power Supply Current (See I_{CC} vs Freq. Graph)		20		mA	V_{CC} = max., V_{IN} = V_{CC} or GND, No Load, f_{IN} = 1 MHz, Active Mode (Turbo = Off), Device Prog. as Two 12-Bit Counters

NOTES:
4. Absolute values with respect to device GND; all over and undershoots due to system or tester noise are included.
5. I_O at CMOS levels (3.84V) = −2 mA.
6. Not more than 1 output should be tested at a time. Duration of that test should not exceed 1 second.
7. With Turbo Bit Off, device automatically enters standby mode approximately 100 ns after last input transition.

A.C. TESTING LOAD CIRCUIT



C_L = 30 pF

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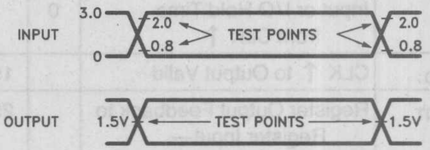
A.C. TESTING INPUT, OUTPUT WAVEFORM



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A.C. Testing: Inputs are driven at 3.0V for a Logic "1" and 0V for a Logic "0". Timing Measurements are made at 2.0V for a Logic "1" and 0.8V for a Logic "0" on inputs. Outputs are measured at a 1.5V point. Device input rise and fall times < 6 ns.

CAPACITANCE

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
C_{IN}	Input Capacitance			8	pF	V_{IN} = 0V, f = 1.0 MHz
C_{OUT}	I/O Capacitance			15	pF	V_{OUT} = 0V, f = 1.0 MHz
C_{CLK}	Clock Pin Capacitance			15	pF	V_{IN} = 0V, f = 1.0 MHz
C_{VPP}	V_{PP} Pin (LIN3)			25	pF	V_{IN} = 0V, f = 1.0 MHz

COMBINATORIAL MODE A.C. CHARACTERISTICS

(T_A = 0°C to +70°C, V_{CC} = 5.0V ±5%, Turbo Bit On)(8)

Symbol	Parameter	5AC324-25			5AC324-30			5AC324-35			Non-Turbo(9) Mode	Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
t_{PD}	Input or I/O to Output Valid		20	25		25	30		30	35	+20	ns
t_{PZX}(10)	Input or I/O to Output Enable		20	25		25	30		30	35	+20	ns
t_{PXZ}(10)	Input or I/O to Output Disable		20	25		25	30		30	35	+20	ns
t_{CLR}	Asynch. Reset to Q Reset		20	25		25	30		30	35	+20	ns
t_{SET}	Asynch. Set to Q Set		20	25		25	30		30	35	+20	ns

NOTES:
8. Typical values are at T_A = +25°C, V_{CC} = 5V, Active Mode.
9. If device is operated with Turbo bit Off (Non-Turbo Mode) and the device is inactive for approx. 100 ns, increase time by amount shown.
10. t_{PZX} and t_{PXZ} measured at ±0.5V from steady-state voltage as driven by spec. output load. t_{PXZ} measured with C_L = 5 pF.

SYNCHRONOUS CLOCK MODE (MACROCELLS) A.C. CHARACTERISTICS

(T_A = 0°C to +70°C, V_{CC} = 5.0V ±5%, Turbo Bit On)(8)

Symbol	Parameter	5AC324-25			5AC324-30			5AC324-35			Non-Turbo(9) Mode	Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
f_{MAX}	Maximum Frequency (Pipelined) ($1/t_{CW}$)—No Feedback		80	66		66	50		50	40		MHz
f_{CNT1}	Maximum Frequency ($1/t_{SU} + t_{CO}$) —External Feedback		40	33		33.3	25		27	21.2		MHz
f_{CNT2}	Maximum Frequency ($1/t_{CNT}$) —Internal Feedback		40	33.3		33.3	28.5		28.5	25		MHz
t_{SU1}	Input Setup Time to CLK ↑	12.5	10		20	15		25	20		+20	ns
t_{SU2}	I/O Setup Time to CLK ↑	12	10		20	15		25	20		+20	ns
t_H	Input or I/O Hold Time from CLK ↑	0			0			0				ns
t_{CO}	CLK ↑ to Output Valid		15	17.8		15	20		17	22		ns
t_{CNT}	Register Output Feedback to Register Input— Internal Path		25	30		30	35		35	40	+20	ns
t_{CH}	Clock High Time	7			9			11				ns
t_{CL}	Clock Low Time	7			9			11				ns
t_{CW}	Minimum Clock Period	15			20			25				ns

SYNCHRONOUS CLOCK MODE (INPUT STRUCTURE) A.C. CHARACTERISTICS

(T_A = 0°C to +70°C, V_{CC} = 5.0V ±5%, Turbo Bit On)(8)

Symbol	Parameter	5AC324-25			5AC324-30			5AC324-35			Non-Turbo(9) Mode	Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
f_{MAXI}	Maximum Frequency ($1/t_{CWI}$)		80	66		60	50		50	40		MHz
t_{SUIR}	Input Register Setup Time Before ILE/ICLK ↓	1			2.5			5				ns
t_{ESUI}(11)	Input Latch Setup Time Before ILE ↑	1			2.5			5				ns
t_{COI}	ICLK ↓ to Comb. Output		25	30		30	35		35	40	+20	ns
t_{EOI}	ILE ↑ to Comb. Output		25	30		30	35		35	40	+20	ns
t_{HI}	Input Hold after ICLK ↓	8			9			10				ns
t_{EHI}	Input Hold after ILE ↓	7			8			9				ns
t_{CHI}	ILE/ICLK High Time	7			9			11				ns
t_{CLI}	ILE/ICLK Low Time	7			9			11				ns
t_{CWI}	Minimum Input Clock Period	15			20			25				ns

ASYNCHRONOUS CLOCK MODE (MACROCELLS) A.C. CHARACTERISTICS

(T_A = 0°C to +70°C, V_{CC} = 5.0V ±5%, Turbo Bit On)(8)

Symbol	Parameter	5AC324-25			5AC324-30			5AC324-35			Non-Turbo(9) Mode	Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
f_{AMAX}	Max. Frequency (Pipelined) ($1/t_{ACW}$)—No Feedback		80	66		60	50		50	40		MHz
f_{ACNT_1}	Max. Frequency ($1/t_{ASU} + t_{ACO}$) External Feedback		32.2	27.7		27	23.8		22.2	20		MHz
f_{ACNT_2}	Max. Frequency ($1/t_{ACNT}$) Internal Feedback		40	33.3		33.3	28.5		28.5	25		MHz
t_{ASU1}	Input Setup Time to Asynch. CLK	11			12			15			+20	ns
t_{ASU2}	I/O Setup Time to Asynch. CLK	11			12			15			+20	ns
t_{AH}	Input or I/O Hold Time from Asynch. CLK	3	0		4	0		5	0			ns
t_{ACO}	Asynch. CLK to Output Valid		20	25		25	30		30	35	+20	ns
t_{ACNT}	Asynch. Output Feedback to Register Input - Internal Path		25	30		30	35		35	40	+20	ns
t_{ACH}	Asynch. CLK High Time	7			9			11			+20	ns
t_{ACL}	Asynch. CLK Low Time	7			9			11			+20	ns
t_{ACW}	Asynch. CLK Period	15			20			25			+20	ns

ASYNCHRONOUS CLOCK MODE (INPUT STRUCTURE) A.C. CHARACTERISTICS

(T_A = 0°C to +70°C, V_{CC} = 5.0V ±5%, Turbo Bit On)(8)

Symbol	Parameter	5AC324-25			5AC324-30			5AC324-35			Non-Turbo(9) Mode	Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
f_{AMAXI}	Maximum Frequency Input Register ($1/t_{ACWI}$)		80	66		60	50		50	40		MHz
t_{ASUIR}	Input Register Setup Time Before Asynch. ICLK	−5			−5			−5				ns
t_{AESUI}(11)	Input Latch Setup Time Before Asynch. ILE	−5			−5			−5				ns
t_{ACOI}	Asynch. ICLK to Comb. Output		25	30		30	35		45	50	+20	ns
t_{AEOI}	Asynch. ILE to Comb. Output		25	30		30	45		45	50	+20	ns
t_{AHI}	Input Hold after Asynch. ICLK	15			18			20				ns
t_{AEHI}	Input Hold after Asynch. ILE	14			17			19				ns
t_{ACHI}	Asynch. ILE/ICLK High Time	7			9			11			+20	ns
t_{ACLI}	Asynch. ILE/ICLK Low Time	7			9			11			+20	ns
t_{ACWI}	Minimum Input Clock Period	15			20			25			+20	ns

NOTE:
11. This specification must be met to guarantee t_{EOI}. When ILE goes high before data is valid, use t_{PD} instead of t_{EOI}.

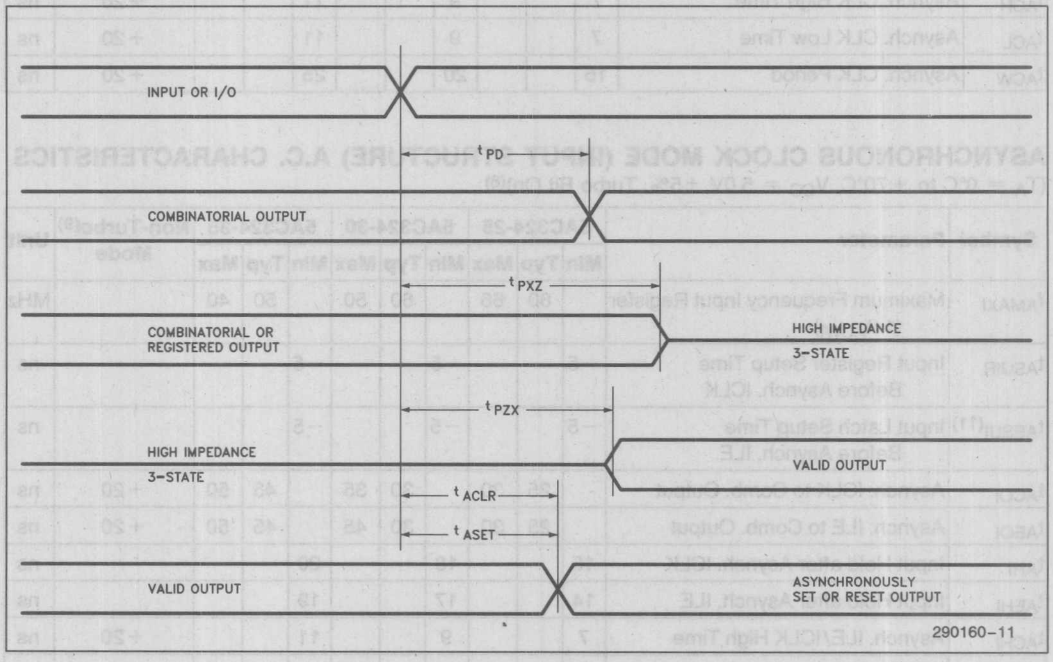
(T_A = 0°C to +70°C, V_{CC} = 5.0V ±5%, Turbo Bit On)(9)

Symbol	Parameter	5AC324-25			5AC324-30			5AC324-35			Non-Turbo(9) Mode	Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
t_{C1C2}(12)	Synchronous ILE/ICLK to Synchronous Macrocell CLK	20			25			30			+20	ns
	Synchronous ILE/ICLK to Asynchronous Macrocell CLK	12.5			15			18			+20	ns
	Asynchronous ILE/ICLK to Synchronous Macrocell CLK	40			45			50			+20	ns
	Asynchronous ILE/CLK to Asynchronous Macrocell CLK	20			25			30			+20	ns

NOTE:
12. Times for SETUP, HOLD, and OUTPUT VALID are shown in previous tables.

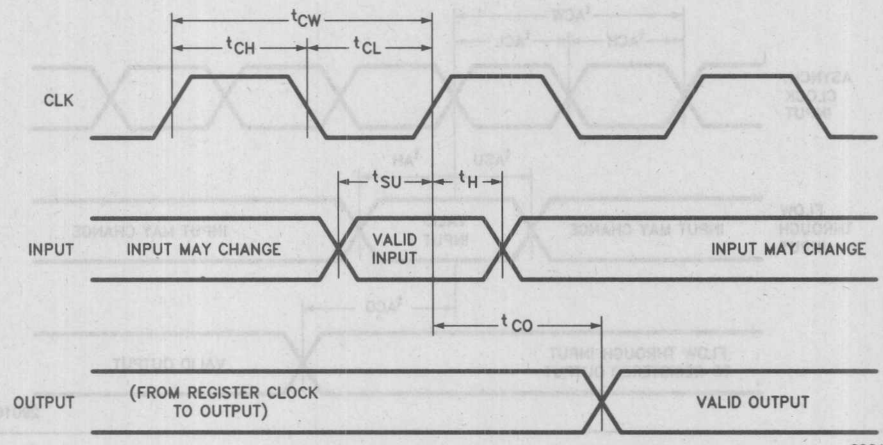
SWITCHING WAVEFORMS

COMBINATORIAL MODE



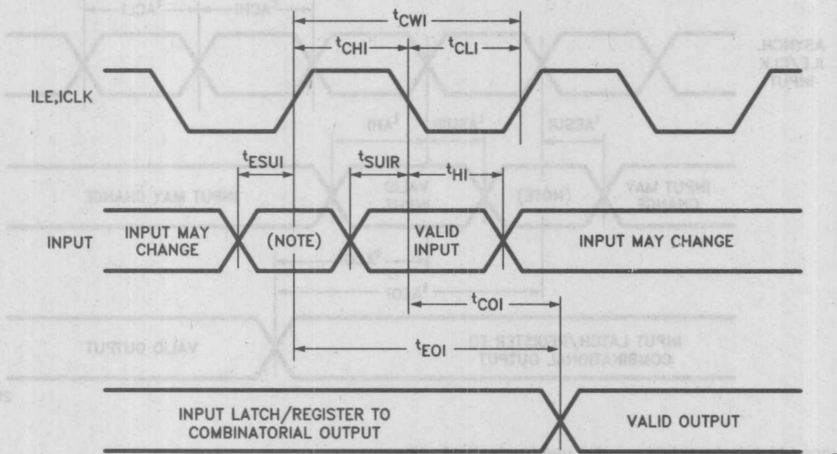
290160-11

SYNCHRONOUS CLOCK MODE (MACROCELLS)



290160-12

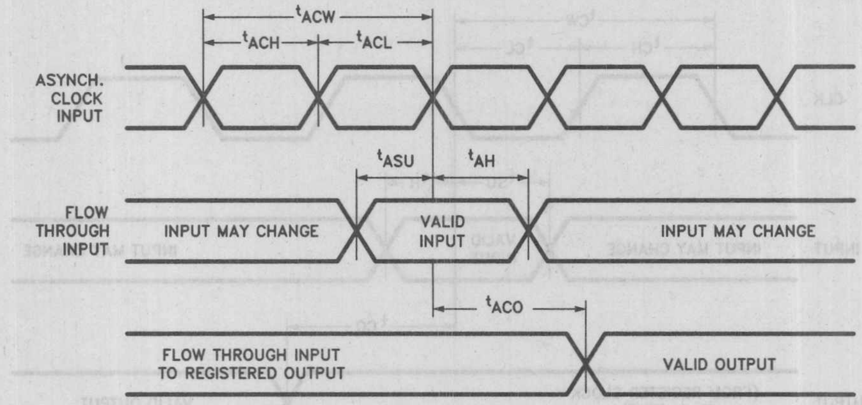
SYNCHRONOUS CLOCK MODE (INPUT STRUCTURE)



290160-13

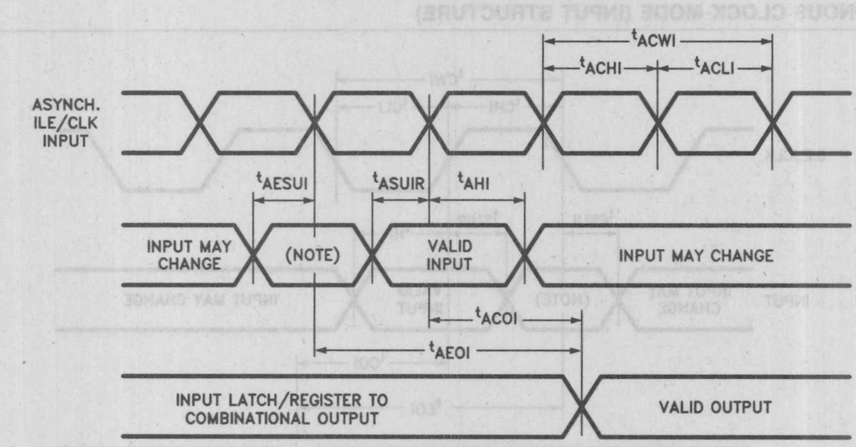
NOTE:
When ILE goes high before data is valid, use t_{PD} instead of t_{EOI}.

ASYNCHRONOUS CLOCK MODE (MACROCELLS)



290160–14

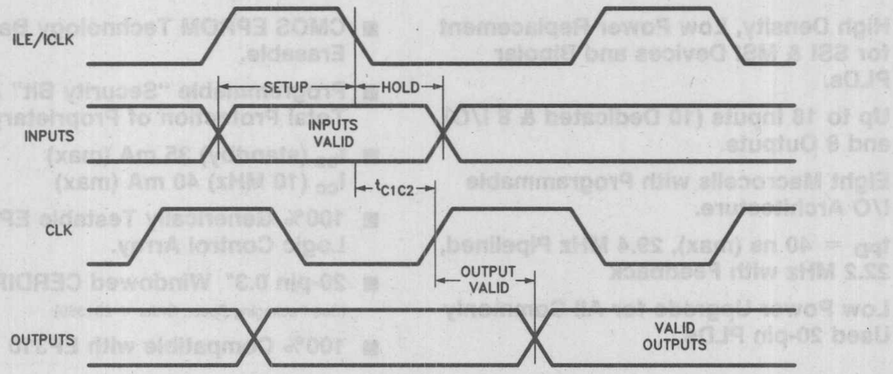
ASYNCHRONOUS CLOCK MODE (INPUT STRUCTURE)



290160–15

NOTE:
When ILE goes high before data is valid, use t_{PD} instead of t_{AEOI}.

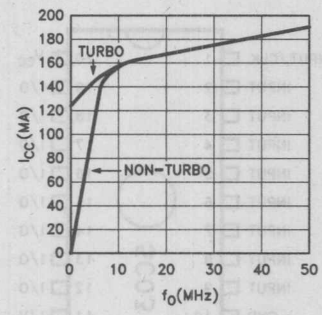
INPUT-CLOCK-TO-MACROCELL CLOCK TIMING (CLOCKED PIPELINED DATA)



290160–16

CLOCK, SETUP, HOLD, and OUTPUT VALID times are dependent on synchronous/asynchronous clocking and are listed in the specification tables.

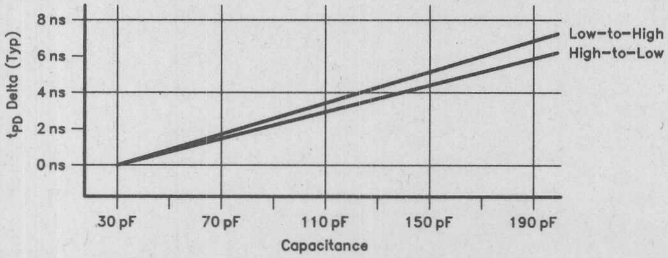
5AC324 I_{CC} vs. Frequency



290160–17

Conditions: $T_A = 25°C$
$V_{CC} = 5.0V$

5AC324 t_{PD} Derating vs. Capacitive Loading

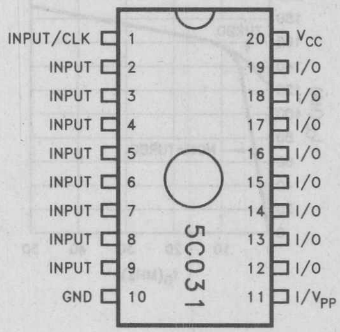


290160–18

Conditions: $T_A = 25°C$
$V_{CC} = 5.0V$

300 GATE CMOS PLD

- **High Density, Low Power Replacement for SSI & MSI Devices and Bipolar PLDs.**
- **Up to 18 Inputs (10 Dedicated & 8 I/O) and 8 Outputs.**
- **Eight Macrocells with Programmable I/O Architecture.**
- **t_{PD} = 40 ns (max), 29.4 MHz Pipelined, 22.2 MHz with Feedback**
- **Low Power Upgrade for All Commonly Used 20-pin PLDs.**
- **CMOS EPROM Technology Based UV Erasable.**
- **Programmable "Security Bit" Allows Total Protection of Proprietary Designs**
- **I_{CC} (standby) 35 mA (max)**
  I_{CC} (10 MHz) 40 mA (max)
- **100% Generically Testable EPROM Logic Control Array.**
- **20-pin 0.3" Windowed CERDIP Package**
  (See Packaging Spec., Order # 231369)
- **100% Compatible with EP310**



290154-1

Pin Configuration

INTRODUCTION

The Intel 5C031 PLD (Programmable Logic Device) is capable of implementing over 300 equivalent gates of user-customized logic functions through programming. This device can be used to replace bipolar programmable logic arrays and LS TTL and 74HC (CMOS) SSI and MSI logic devices. The 5C031 can also be used as a direct, low-power replacement for almost all common 20-pin fuse-based programmable logic devices. With its flexible programmable I/O architecture, this device has advanced functional capabilities beyond that of typical programmable logic.

The 5C031 PLD uses CMOS EPROM (floating gate) cells as logic control elements instead of fuses. The CMOS EPROM technology reduces power consumption of PLDs to less than 20% of a comparable bipolar device without sacrificing speed performance. In addition, the use of Intel's advanced CMOS II-E EPROM process technology enables greater logic densities to be achieved with superior speed and low-power performance over other comparable devices. EPROM technology allows these devices to be 100% factory tested by programming and erasing all the EPROM logic control elements.

The 5C031 is housed in a windowed 0.3″ 20-pin DIP and has the benefits of being an ideal prototyping tool with its highly flexible I/O architecture.

ARCHITECTURE DESCRIPTION

The architecture of the 5C031 is based on the "Sum of Products" PLA (Programmable Logic Array) structure with a programmable AND array feeding into a fixed OR array. This device can accommodate both combinational and sequential logic functions. A proprietary programmable I/O architecture provides individual selection of either combinational or registered output and feedback signals, all with selectable polarity.

The 5C031 contains 10 dedicated inputs as well as 8 input/output pins. These I/O pins can be individually configured to be inputs, outputs or bi-directional I/O pins. Each of these I/O pins is connected to a macrocell. The 5C031 contains 8 identical macrocells organized as shown in Figure 1.

Each macrocell (see Figure 2) consists of a PLA (programmable logic array) block and an I/O architecture block, which contains a "D" type register. The PLA block consists of eight 36-input AND gates (TRUE & COMPLEMENT of 10 dedicated inputs plus the 8 feedback inputs from the eight macrocells), feeding into an OR gate. The output of this PLA block is fed into the I/O architecture block. The different I/O and feedback options that are achievable from the 5C031 I/O block are shown in Figure 3.

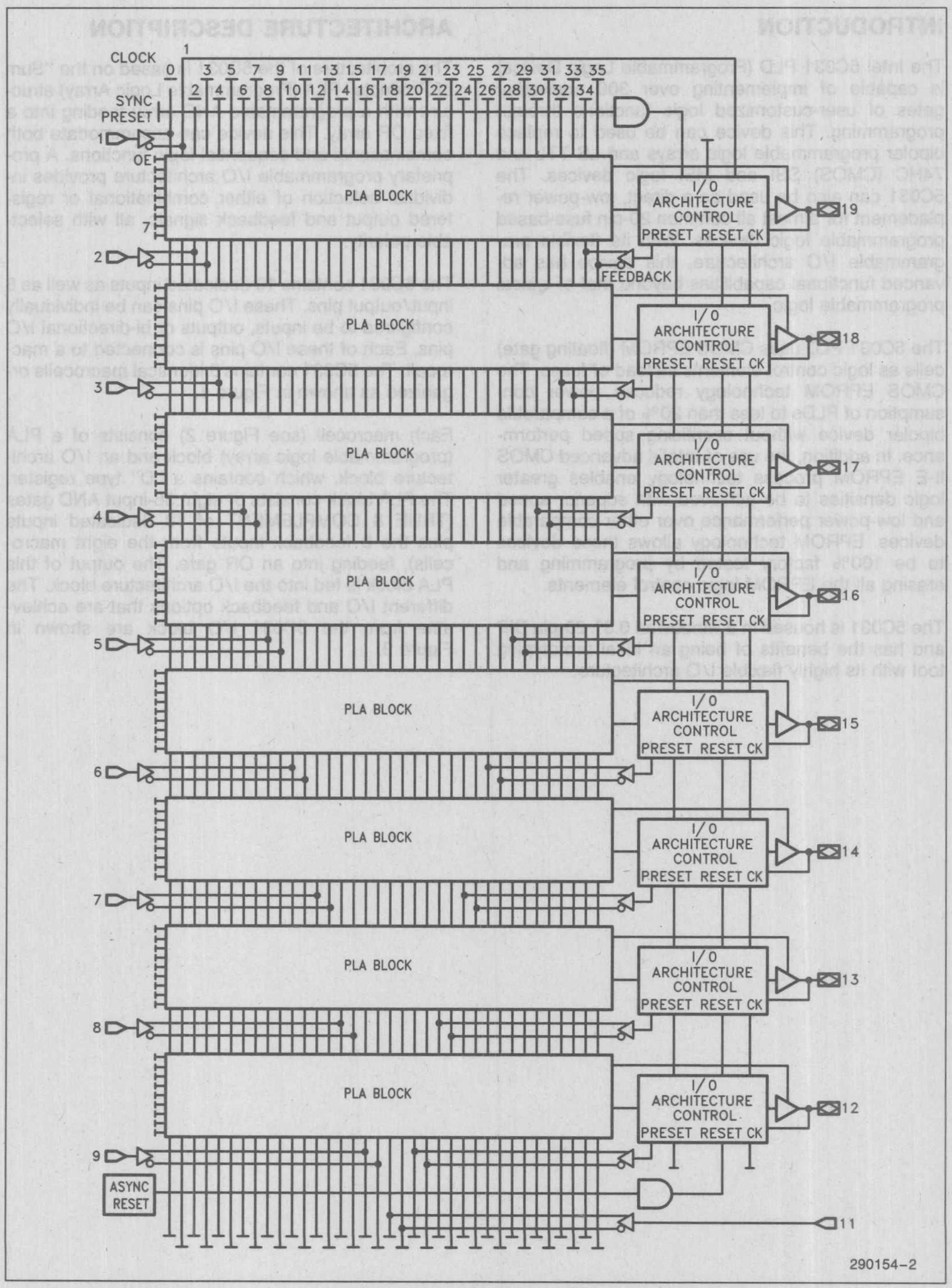


Figure 1. 5C031 Architecture

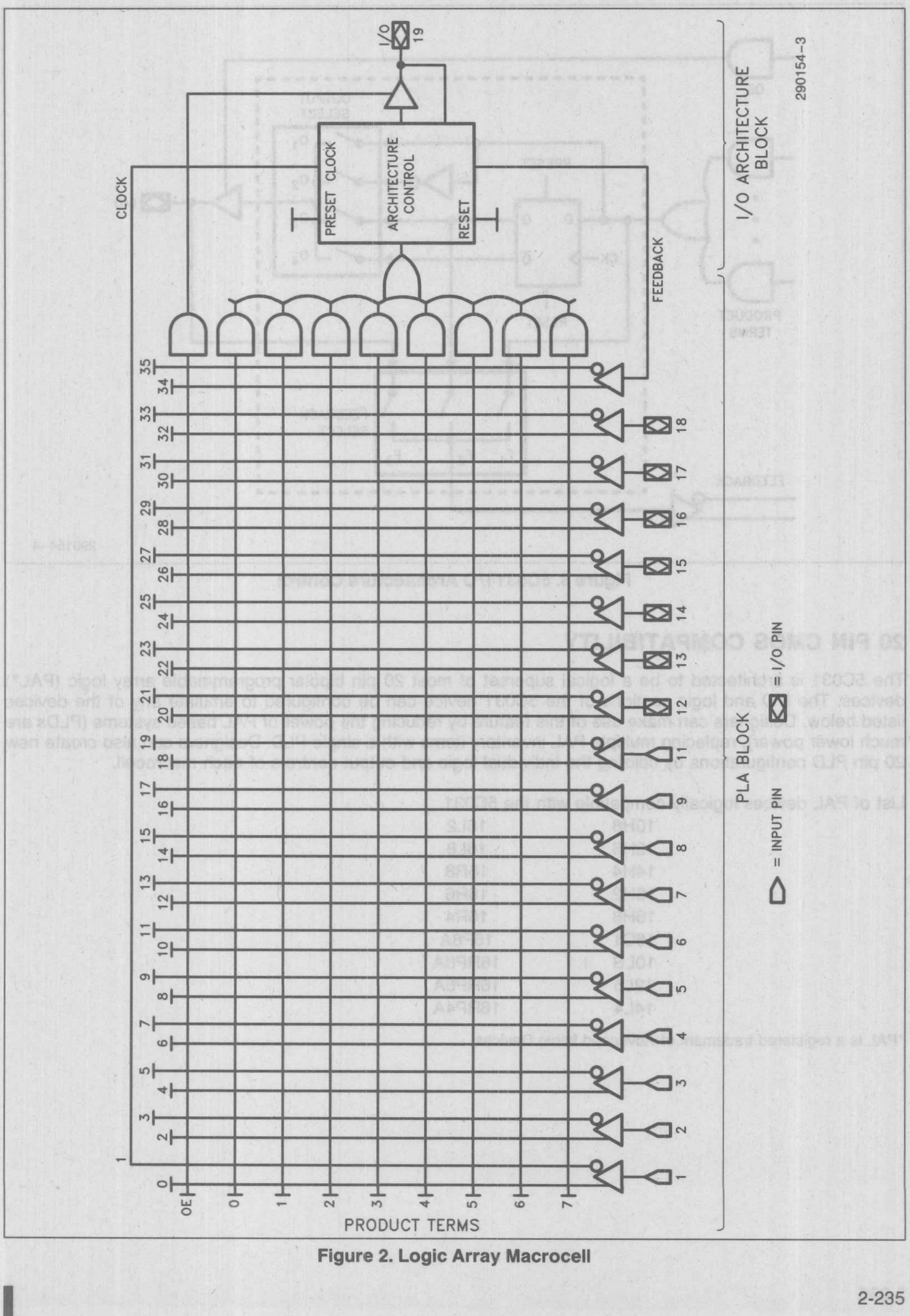


Figure 2. Logic Array Macrocell

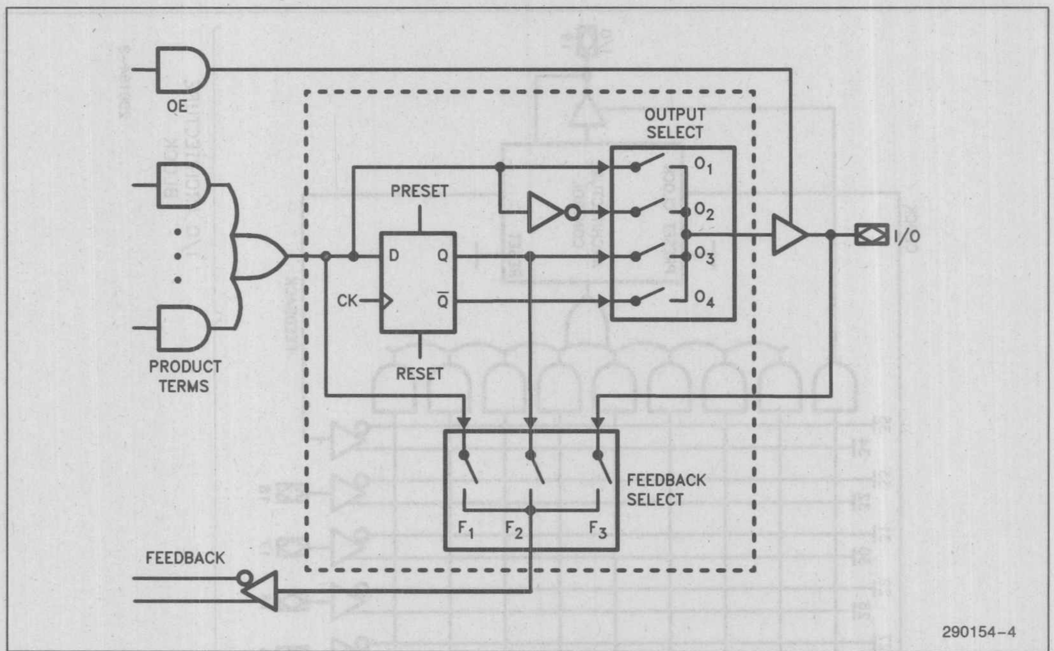


Figure 3. 5C031 I/O Architecture Control

20 PIN CMOS COMPATIBILITY

The 5C031 is architected to be a logical superset of most 20 pin bipolar programmable array logic (PAL*) devices. The I/O and logic sections of the 5C031 device can be configured to emulate any of the devices listed below. Designers can make use of this feature by reducing the power of PAL based systems (PLDs are much lower power), replacing multiple PAL inventory items with a single PLD. Designers can also create new 20 pin PLD configurations by utilizing the individual logic and output controls of each macrocell.

List of PAL devices logically compatible with the 5C031.

10H8	16L2
12H6	16L8
14H4	16R8
16H2	16R6
16H8	16R4
16C1	16P8A
10LB	16RP8A
12L6	16RP6A
14L4	16RP4A

*PAL is a registered trademark of Advanced Micro Devices.

Prior to programming or after erasing, the I/O structure is configured for combinatorial active low output with input (pin) feedback.

ERASURE CHARACTERISTICS

Erasure characteristics of the 5C031 are such that erasure begins to occur upon exposure to light with wavelengths shorter than approximately 4000Å. It should be noted that sunlight and certain types of flourescent lamps have wavelengths in the 3000–4000Å. Data shows that constant exposure to room level flourescent lighting could erase the typical 5C031 in approximately three years, while it would take approximately one week to cause erasure when exposed to direct sunlight. If the 5C031 is to be exposed to these types of lighting conditions for extended periods of time, conductive opaque labels should be placed over the device window to prevent unintentional erasure.

The recommended erasure procedure for the 5C031 is exposure to shortwave ultraviolet light with a wavelength of 2537Å. The integrated dose (i.e., UV intensity × exposure time) for erasure should be a minimum of fifteen (15) $Wsec/cm^2$. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 12,000 $\mu W/cm^2$ power rating. The 5C031 should be placed within one inch of the lamp tubes during erasure. The maximum integrated dose the 5C031 can be exposed to without damage is 7258 $Wsec/cm^2$ (1 week at 12,000 $\mu W/cm^2$). Exposure to high intensity UV light for longer periods may cause permanent damage to the device.

PROGRAMMING CHARACTERISTICS

Initially, and after erasure, all the EPROM control bits of the 5C031 are connected (in the "1" state). Each of the connected control bits are selectively disconnected by programming the EPROM cells into their "0" state. Programming voltage and waveform specifications are available by request from Intel to support programming of the 5C031.

Intelligent Programming Algorithm

The 5C031 supports the intelligent Programming Algorithm which rapidly programs Intel LPDs (and EPROMs) using an efficient and reliable method. This method greatly decreases the overall programming time while programming reliability is ensured as the incremental program margin of each bit is continually monitored to determine when the bit has been successfully programmed.

FUNCTIONAL TESTING

Since the logical operation of the 5C031 is controlled by EPROM elements, the device is completely testable. Each programmable EPROM bit controlling the internal logic is tested using application-independent test program patterns. After testing, the devices are erased before shipment to customers. No post-programming tests of the EPROM array are required.

The testability and reliability of EPROM-based programmable logic devices is an important feature over similar devices based on fuse technology. Fuse-based programmable logic devices require a user to perform post-programming tests to insure proper programming. These tests must be done at the device level because of the cummulative error effect. For example, a board containing ten devices each possessing a 2% device fallout translates into an 18% fallout at the board level (it should be noted that programming fallout of fuse-based programmable logic devices is typically 2% or higher).

DESIGN RECOMMENDATIONS

For proper operation, it is recommended that all input and output pins be constrained to the voltage range GND < (V_{IN} or V_{OUT}) < V_{CC}. Unused inputs should be tied to an appropriate logic level (e.g. either V_{CC} or GND) to minimize device power consumption. Reserved pins (as indicated in the iPLDS REPORT file) should be left floating (no connect) so that the pin can attain the appropriate logic level. A power supply decoupling capacitor of at least 0.2 μF must be connected directly between V_{CC} and GND pins of the device.

As with all CMOS devices, ESD handling procedures should be used with the 5C031 to prevent damage to the device during programming, assembly, and test.

DESIGN SECURITY

A single EPROM bit provides a programmable design security feature that controls the access to the data programmed into the device. If this bit is set, a proprietary design within the device cannot be copied. This EPROM security bit enables a higher degree of design security than fused-based devices since programmed data within EPROM cells is invisible even to microscopic evaluation. The EPROM security bit, along with all the other EPROM control bits, will be reset by erasing the device.

LATCH-UP IMMUNITY

All of the input, I/O, and clock pins of the 5C031 have been designed to resist latch-up which is inherent in inferior CMOS structures. The 5C031 is designed with Intel's proprietary CMOS II-E EPROM process. Thus, each of the 5C031 pins will not experience latch-up with currents up to 100 mA and voltages ranging from −1V to (V_{CC} + 1V). Furthermore, the programming pin is designed to resist latch-up to the 13.5V maximum device limit.

INTEL PROGRAMMABLE LOGIC SOFTWARE SUPPORT

Full logic compilation and functional simulation for the 5C031 is supported by PLDshell Plus software.

PLDshell Plus design software is Intel's new, user-friendly design tool for μPLD design. PLDshell Plus allows users to incorporate their preferred text editor, programming software, and additional design tools into a easy-to-use, menued design environment that includes Intel's PLDasm logic compiler and simulation software along with disassembly, conversion and translation utilities. The PLDasm compiler and simulator software accepts industry-standard PDS source files that express designs as Boolean equations, truth tables, or state machines. On-line help, datasheet briefs, technical notes, and error message information, along with waveform viewing/printing capability make the design task as easy as possible. PLDshell Plus software is available from Intel Literature channels or from your local Intel sales representative.

Tools that support schematic capture and timing simulation for the 5C031 are available. Please refer to the "Development Tools" section of the Programmable Logic handbook.

The 5C031 is also supported by third-party logic compilers such as ABEL*, CUPL*, PLDesigner*, Log/IC*, etc. Programming support is provided by third-party programmer companies such as Data I/O, Logical Devices, STAG, etc. Please refer to the "Third-Party Support" lists in the *Programmable Logic* handbook for complete information and vendor contacts.

ORDERING INFORMATION

t_{PD} (ns)	t_{CO} (ns)	f_{MAX} (MHz)	Order Code	Package	Operating Range
40	24	29.5	D5C031-40	CERDIP	Commercial
50	28	22.5	D5C031-50	CERDIP	Commercial

*ABEL is a trademark of Data I/O, Corporation. CUPL is a trademark of Logical Devices, Inc. PLDesigner is a trademark of MINC, Inc. Logic/IC is a trademark of ISDATA, Inc.

ABSOLUTE MAXIMUM RATINGS*

Symbol	Parameter	Min	Max	Units
V_{CC}	Supply Voltage(1)	−2.0	7.0	V
V_{PP}	Programming Supply Voltage(1)	−2.0	13.5	V
V_I	DC Input Voltage(1)(2)	−0.5	$V_{CC}+0.5$	V
t_{stg}	Storage Temperature	−65	+150	°C
t_{amb}	Ambient Temperature(3)	−10	+85	°C

NOTES:
1. Voltages with respect to ground.
2. Minimum DC input is −0.5V. During transitions, the inputs may undershoot to −2.0V or overshoot to 7.0V for periods less than 20 ns under no load conditions.
3. Under bias. Extended temperature versions are also available.

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage	4.75	5.25	V
V_{IN}	Input Voltage	0	V_{CC}	V
V_O	Output Voltage	0	V_{CC}	V
T_A	Operating Temperature	0	+70	°C
t_R	Input Rise Time		500	ns
t_F	Input Fall Time		500	ns

D.C. CHARACTERISTICS $T_A = 0°$ to $+70°C$, $V_{CC} = 5V \pm 5\%$

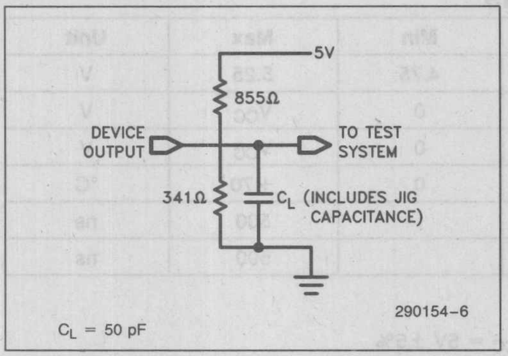
Symbol	Parameter/Test Conditions	Min	Typ	Max	Unit
V_{IH}(4)	High Level Input Voltage	2.0		$V_{CC} + 0.3$	V
V_{IL}(4)	Low Level Input Voltage	−0.3		0.8	V
V_{OH}(5)	High Level Output Voltage $I_O = -4.0$ mA D.C., V_{CC} = min.	2.4			V
V_{OL}	Low Level Output Voltage $I_O = 4.0$ mA D.C., V_{CC} = min.			0.45	V
I_I	Input Leakage Current V_{CC} = max., GND < V_{IN} < V_{CC}			±10	μA

D.C. CHARACTERISTICS $T_A = 0°$ to $+70°C$, $V_{CC} = 5V \pm 5\%$ (Continued)

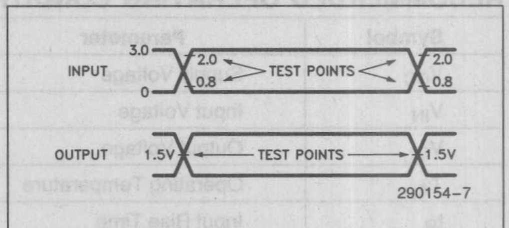
Symbol	Parameter/Test Conditions	Min	Typ	Max	Unit
I_{OZ}	Output Leakage Current V_{CC} = max., GND < V_{OUT} < V_{CC}			±10	μA
I_{SC}(6)	Output Short Circuit Current V_{CC} = max., V_{OUT} = 0.5V			10	mA
I_{CC}	Power Supply Current V_{CC} = max., V_{IN} = V_{CC} or GND No Load, Input Freq. = 1 MHz Device prog. as 8-bit Ctr.		15	40	mA

NOTES:
4. Absolute values with respect to device GND; all over and undershoots due to system or tester noise are included.
5. I_O at CMOS levels (3.84V) = −2 mA.
6. Not more than 1 output should be tested at a time. Duration of that test must not exceed 1 second.

A.C. TESTING LOAD CIRCUIT



A.C. TESTING INPUT, OUTPUT WAVEFORM



A.C. Testing: Inputs are Driven at 3.0V for a Logic "1" and 0V for a Logic "0". Timing Measurements are made at 2.0V for a Logic "1" and 0.8V for a Logic "0" on inputs. Outputs are measured at a 1.5V point. Device input rise and fall times < 6 ns.

CAPACITANCE

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V, f = 1.0 MHz			20	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V, f = 1.0 MHz			20	pF
C_{CLK}	Clock Pin Capacitance	V_{IN} = 0V, f = 1.0 MHz			20	pF
C_{VPP}	V_{PP} Pin	Pin 11			50	pF

A.C. CHARACTERISTICS $T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 5\%$, Turbo Bit Programmed(7)

Symbol	From	To	5C031-40 EP310-3			5C031-50 EP310			Unit
			Min	Typ	Max	Min	Typ	Max	
t_{PD}	I/O	Comb. Output			40			50	ns
t_{PZX}(8)	I or I/O	Output Enable			40			50	ns
t_{PXZ}(8)	I or I/O	Output Disable			40			50	ns
t_{CLR}	Asynch Reset	Q Reset			40			50	ns

NOTES:
7. Typical Values are at $T_A = 25°C$, $V_{CC} = 5V$, Active Mode
8. t_{PZX} and t_{PXZ} are measured at ±0.5V from steady state voltage as driven by spec. output load. t_{PXZ} is measured with $C_L = 5$ pF.

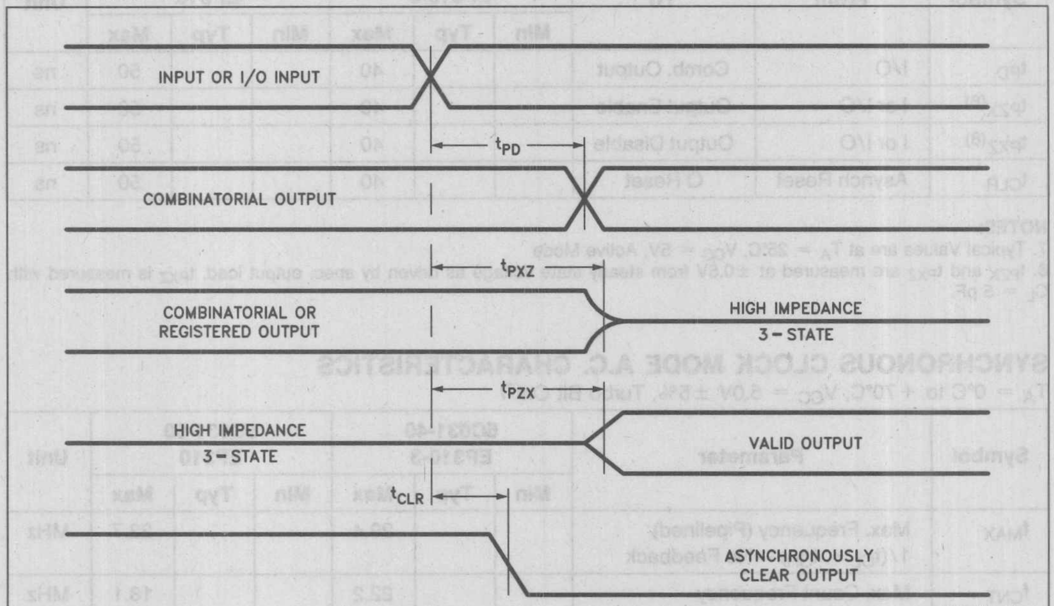
SYNCHRONOUS CLOCK MODE A.C. CHARACTERISTICS

$T_A = 0°C$ to $+70°C$, $V_{CC} = 5.0V \pm 5\%$, Turbo Bit On(7)

Symbol	Parameter	5C031-40 EP310-3			5C031-50 EP310			Unit
		Min	Typ	Max	Min	Typ	Max	
f_{MAX}	Max. Frequency (Pipelined) $1/(t_{CL} + t_{CH})$— No Feedback			29.4			22.7	MHz
f_{CNT}	Max. Count Frequency $1/t_{CNT}$ — With Internal Feedback			22.2			18.1	MHz
t_{SU}	I/O Setup Time to CLK	30			32			ns
t_H	I or I/O Hold after CLK High	0			0			ns
t_{CO}	CLK High to Output Valid			24			28	ns
t_{CNT}	Register Output Feedback to Register Input — Internal Path	45			55			ns
t_{CH}	CLK High Time	17			22			ns
t_{CL}	CLK Low Time	17			22			ns
t_{SET}	CLK High to Synch. Q Set			24			28	ns

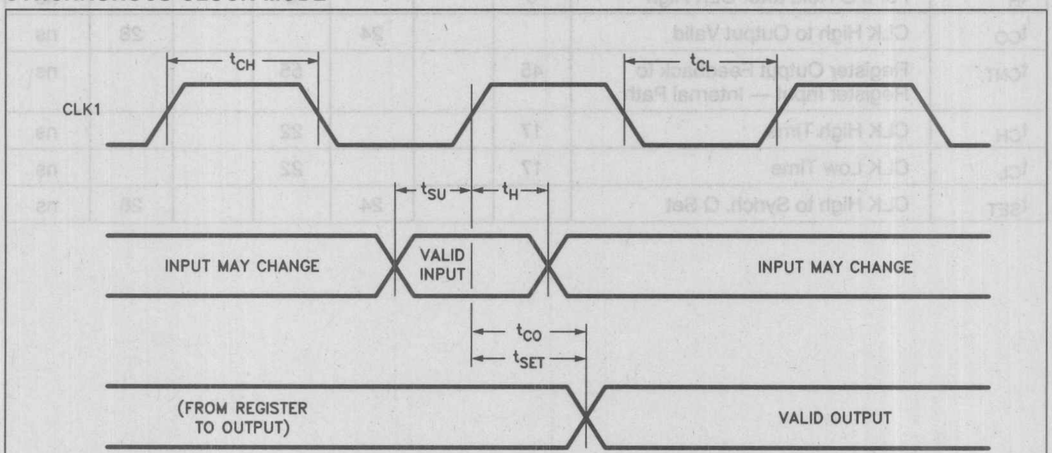
SWITCHING WAVEFORMS

COMBINATORIAL MODE



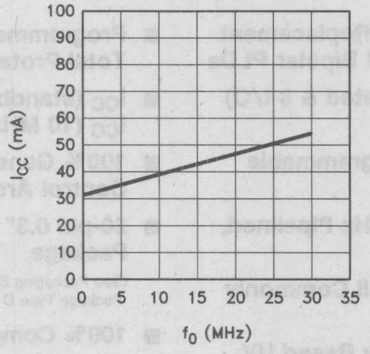
290154–8

SYNCHRONOUS CLOCK MODE



290154–9

5C031 Current in Relation to Frequency

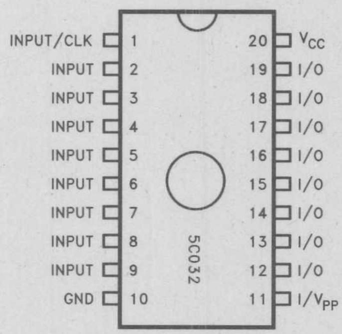


290154–10

Conditions: $T_A = 0°C$, $V_{CC} = 5.25V$

8-MACROCELL CMOS PLD

- High-Density, Low-Power Replacement for SSI & MSI Devices and Bipolar PLDs
- Up to 18 Inputs (10 Dedicated & 8 I/O) and 8 Outputs
- Eight Macrocells with Programmable I/O Architecture
- t_{PD} = 30 ns (max), 43.5 MHz Pipelined, 28.5 MHz with Feedback
- Low Power Upgrade for All Commonly Used 20-pin PLDs
- CMOS EPROM Technology Based UV Erasable (CerDIP)
- Programmable "Security Bit" Allows Total Protection of Proprietary Designs
- I_{CC} (standby) 100 μA (max)
  I_{CC} (10 MHz) 25 mA (max)
- 100% Generically Tested EPROM Logic Control Array
- 20-pin 0.3″ Ceramic and Plastic DIP Package
  (See Packaging Spec., Order #240800)
  Package Type D and P
- 100% Compatible with EP320



290155–1

Pin Configuration

INTRODUCTION

The Intel 5C032 is an 8-macrocell, 20-pin, general-purpose PLD (Programmable Logic Device).This device can be used to replace bipolar programmable logic arrays and LS TTL and 74HC (CMOS) SSI and MSI logic devices. The 5C032 can also be used as a direct, low-power replacement for almost all common 20-pin fuse-based programmable logic devices. With its flexible programmable I/O architecture, this device is a superset of common 20-pin PLDs.

The 5C032 PLD uses CMOS EPROM (floating gate) cells as logic control elements instead of fuses. The CMOS EPROM technology reduces power consumption of PLDs to less than 20% of a comparable bipolar device without sacrificing speed performance. In addition, the use of Intel's advanced CMOS II-E EPROM process technology enables greater logic densities to be achieved with superior speed and low-power performance over other comparable devices. Intel's 5C032 has the benefit of "zero" stand-by power not available on other programmable logic devices. EPROM technology allows these devices to be 100% factory tested by programming and erasing all the EPROM logic control elements.

The 5C032 with its superior speed and power performance and its plastic package is an ideal production vehicle for high-volume manufacturing. Most commonly used 20-pin bipolar PLDs can be easily replaced with this device allowing for tremendous power consumption savings without sacrificing speed of operation.

ARCHITECTURE DESCRIPTION

The architecture of the 5C032 is based on the "Sum of Products" PLA (Programmable Logic Array) structure with a programmable AND array feeding into a fixed OR array. This device can accommodate both combinational and sequential logic functions. A proprietary programmable I/O architecture provides individual selection of either combinational or registered output and feedback signals, all with selectable polarity.

The 5C032 contains 10 dedicated inputs as well as 8 input/output pins. These I/O pins can be individually configured to be inputs, outputs or bi-directional I/O pins. Each of these I/O pins is connected to a macrocell. The 5C032 contains 8 identical macrocells organized as shown in Figure 1.

Each macrocell (see Figure 2) consists of a PLA (programmable logic array) block and an I/O architecture block, which contains a "D" type register. The PLA block consists of eight 36-input AND gates (TRUE & COMPLEMENT of 10 dedicated inputs plus the 8 feedback inputs from the eight macrocells), feeding into an OR gate. The output of this PLA block is fed into the I/O architecture block. The different I/O and feedback options that are available in the 5C032 I/O block are shown in Figure 3.

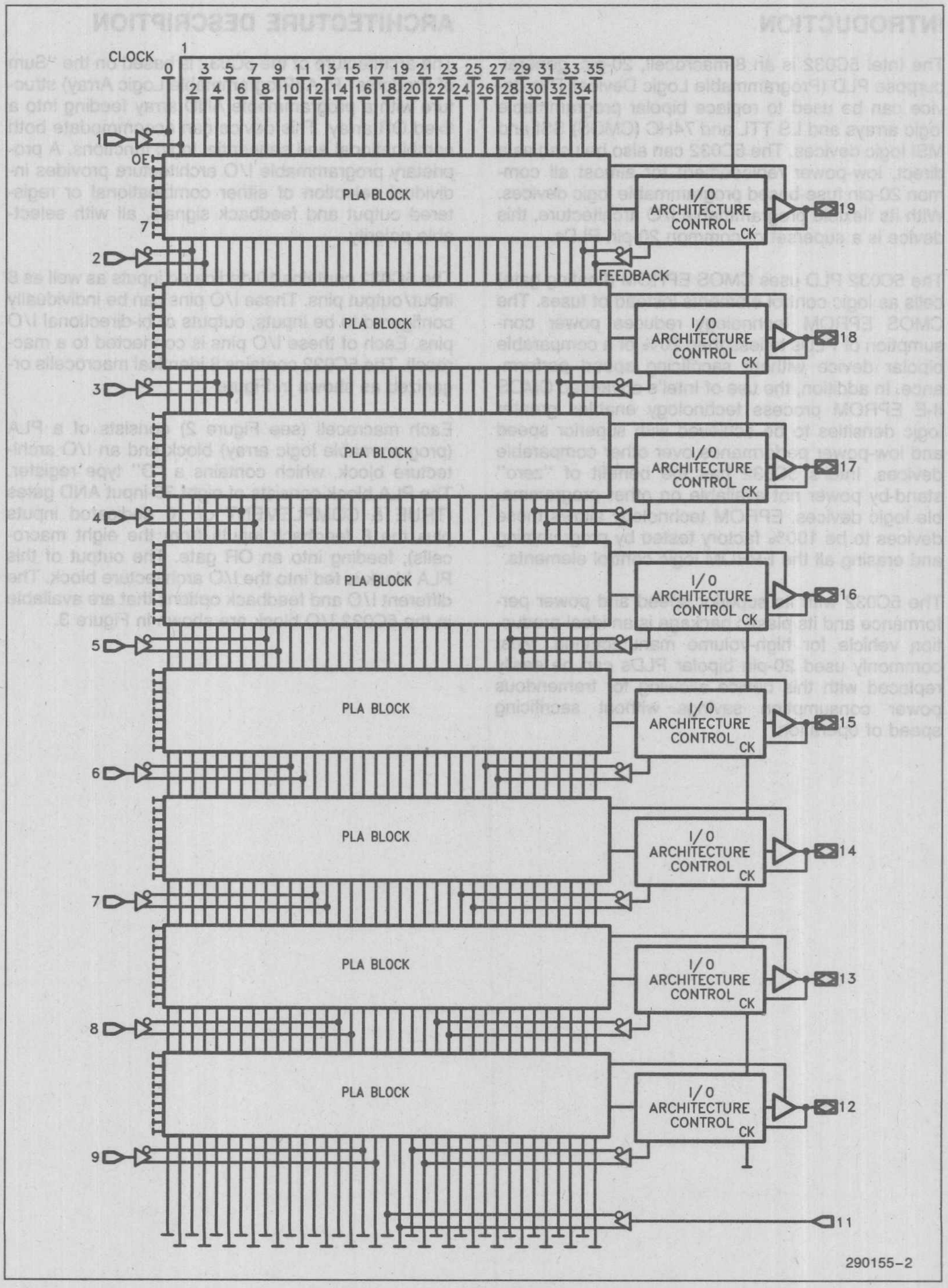


Figure 1. 5C032 Architecture

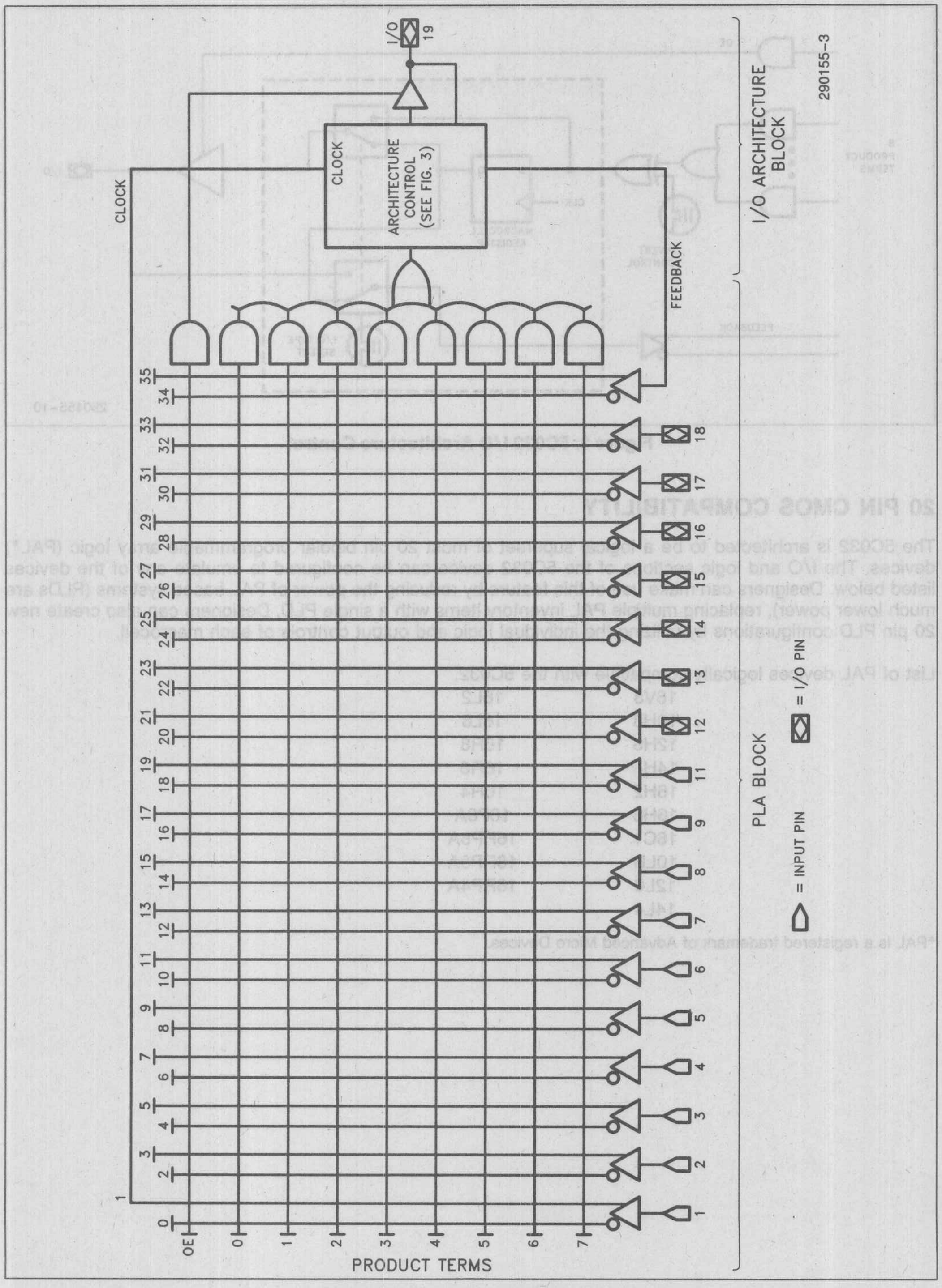


Figure 2. Logic Array Macrocell

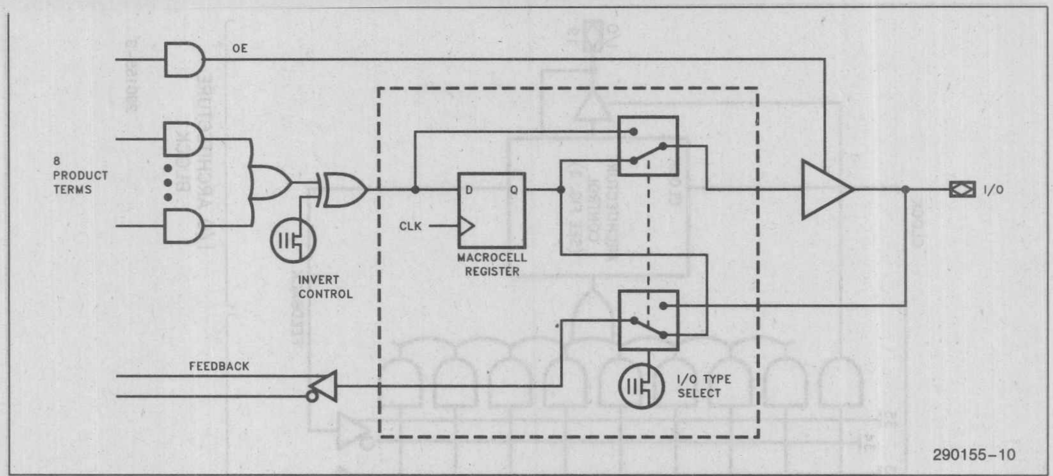


Figure 3. 5C032 I/O Architecture Control

20 PIN CMOS COMPATIBILITY

The 5C032 is architected to be a logical superset of most 20 pin bipolar programmable array logic (PAL*) devices. The I/O and logic sections of the 5C032 device can be configured to emulate any of the devices listed below. Designers can make use of this feature by reducing the power of PAL based systems (PLDs are much lower power), replacing multiple PAL inventory items with a single PLD. Designers can also create new 20 pin PLD configurations by utilizing the individual logic and output controls of each macrocell.

List of PAL devices logically compatible with the 5C032.

16V8	16L2
10H8	16L8
12H6	16R8
14H4	16R6
16H2	16R4
16H8	16P8A
16C1	16RP8A
10LB	16RP6A
12L6	16RP4A
14L4	

*PAL is a registered trademark of Advanced Micro Devices.

Erased-State Configuration

Prior to programming or after erasing, the I/O structure is configured for combinatorial active low output with input (pin) feedback.

ERASURE CHARACTERISTICS

Erasure characteristics of the 5C032 are such that erasure begins to occur upon exposure to light with wavelengths shorter than approximately 4000Å. It should be noted that sunlight and certain types of flourescent lamps have wavelengths in the 3000–4000Å. Data shows that constant exposure to room level flourescent lighting could erase the typical 5C032 in approximately three years, while it would take approximately one week to cause erasure when exposed to direct sunlight. If the 5C032 is to be exposed to these types of lighting conditions for extended periods of time, conductive opaque labels should be placed over the device window to prevent unintentional erasure.

The recommended erasure procedure for the 5C032 is exposure to shortwave ultraviolet light with a wavelength of 2537Å. The integrated dose (i.e., UV intensity × exposure time) for erasure should be a minimum of fifteen (15) Wsec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 12,000 μW/cm^2 power rating. The 5C032 should be placed within one inch of the lamp tubes during erasure. The maximum integrated dose the 5C032 can be exposed to without damage is 7258 Wsec/cm^2 (1 week at 12,000 μW/cm^2). Exposure to high intensity UV light for longer periods may cause permanent damage to the device.

PROGRAMMING CHARACTERISTICS

Initially, and after erasure, all the EPROM control bits of the 5C032 are connected (in the "1" state). Each of the connected control bits are selectively disconnected by programming the EPROM cells into their "0" state. Programming voltage and waveform specifications are available by request from Intel to support programming of the device.

Intelligent Programming Algorithm

The 5C032 supports the Intelligent Programming Algorithm which rapidly programs Intel H-ELPDs (and EPROMs) using an efficient and reliable method. The Intelligent Programming Algorithm is particularly suited to the production programming environment. This method greatly decreases the overall programming time while programming reliability is ensured as the incremental program margin of each bit is continually monitored to determine when the bit has been successfully programmed.

FUNCTIONAL TESTING

Since the logical operation of the 5C032 is controlled by EPROM elements, the device is completely testable. Each programmable EPROM bit controlling the internal logic is tested using application-independent test program patterns. After testing, the devices are erased before shipment to customers. No post-programming tests of the EPROM array are required.

The testability and reliability of EPROM-based programmable logic devices is an important feature over similar devices based on fuse technology. Fuse-based programmable logic devices require a user to perform post-programming tests to insure proper programming. These tests must be done at the device level because of the cummulative error effect. For example, a board containing ten devices each possessing a 2% device fallout translates into an 18% fallout at the board level (it should be noted that programming fallout of fuse-based programmable logic devices is typically 2% or higher).

DESIGN RECOMMENDATIONS

For proper operation, it is recommended that all input and output pins be constrained to the voltage range GND < (V_{IN} or V_{OUT}) < V_{CC}. Unused inputs should be tied to an appropriate logic level (e.g. either V_{CC} or GND) to minimize device power consumption. Reserved pins (as indicated in the iPLDS REPORT file) should be left floating (no connect) so that the pin can attain the appropriate logic level. A power supply decoupling capacitor of at least 0.2 μF must be connected directly between V_{CC} and GND pins of the device.

As with all CMOS devices, ESD handling procedures should be used with the 5C032 to prevent damage to the device during programming, assembly, and test.

DESIGN SECURITY

A single EPROM bit provides a programmable design security feature that controls the access to the data programmed into the device. If this bit is set, a proprietary design within the device cannot be copied. This EPROM security bit enables a higher degree of design security than fused-based devices since programmed data within EPROM cells is invisi-

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ble even to microscopic evaluation. The EPROM security bit, along with all the other EPROM control bits, will be reset by erasing the device.

AUTOMATIC STAND-BY MODE

The 5C032 contains a programmable bit, the Turbo Bit, that optimizes operation for speed or for power savings. When the Turbo Bit is programmed (TURBO = ON), the device is optimized for maximum speed. When the Turbo bit is not programmed (TURBO = OFF), the device is optimized for power savings by entering standby mode during periods of inactivity.

Figure 4 shows the device entering standby mode approximately 100 ns after the last input transition. When the next input transition is detected, the device returns to active mode. Wakeup time adds an additional 15 ns to the propagation delay through the device as measured from the first input. No delay will occur if an output is dependent on more than one input and the last of the inputs changes after the device has returned to active mode.

After erasure, the Turbo Bit is unprogrammed (OFF); automatic standby mode is enabled. When the Turbo Bit is programmed (ON), the device never enters standby mode.

LATCH-UP IMMUNITY

All of the input, I/O, and clock pins of the 5C032 have been designed to resist latch-up which is inherent in inferior CMOS structures. The 5C032 is designed with Intel's proprietary CMOS II-E EPROM process. Thus, each of the 5C032 pins will not experience latch-up with currents up to ± 100 mA and voltages ranging from $-1V$ to ($V_{CC} + 1V$). Furthermore, the programming pin is designed to resist latch-up to the 13.5V maximum device limit.

SOFTWARE SUPPORT

Full logic compilation and functional simulation for the 5C032 is supported by PLDshell Plus software.

PLDshell Plus design software is Intel's user-friendly design tool for μPLD design. PLDshell Plus allows users to incorporate their preferred text editor, programming software, and additional design tools into an easy-to-use, menued design environment that includes Intel's PLDasm logic compiler and simulation software along with disassembly, conversion, and translation utilities. The PLDasm compiler and simulator software accepts industry-standard PDS source files that express designs as Boolean equations, truth tables, or state machines. On-line help, datasheet briefs, technical notes, and error message information, along with waveform viewing/printing capability make the design task as easy as possible. PLDshell Plus software is available from Intel Literature channels or from your local Intel sales representative.

Tools that support schematic capture and timing simulation for the 5C032 are available. Please refer to the "Development Tools" section of the Programmable Logic handbook.

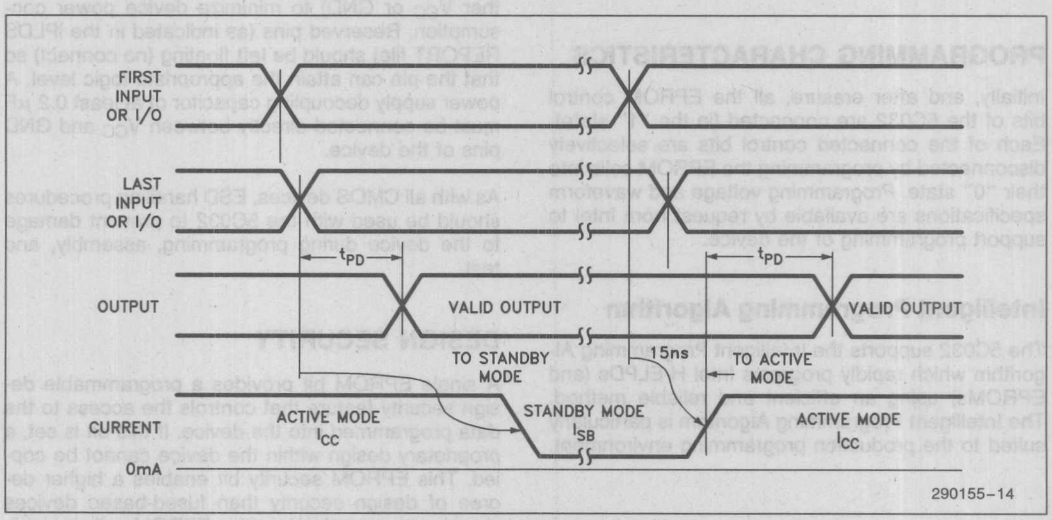

Figure 4. 5C032 Standby and Active Mode Transitions

The 5C032 is also supported by third-party compilers such as ABEL*, CUPL*, PLDesigner*, Log/IC, etc. Programming support is provided by third-party programmer companies such as Data I/O, Logical Devices, STAG, etc. Please refer to the "Third-Party Support" lists in the *Programmable Logic* handbook for complete information and vendor contacts.

ORDERING INFORMATION

t_{PD} (ns)	t_{CO} (ns)	f_{MAX} (MHz)	Order Code	Package	Operating Range
30	17	43.5	D5C032-30	CERDIP	Commercial
			P5C032-30	PDIP	
35	20	40	D5C032-35	CERDIP	Commercial
			P5C032-35	PDIP	
40	24	33.3	D5C032-40	CERDIP	Commercial
			P5C032-40	PDIP	
35	20	40	TP5C032-35	PDIP	Industrial

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*ABEL is a trademark of Data I/O, Corp. CUPL is a trademark of Logical Devices, Inc. PLDesigner is a trademark of MINC, Inc. Log/IC is a trademark of ISDATA, Incorporated.

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage(1)	−2.0	7.0	V
V_{PP}	Programming Supply Voltage(1)	−2.0	13.5	V
V_I	DC Input Voltage(1)(2)	−0.5	V_{CC} + 0.5	V
t_{stg}	Storage Temperature	−65	+150	°C
t_{amb}	Ambient Temperature(4)	−10	+85	°C

NOTES:
1. Voltages with respect to ground.
2. Minimum DC input is −0.5V. During transitions, the inputs may undershoot to −2.0V or overshoot to +7.0V for periods less than 20 ns under no load conditions.
3. Under bias, Extended temperature versions are also available.
4. Extended temperature versions also available.

cations are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

RECOMMENDED OPERATING CONDITIONS

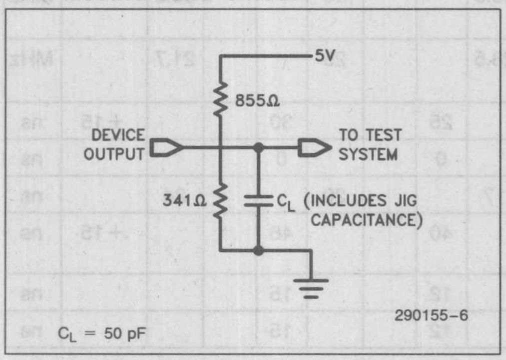
Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage	4.75	5.25	V
V_{IN}	Input Voltage	0	V_{CC}	V
V_O	Output Voltage	0	V_{CC}	V
T_A	Operating Temperature	0	+70	°C
t_R	Input Rise Time		500	ns
t_F	Input Fall Time		500	ns

D.C. CHARACTERISTICS $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$

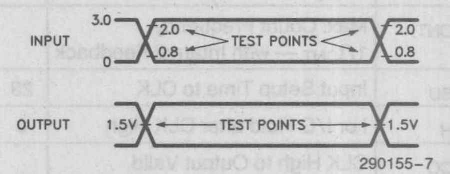
Symbol	Parameter/Test Conditions	Min	Typ	Max	Unit
V_{IH}(5)	High Level Input Voltage	2.0		$V_{CC} + 0.3$	V
V_{IL}(5)	Low Level Input Voltage	−0.3		0.8	V
V_{OH}(6)	High Level Output Voltage $I_O = -4.0$ mA D.C., V_{CC} = min.	2.4			V
V_{OL}	Low Level Output Voltage $I_O = 4.0$ mA D.C., V_{CC} = min.			0.45	V
I_I	Input Leakage Current V_{CC} = max., GND < V_{IN} < V_{CC}			±10	μA
I_{OZ}	Output Leakage Current V_{CC} = max., GND < V_{OUT} < V_{CC}			±10	μA
I_{SC}(7)	Output Short Circuit Current V_{CC} = max., V_{OUT} = 0.5V			10	mA
I_{SB}(8)	Standby Current V_{CC} = max., V_{IN} = V_{CC} or GND, Standby Mode		10	100	μA
I_{CC}(9)	Power Supply Current V_{CC} = max., V_{IN} = V_{CC} or GND, No Load, Input Freq. = 10 MHz Active Mode (Turbo = Off), Device Prog. as 8-bit Ctr.		15	25	mA

NOTES:
5. Absolute values with respect to device GND; all over- and undershoots due to system or tester noise are included.
6. I_O at CMOS levels (3.84V) = −2 mA.
7. Not more than 1 output should be tested at a time. Duration of that test must not exceed 1 second.
8. With Turbo Bit = Off, device automatically enters standby mode approximately 100 ns after last input transition.
9. Maximum Active Current at operational frequency is less than 40 mA.

A.C. TESTING LOAD CIRCUIT



A.C. TESTING INPUT, OUTPUT WAVEFORM



A.C. Testing: Inputs are Driven at 3.0V for a Logic "1" and 0V for a Logic "0". Timing Measurements are made at 2.0V for a Logic "1" and 0.8V for a Logic "0" on inputs. Outputs are measured at a 1.5V point. Device input rise and fall times < 6 ns.

CAPACITANCE

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V, f = 1.0 MHz			10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V, f = 1.0 MHz			10	pF
C_{CLK}	Clock Pin Capacitance	V_{IN} = 0V, f = 1.0 MHz			10	pF
C_{VPP}	V_{PP} Pin	Pin 11, f = 1.0 MHz			20	pF

A.C. CHARACTERISTICS T_A = 0°C to +70°C, V_{CC} = 5V ±5%, Turbo Bit On(10)

Symbol	From	To	5C032-30			5C032-35			5C032-40			Non-(8) Turbo Mode	Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
t_{PD}	I or I/O	Comb. Output			30			35			40	+15	ns
t_{PZX}(11)	I or I/O	Output Enable			30			35			40	+15	ns
t_{PXZ}(11)	I or I/O	Output Disable			30			35			40	+15	ns

NOTES:
10. Typ. values are at T_A = 25°C, V_{CC} = 5V, Active Mode.
11. t_{PZX} and t_{PXZ} are measured at ±0.5V from steady state voltage as driven by spec. output load. t_{PXZ} is measured with C_L = 5 pF.

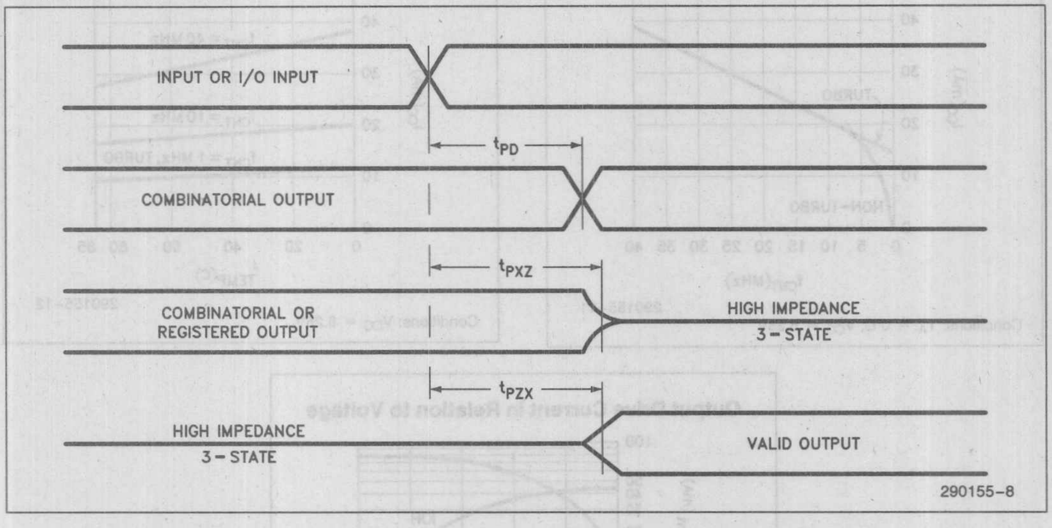
A.C. CHARACTERISTICS T_A = 0°C to 70°C, V_{CC} = 5V ±5%, Turbo Bit On (10)

SYNCHRONOUS CLOCK MODE

Symbol	Parameter	5C032-30 EP320-1			5C032-35 EP320-2			5C032-40			Non-(8) Turbo Mode	Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
f_{MAX}	Max. Frequency (Pipelined) $1/t_{SU}$ — No Feedback			43.5			40			33.3		MHz
f_{CNT}	Max. Count Frequency $1/t_{CNT}$ — with Internal Feedback			28.5			25			21.7		MHz
t_{SU}	Input Setup Time to CLK	23			25			30			+15	ns
t_H	I or I/O Hold after CLK High	0			0			0				ns
t_{CO}	CLK High to Output Valid			17			20			24		ns
t_{CNT}	Register Output Feedback to Register Input — Internal Path	35			40			46			+15	ns
t_{CH}	CLK High Time	11			12			15				ns
t_{CL}	CLK Low Time	11			12			15				ns

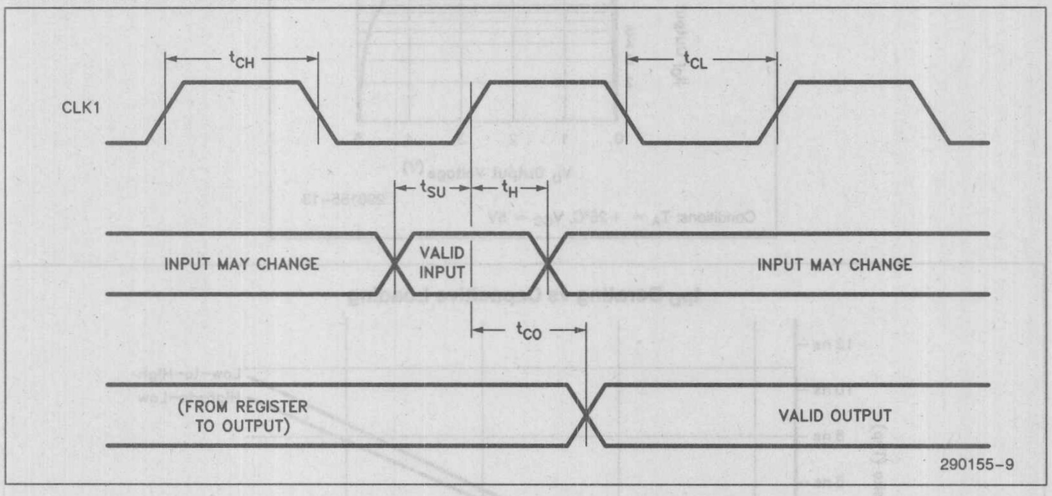
SWITCHING WAVEFORMS

COMBINATORIAL MODE



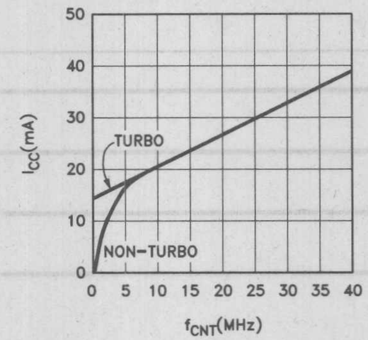
290155-8

SYNCHRONOUS CLOCK MODE



290155-9

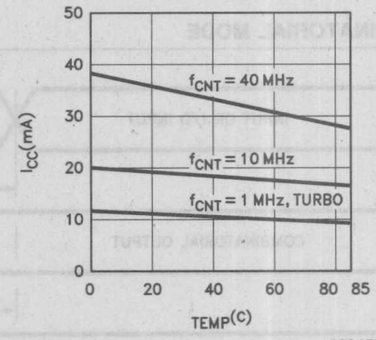
Current in Relation to Frequency



290155-11

Conditions: $T_A = 0°C$, $V_{CC} = 5.25V$

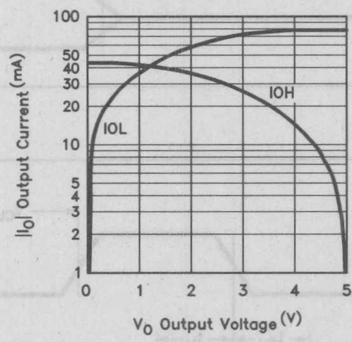
Current in Relation to Temperature



290155-12

Conditions: $V_{CC} = 5.25V$

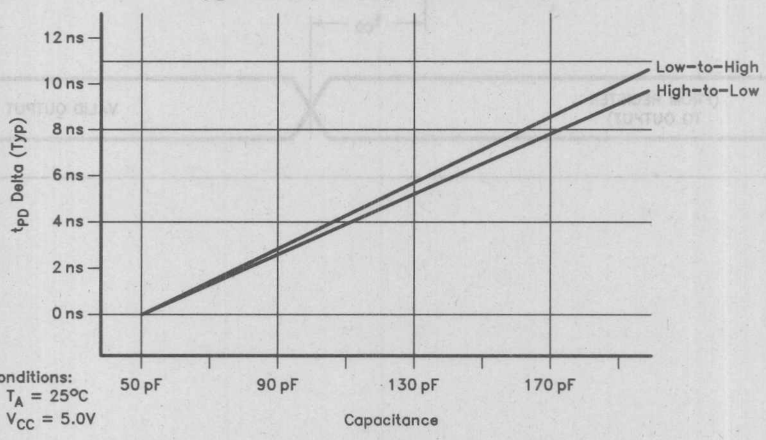
Output Drive Current in Relation to Voltage



290155-13

Conditions: $T_A = +25°C$, $V_{CC} = 5V$

t_{PD} Derating vs Capacitive Loading



Conditions:
$T_A = 25°C$
$V_{CC} = 5.0V$

290155-15

16-MACROCELL CMOS PLD

- High-Performance LSI Semi-Custom Logic Alternative to Low-End Gate Arrays, TTL, and 74HC SSI and MSI Logic
- 16 Macrocells with Programmable I/O Architecture; up to 20 Inputs (4 Dedicated, 16 I/O) or 16 Outputs
- Programmable Output Registers can be Configured as D, T, SR, or JK Types
- t_{PD} (max) 45 ns, 26.3 MHz Pipelined, 22.2 MHz w/Feedback
- Programmable Clock System with 2 Synchronous Clocks and Asynchronous Clocking Option on all Registers
- 8 P-Terms, Selectable SOP Invert, Clear and OE P-Terms for Each Macrocell
- Programmable Security Bit Allows Total Protection of Proprietary Designs
- CMOS EPROM Technology Based. UV Erasable (CerDIP) or OTP
- Progammable Low Power Option; 50 μA Typical Standby Current
- 100% Generically Tested Logic Array
- 100% Compatible with EP600
- Available in 24-Pin 300-mil CerDIP/PDIP and 28-Pin PLCC Packages

(See Packaging Specifications, Order Number 240800, Package Types D, P, and N)

2

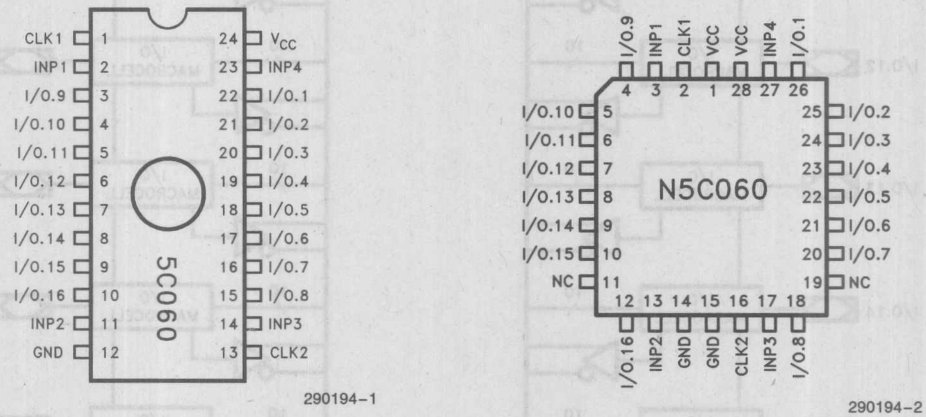


Figure 1. 5C060 Pin Configurations

The Intel 5C060 PLD (Programmable Logic Device) is a 16-macrocell, 24-pin, general purpose device. The device can be used to replace low-end gate arrays, multiple programmable logic arrays and LS TTL and 74HC (CMOS) SSI and MSI logic devices. The 5C060 can also be used as a direct, low-power replacement for most, common 24-pin fuse-based programmable logic devices. With its revolutionary programmable I/O architecture, the device has advanced functional capabilities beyond that of typical programmable logic. Figure 2 shows the global architecture of the device.

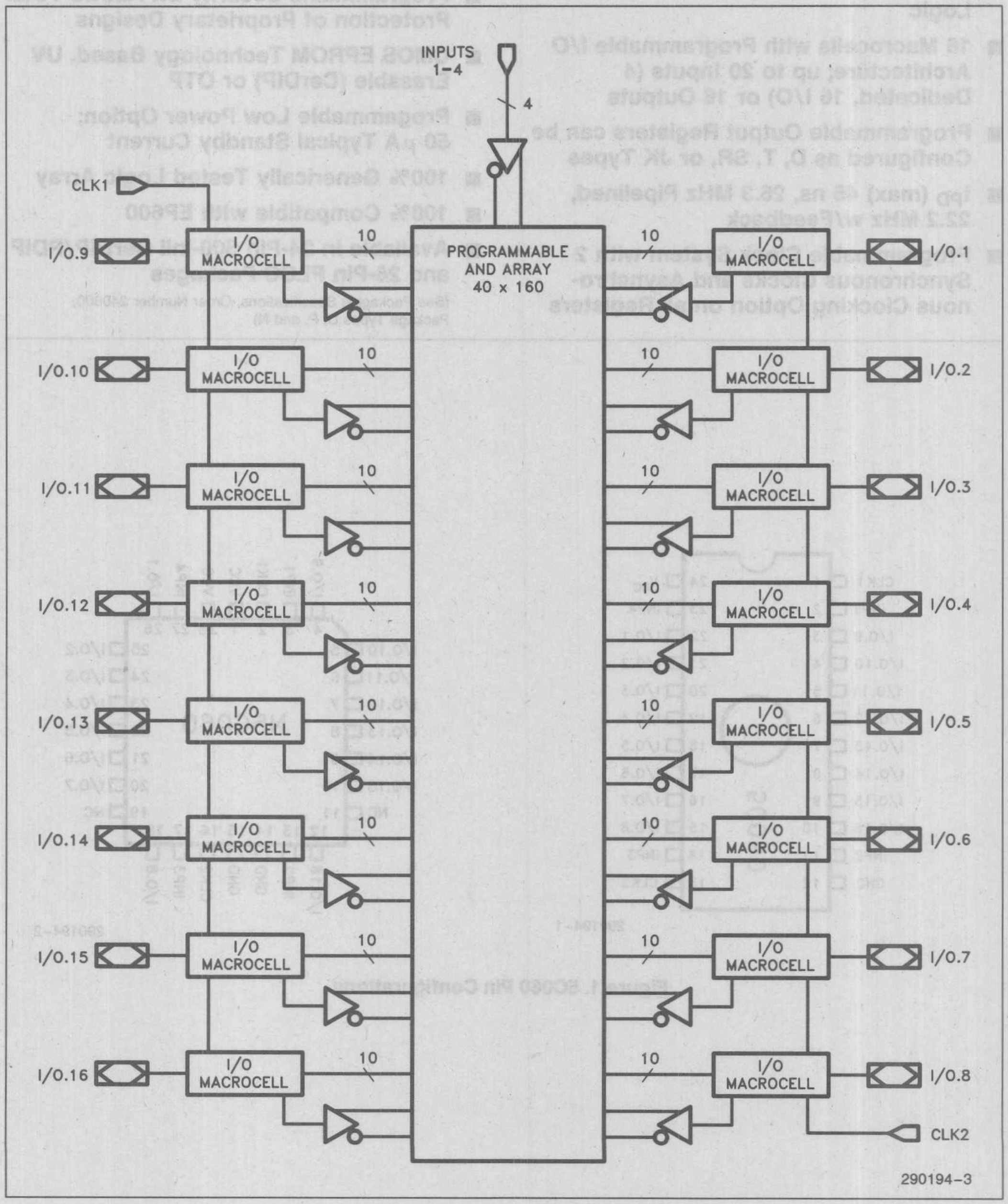


Figure 2. 5C060 Global Architecture

The 5C060 PLD uses CMOS EPROM (floating gate) cells as logic control elements instead of fuses. The CMOS EPROM technology reduces power consumption of PLDs to less than 20% of a comparable bipolar device without sacrificing speed performance. In addition, Intel's advanced CMOS II-E EPROM process technology enables greater logic densities to be achieved with superior speed and low-power performance over other comparable devices. Intel's ELPDs add the benefits of "zero" stand-by power not available on other programmable logic devices. EPROM technology allows these devices to be 100% factory tested by programming and erasing all the EPROM logic control elements.

The architecture of the 5C060 is based on the "Sum of Products" PLA (Programmable Logic Array) structure with a programmable AND array feeding into a fixed OR array. The device accommodates combinational and sequential logic functions. A proprietary programmable I/O architecture provides individual selection of either combinatorial or registered output and feedback signals all with selectable polarity.

A feature unique to the 5C060 is the ability to individually program the output registers as a D-, T-, SR-, or JK-type Flip-Flop without sacrificing the utilization of programmable AND logic. Additionally, each output register can be individually clocked from any of the input or feedback paths available within the AND array. With these features, a wide variety of logic functions can be simultaneously implemented—all on the same device.

ARCHITECTURE DESCRIPTION

Externally, the 5C060 has 4 dedicated data input pins, 16 I/O pins which may be configured for input, output, or bidirectional operations, and 2 synchronous clock inputs. The 5C060 is contained in a 24-pin windowed package (0.3 inch wide) or 28-lead J-leaded chip carrier package, and contains 16 programmable registers.

The basic Macrocell architecture for the 5C060 is shown in Figure 3. The 5C060 has 16 of these Macrocells (one for each I/O pin). The Macrocell is organized in the familiar sum-of-products structure with a programmable AND array attached to a fixed OR term. The inputs to the programmable AND array originate from the true and complement signals from each of the dedicated input pins and each of the I/O control blocks. The 40-input AND array of the 5C060 feeds 160 AND gates (product terms) which are distributed among the 16 available Macrocells within that device.

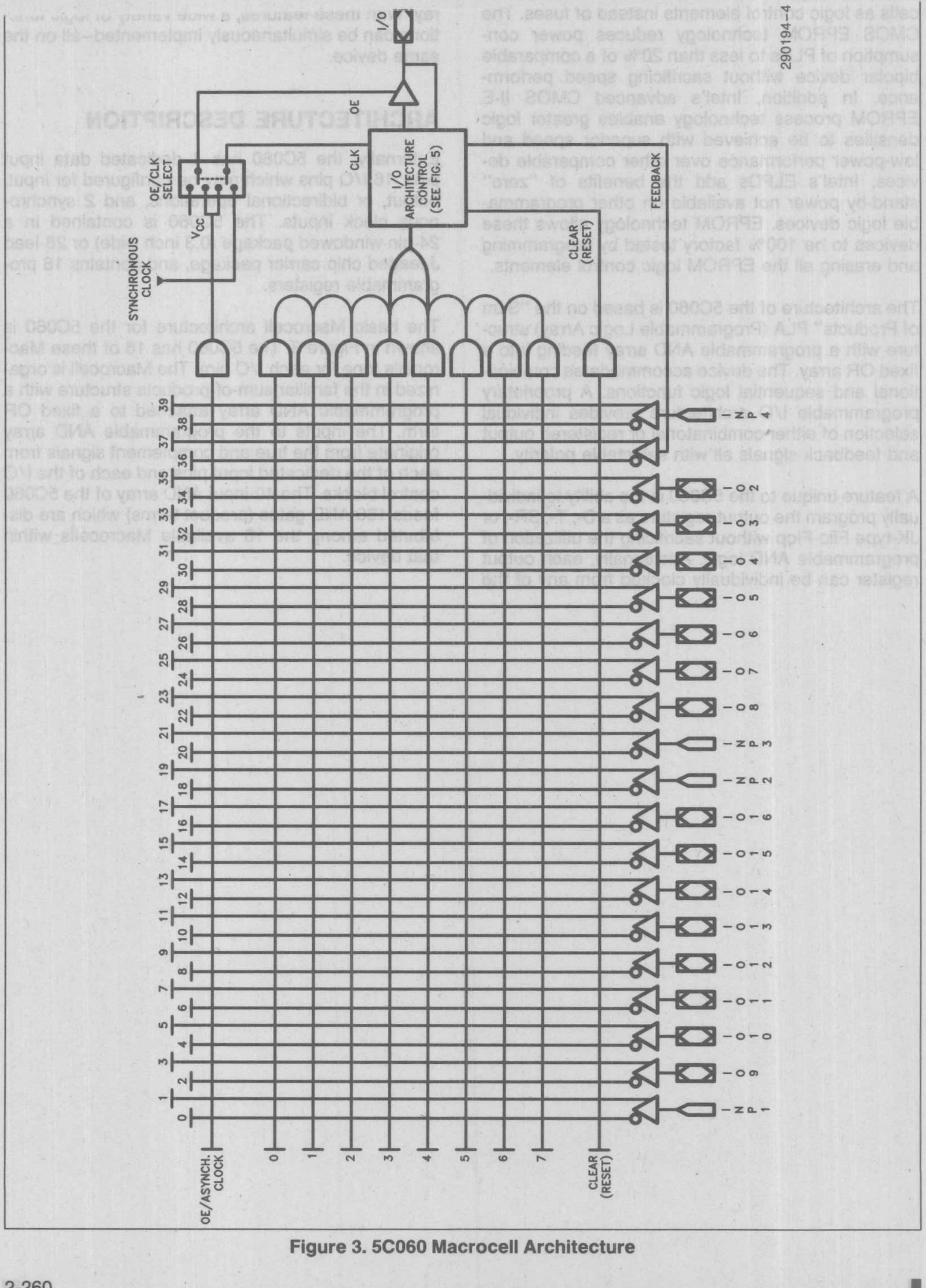


Figure 3. 5C060 Macrocell Architecture

Eight of the ten product terms (AND gates) are dedicated for logic implementation. One product term on each Macrocell is used for RESET control to the output register associated with the Macrocell. The final product term is used for OUTPUT ENABLE/ Asynchronous Clock implementation.

Within the AND array, there is an EPROM connection at every intersection of an input signal (true and complement) and a product term to a given Macrocell. Before programming an erased device, every EPROM connection is made at every intersection. But during the programming process, these connections are opened so that only the desired connections remain. Therefore, the true or complement of any input signal can be connected to any product term. If both the true and complement connections of any signal are left intact, a logical false results on the output of the AND gate. However, if both the true and complement connections are open, then a logic "don't care" results on the AND gate. Lastly, if all the inputs of a product term are programmed open, then a logical true results on the output of the AND gate.

The 5C060 has two dedicated clock inputs to provide synchronous clock signals to the internal registers. Each of the clock signals controls half the total registers within the given device. For example, CLK1 provides synchronous clocking to the registers in Macrocells in the left half of the array while CLK2 controls the registers associated with Macrocells in the right half of the array. The advanced I/O architecture allows for any number of the registers to be synchronously clocked (from none to all). Both of the dedicated clock inputs latch the data into a given register when triggered on a positive edge.

MACROCELL ARCHITECTURE SELECTION

The 5C060 architecture provides each Macrocell with over 50 different possible I/O register configurations. Each I/O pin can be configured for combinatorial or registered output (true or complement) with feedback. In addition, four different types of output registers can be implemented into every I/O pin without any additional logic requirements. The feedback mechanism for each register back into the AND array can be programmed to provide for either registered feedback from the Macrocell or input feedback (treating the pin as an input). Another advantage of the advanced I/O capability of the 5C060 is the ability to individually clock each internal register from asynchronous clock signals.

Output Enable (OE)/Clock Selection

Two modes of operation are provided by the OE/CLK Select Multiplexer as a part of each Macrocell. One mode provides for three-state buffering of outputs while in the other mode, the outputs are always enabled. The operation of the OE/CLK Select Multiplexer sets the mode within a given Macrocell. Therefore, the output mode can be selected individually on every output. Figure 4 illustrates the two modes of OE/CLK operation.

MODE 0: THREE-STATE BUFFERING

In Mode 0, the three-state output buffer is controlled by a single product term originating from the AND array. The output is enabled when the product term is a logical true. Conversely, the output appears as high impedance when the product term is a logical false as shown in Table 1. In Mode 0, the Macrocell Flip-Flop is connected to its associated synchronous clock (either CLK1 or CLK2 depending upon the Macrocell's location within the device). Thus, the Macrocell Flip-Flop may be clocked by its respective synchronous clock but its output will not become valid until the output is enabled.

Table 1. Mode 0 Output Selection

Product Term	Output Buffer
FALSE	Three-State
TRUE	Enabled

MODE 1: OUTPUT BUFFER ENABLED

In Mode 1, the Output Buffer is always enabled. In addition, the Macrocell Flip-Flop is connected to the AND array. The Macrocell Flip-Flop may now be triggered from an asynchronous clock signal generated by the AND array logic to the OE/CLK multiplexable term. Mode 1 allows the Macrocell Flip-Flops to be individually clocked from any of the available signals in the AND array. Since both true and complement values appear in the AND array, the Flip-Flop may be clocked by any positive- or negative-going signals at any input pin. Gated clock structures can be created since the Flip-Flop clock is created by a product term.

Invert Select EPROM Bit

The Invert Select EPROM bit is used to invert the product term input into the register. This applies to all inputs including double inputs on the JK and SR registers.

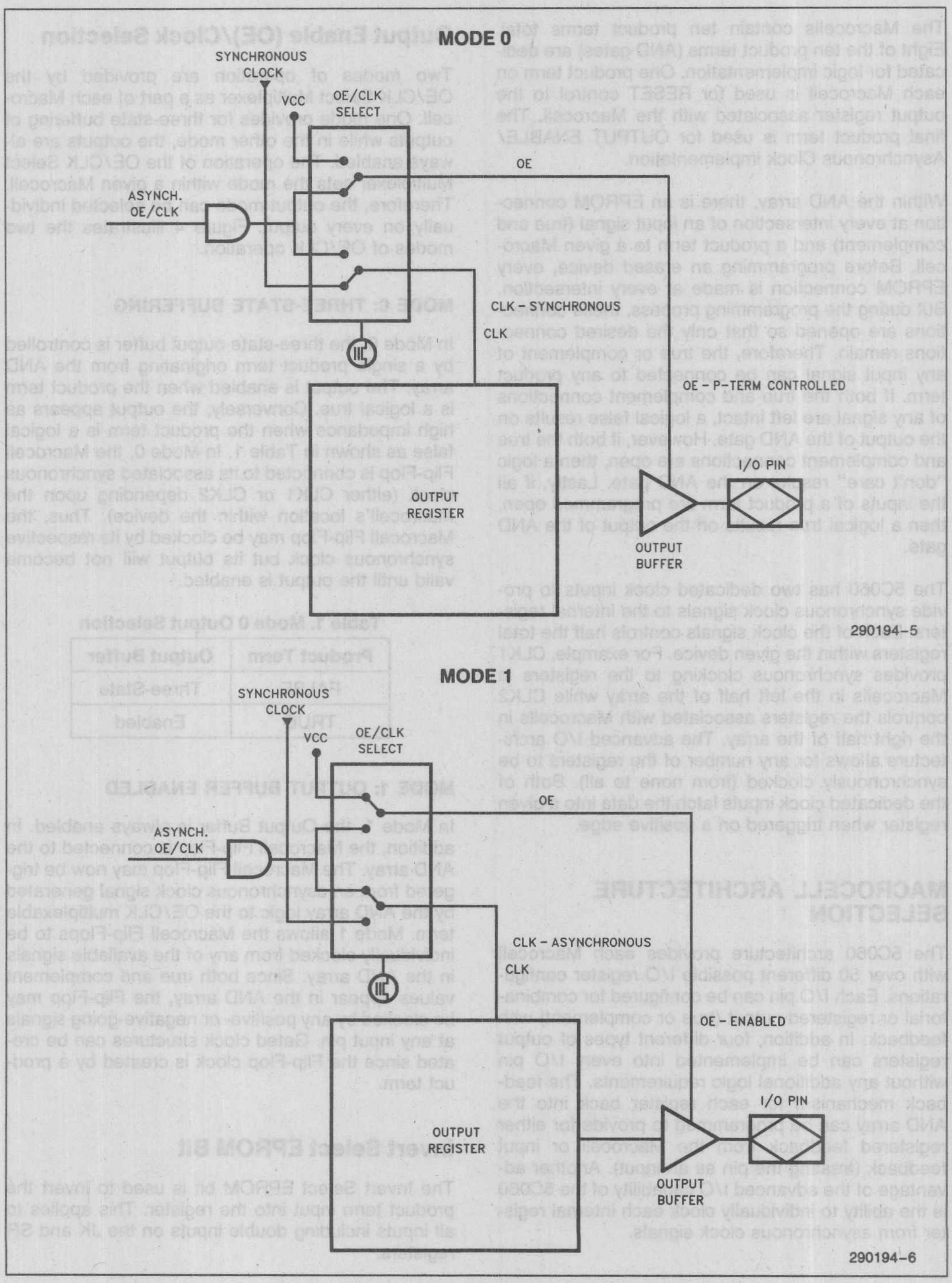


Figure 4. Output Enable/Clock Configuration

REGISTER SELECTION

The advanced I/O architecture of the 5C060 allows four different register types along with combinatorial output as illustrated in Figure 5a. The register types include a T, D, JK, or SR Flip-Flop and each Macrocell I/O structure may be independently configured. In addition, all registers have an individual asynchronous RESET control from a dedicated product term derived in the AND array. When this dedicated product term is a logical one, the Macrocell register is immediately cleared to a logical zero independent of the register clock. The RESET function occurs automatically on power-up.

Output Register Configuration

The four different register types shown in Figure 5b–5e are described below.

D- or T-type Flip-Flops

When either a D- or T-type Flip-Flop is configured as part of the I/O structure, all eight of the product terms into the Macrocell are ORed together and fed into the register input.

JK or SR Registers

When either a JK or SR register is configured, the eight product terms are shared among two OR gates (one for the J or S input and the other for the K or R input). The allocation for these product terms for each of the register inputs is optimized by the PLDshell Plus software.

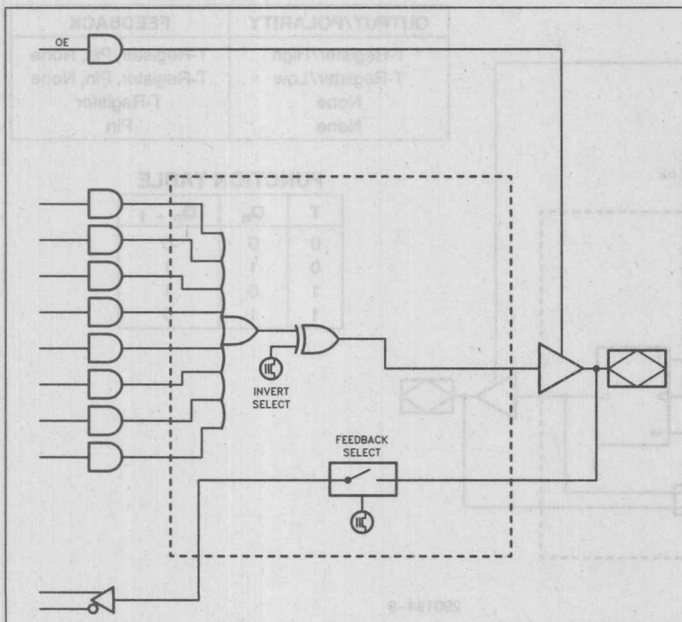
OUTPUT/FEEDBACK

The Output Select Multiplexer allows for either registered, combinatorial or no output.

The Feedback Select Multiplexer EPROM bit enables registered, I/O (using the pin for bidirectional input or just input), or no feedback to the AND array.

The Feedback Select is also important for building product terms with more than 8 products. The 8-product product term of a Macrocell can be fed back into the AND array and combined with still more signals to create a much larger product term (of more than 8-inputs). In addition, if the feedback product term is not to be output, then the PLDshell Plus software will reserve the associated Macrocell pin and indicate it in the REPORT file. A reserved pin should be left floating (no connect) when assembled onto a circuit board.

Any I/O pin may be configured as a dedicated input by selecting no output and pin feedback through the appropriate multiplexers.

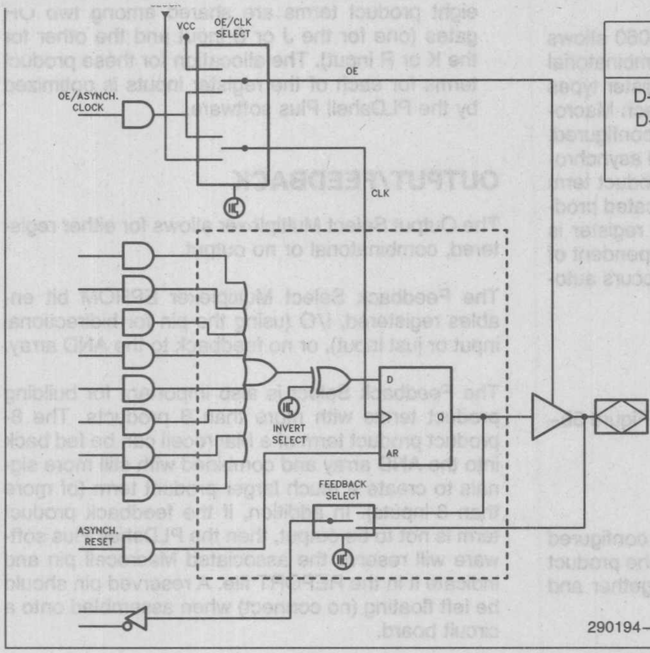


I/O SELECTION

OUTPUT/POLARITY	FEEDBACK
Combinatorial/High	Pin, None
Combinatorial/Low	Pin, None
None	Pin

290194–7

Figure 5a. Combinatorial I/O Configuration



I/O SELECTION

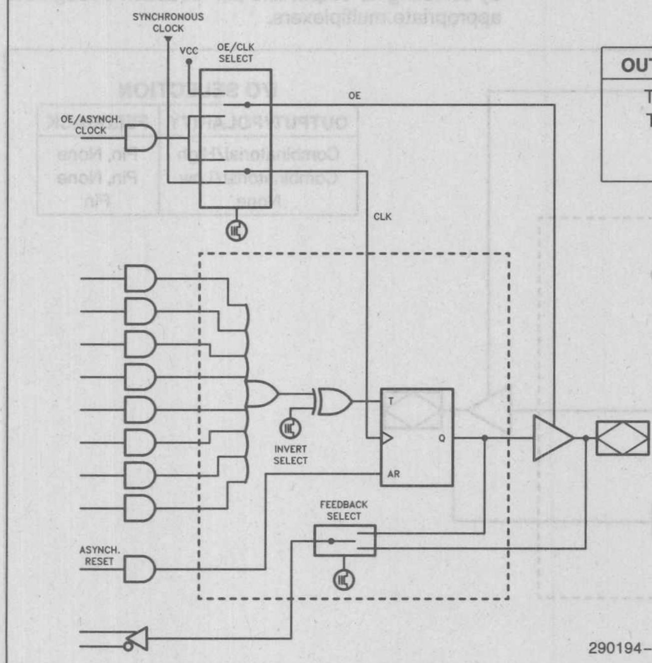
OUTPUT/POLARITY	FEEDBACK
D-Register/High	D-Register, Pin, None
D-Register/Low	D-Register, Pin, None
None	D-Registered
None	Pin

FUNCTION TABLE

D	Q_n	Q_{n+1}
0	0	0
0	1	0
1	0	1
1	1	1

290194-8

Figure 5b. D-Type (T-type) Flip-Flop Register Configuration



I/O SELECTION

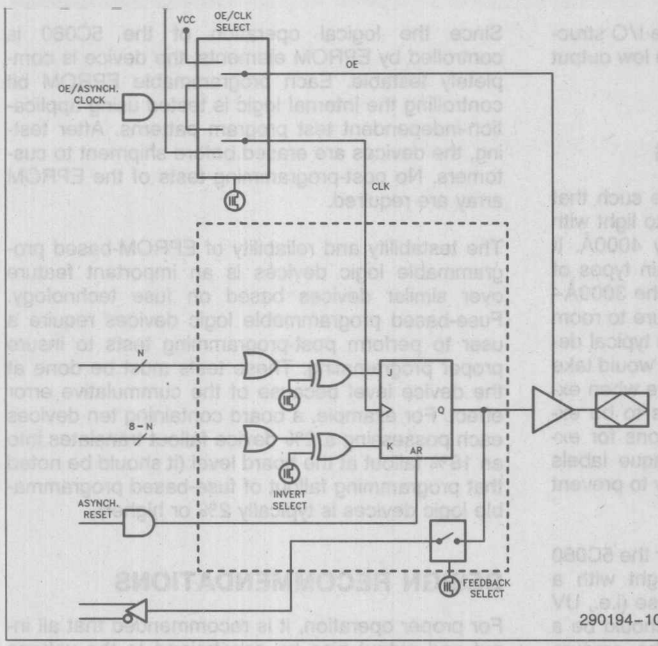
OUTPUT/POLARITY	FEEDBACK
T-Register/High	T-Register, Pin, None
T-Register/Low	T-Register, Pin, None
None	T-Register
None	Pin

FUNCTION TABLE

T	Q_n	Q_{n+1}
0	0	0
0	1	1
1	0	1
1	1	0

290194-9

Figure 5c. Toggle T-Type Flip-Flop Register Configuration

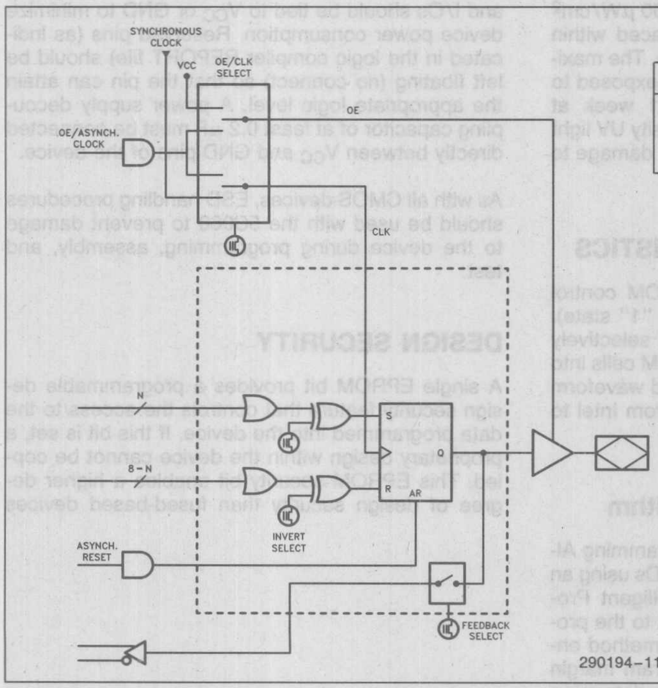


OUTPUT/POLARITY	FEEDBACK
JK Register/High	JK Register, None
JK Register/Low	JK Register, None
None	JK Register

FUNCTION TABLE

J	K	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Figure 5d. JK Flip-Flop Register Configuration



I/O SELECTION

OUTPUT/POLARITY	FEEDBACK
SR Register/High	SR Register, None
SR Register/Low	SR Register, None
None	SR Register

FUNCTION TABLE

S	R	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	Illegal	

Figure 5e. SR Flip-Flop Register Configuration

Erased-State Configuration

Prior to programming or after erasing, the I/O structure is configured for combinatorial active low output with input (pin) feedback.

ERASURE CHARACTERISTICS

Erasure characteristics of the device are such that erasure begins to occur upon exposure to light with wavelengths shorter than approximately 4000Å. It should be noted that sunlight and certain types of flourescent lamps have wavelengths in the 3000Å–4000Å. Data shows that constant exposure to room level flourescent lighting could erase the typical device in approximately three years, while it would take approximately one week to cause erasure when exposed to direct sunlight. If the 5C060 is to be exposed to these types of lighting conditions for extended periods of time, conductive opaque labels should be placed over the device window to prevent unintentional erasure.

The recommended erasure procedure for the 5C060 is exposure to shortwave ultraviolet light with a wavelength of 2537Å. The integrated dose (i.e., UV intensity × exposure time) for erasure should be a minimum of fifteen (15) Wsec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 12,000 μW/cm^2 power rating. The 5C060 should be placed within one inch of the lamp tubes during erasure. The maximum integrated dose the 5C060 can be exposed to without damage is 7258 Wsec/cm^2 (1 week at 12,000 μW/cm^2). Exposure to high intensity UV light for longer periods may cause permanent damage to the device.

PROGRAMMING CHARACTERISTICS

Initially, and after erasure, all the EPROM control bits of the 5C060 are connected (in the "1" state). Each of the connected control bits are selectively disconnected by programming the EPROM cells into their "0" state. Programming voltage and waveform specifications are available by request from Intel to support programming of the 5C060.

Intelligent Programming Algorithm

The 5C060 supports the Intelligent Programming Algorithm which rapidly programs Intel ELPDs using an efficient and reliable method. The Intelligent Programming Algorithm is particularly suited to the production programming environment. This method ensures reliability as the incremental program margin of each bit is continually monitored to determine when the bit has been successfully programmed.

FUNCTIONAL TESTING

Since the logical operation of the 5C060 is controlled by EPROM elements, the device is completely testable. Each programmable EPROM bit controlling the internal logic is tested using application-independent test program patterns. After testing, the devices are erased before shipment to customers. No post-programming tests of the EPROM array are required.

The testability and reliability of EPROM-based programmable logic devices is an important feature over similar devices based on fuse technology. Fuse-based programmable logic devices require a user to perform post-programming tests to insure proper programming. These tests must be done at the device level because of the cummulative error effect. For example, a board containing ten devices each possessing a 2% device fallout translates into an 18% fallout at the board level (it should be noted that programming fallout of fuse-based programmable logic devices is typically 2% or higher).

DESIGN RECOMMENDATIONS

For proper operation, it is recommended that all input and output pins be constrained to the voltage range GND < (V_{IN} or V_{OUT}) < V_{CC}. Unused inputs and I/Os should be tied to V_{CC} or GND to minimize device power consumption. Reserved pins (as indicated in the logic compiler REPORT file) should be left floating (no connect) so that the pin can attain the appropriate logic level. A power supply decoupling capacitor of at least 0.2 μF must be connected directly between V_{CC} and GND pins of the device.

As with all CMOS devices, ESD handling procedures should be used with the 5C060 to prevent damage to the device during programming, assembly, and test.

DESIGN SECURITY

A single EPROM bit provides a programmable design security feature that controls the access to the data programmed into the device. If this bit is set, a proprietary design within the device cannot be copied. This EPROM security bit enables a higher degree of design security than fused-based devices

since programmed data within EPROM cells is invisible even to microscopic evaluation. The EPROM security bit, along with all the other EPROM control bits, will be reset by erasing the device.

AUTOMATIC STAND-BY MODE

The 5C060 contains a programmable bit, the Turbo Bit, that optimizes operation for speed or for power savings. When the Turbo Bit is programmed (TURBO = ON), the device is optimized for maximum speed. When the Turbo Bit is not programmed (TURBO = OFF), the device is optimized for power savings by entering standby mode during periods of inactivity.

Figure 6 shows the device entering standby mode approximately 100 ns after the last input transition. When the next input transition is detected, the device returns to active mode. Wakeup time adds an additional 25 ns to the propagation delay through the device as measured from the first input. No delay will occur if an output is dependent on more than one input and the last of the inputs changes after the device has returned to active mode.

After erasure, the Turbo Bit is unprogrammed (OFF); automatic standby mode is enabled. When the Turbo Bit is programmed (ON), the device never enters standby mode.

LATCH-UP IMMUNITY

All of the input, I/O, and clock pins of the 5C060 have been designed to resist latch-up which is inherent in inferior CMOS structures. The 5C060 is designed with Intel's proprietary CMOS II-E EPROM process. Thus, each of the pins will not experience latch-up with currents up to ±100 mA and voltages ranging from −1V to (V_{CC} + 1V). Furthermore, the programming pin is designed to resist latch-up to the 13.5V maximum device limit.

SOFTWARE SUPPORT

Full logic compilation and functional simulation for the 5C060 is supported by PLDshell Plus software.

PLDshell Plus design software is Intel's user-friendly design tool for μPLD design. PLDshell Plus allows users to incorporate their preferred text editor, programming software, and additional design tools into an easy-to-use, menued design environment that includes Intel's PLDasm logic compiler and simulation software along with disassembly, conversion, and translation utilities. The PLDasm compiler and simulator software accepts industry-standard PDS source files that express designs as Boolean equations, truth tables, or state machines. On-line help, data sheet briefs, technical notes, and error message information, along with waveform viewing/printing capability make the design task as easy as possible. PLDshell Plus software is available from Intel Literature channels or from your local Intel sales representative.

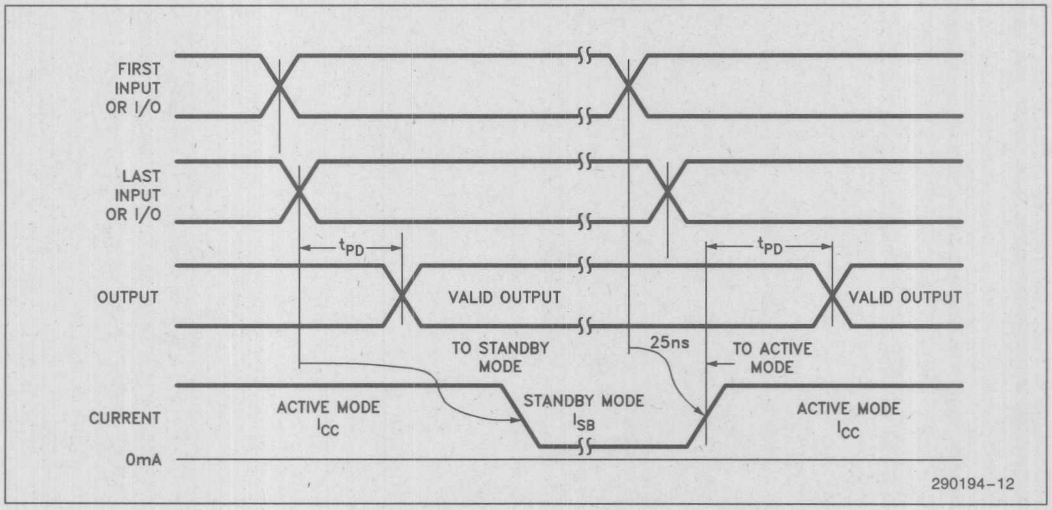


Figure 6. 5C060 Standby and Active Mode Transitions

Tools that support schematic capture and timing simulation for the 5C060 are available. Please refer to the "Development Tools" section of the Programmable Logic Handbook.

The 5C060 is also supported by third-party logic compilers such as ABEL*, CUPL*, PLDesigner*, Log/IC*, etc. Programming support is provided by third-party programmer companies such as Data I/O, Logical Devices, STAG, etc. Please refer to the "Third-Party Support" lists in the *Programmable Logic* handbook for complete information and vendor contacts.

ORDERING INFORMATION

t_{PD} (ns)	t_{CO} (ns)	f_{MAX} (MHz)	Order Code	Package	Operating Range
45	22	26	D5C060-45	CERDIP	Commercial
			P5C060-45	PDIP	
			N5C060-45	PLCC	
55	25	23	D5C060-55	CERDIP	Commercial
			P5C060-55	PDIP	
			N5C060-55	PLCC	
45	22	26	TD5C060-45	CERDIP	Industrial
45	22	26	TN5C060-45	PLCC	Industrial

*Abel is a trademark of Data I/O, Corp. CUPL is a trademark of Logical Devices, Inc. PLDesigner is a trademark of MINC, Inc. Log/IC is a trademark of ISDATA, Inc.

ABSOLUTE MAXIMUM RATINGS*

Symbol	Parameter	Min	Max	Units
V_{CC}	Supply Voltage(1)	−2.0	7.0	V
V_{PP}	Programming Supply Voltage(1)	−2.0	13.5	V
V_I	DC Input Voltage(1)(2)	−0.5	$V_{CC}+0.5$	V
t_{stg}	Storage Temperature	−65	+150	°C
t_{amb}	Ambient Temperature(3)	−10	+85	°C

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

NOTES:
1. Voltages with respect to ground.
2. Minimum DC input is −0.5V. During transitions, the inputs may undershoot to −2.0V or overshoot to 7.0V for periods less than 20 ns under no load conditions.
3. Under bias. Extended temperature versions are also available.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage	4.75	5.25	V
V_{IN}	Input Voltage	0	V_{CC}	V
V_O	Output Voltage	0	V_{CC}	V
T_A	Operating Temperature	0	+70	°C
t_R(4)	Input Rise Time		500	ns
t_F(4)	Input Fall Time		500	ns

NOTE:
4. t_R, t_F for CLK is 250 ns max.

D.C. CHARACTERISTICS $T_A = 0°C$ to $70°C$, $V_{CC} = 5.0V \pm 5\%$

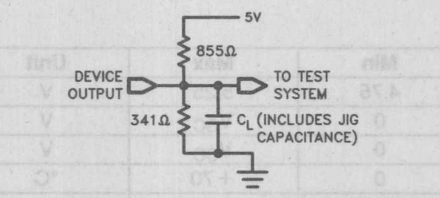
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}(5)	HIGH Level Input Voltage		2.0		$V_{CC} + 0.3$	V
V_{IL}(5)	LOW Level Input Voltage		−0.3		0.8	V
V_{OH}(6)	HIGH Level Output Voltage	$I_O = -4.0$ mA DC, V_{CC} = Min.	2.4			V
V_{OL}	LOW Level Output Voltage	$I_O = 4.0$ mA DC, V_{CC} = Min.			0.45	V
I_I	Input Leakage Current	V_{CC} = Max., GND < V_{IN} < V_{CC}			±10.0	μA
I_{OZ}	Output Leakage Current	V_{CC} = Max., GND < V_{OUT} < V_{CC}			±10.0	μA
I_{SC}(7)	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0.5V		20	30	mA
I_{SB}(8)	Standby Current (Standby)	V_{CC} = Max., V_{IN} = V_{CC} or GND		50	100	μA

$T_A = 0°C$ to $70°C$, $V_{CC} = 5.0V \pm 5\%$ (Continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{CC}	Power Supply Current (Active) (Turbo Bit Off) Device Prog. as 16-Bit Ctr. (See I_{CC} vs. Freq. Graph.)	V_{CC} = Max., $V_{IN} = V_{CC}$ or GND	No Load, Input Freq. = 1 MHz		10	15	mA

NOTES:
5. Absolute values with respect to device GND; all over and undershoots due to system or tester noise are included.
6. I_O at CMOS levels (3.84V) = −2 mA.
7. Not more than 1 output should be tested at a time. Duration of that test must not exceed 1 second.
8. With Turbo Bit Off, device automatically enters standby mode approximately 100 ns after last input transition.

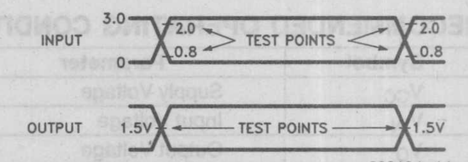
A.C. TESTING LOAD CIRCUIT



290194–13

C_L = 50 pF

A.C. TESTING INPUT, OUTPUT WAVEFORM



290194–14

A.C. Testing: Inputs are Driven at 3.0V for a Logic "1" and 0V for a Logic "0". Timing Measurements are made at 2.0V for a Logic "1" and 0.8V for a Logic "0" on inputs. Outputs are measured at a 1.5V point. Device input rise and fall times < 6 ns.

CAPACITANCE

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V, f = 1.0 MHz			20	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V, f = 1.0 MHz			20	pF
C_{CLK}	Clock Pin Capacitance	V_{IN} = 0V, f = 1.0 MHz			20	pF
C_{VPP}	V_{PP} Pin	CLK2 on 5C060, f = 1.0 MHz			50	pF

A.C. CHARACTERISTICS $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$, Turbo Bit On(9)

Symbol	From	To	Device 5C060-45 EP600-3			5C060-55 EP600			Non-(11) Turbo Mode	Unit
			Min	Typ	Max	Min	Typ	Max		
t_{PD1}	Input	Comb. Output			43			53	+25	ns
t_{PD2}	I/O	Comb. Output			45			55	+25	ns
t_{PZX}(10)	I or I/O	Output Enable			45			55	+25	ns
t_{PXZ}(10)	I or I/O	Output Disable			45			55	+25	ns
t_{CLR}	Asynch. Reset	Q Reset			45			55	+25	ns

NOTES:
9. Typical Values are at T_A = 25°C, V_{CC} = 5V, Active Mode.
10. t_{PZX} and t_{PXZ} are measured at ±0.5V from steady state voltage as driven by spec. output load. t_{PXZ} is measured with C_L = 5 pF.
11. If device is operated with Turbo Bit Off (Non-Turbo Mode), and the device has been inactive for approx. 100 ns, increase time by amount shown.

SYNCHRONOUS CLOCK MODE A.C. CHARACTERISTIC

T_A = 0°C to 70°C, V_{CC} = 5.0V ±5%, Turbo Bit On(9)

Symbol	Parameter	Device						Non-(11) Turbo Mode	Unit
		5C060-45 EP600-3			5C060-55 EP600				
		Min	Typ	Max	Min	Typ	Max		
f_{MAX}	Max. Frequency (Pipelined) (1/t_{SU}—No Feedback)			26.3			23.3		MHz
f_{CNT}	Max. Count Frequency (1/t_{CNT}—With Feedback)			22.2			18.2		MHz
t_{SU1}	Input Setup Time to CLK	36			41			+25	ns
t_{SU2}	I/O Setup Time to CLK	38			43			+25	ns
t_H	I or I/O Hold after CLK High	0			0				ns
t_{CO}	CLK High to Output Valid			22			25		ns
t_{CNT}	Register Output Feedback to Register Input—Internal Path	45			55			+25	ns
t_{CH}	CLK High Time	17.5			21.5				ns
t_{CL}	CLK Low Time	17.5			21.5				ns

ASYNCHRONOUS CLOCK MODE A.C. CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = 5.0V ±5%, Turbo Bit On(8)

Symbol	Parameter	Device						Non-(11) Turbo Mode	Unit
		5C060-45 EP600-3			5C060-55 EP600				
		Min	Typ	Max	Min	Typ	Max		
f_{ACNT}	Max. Count Frequency (1/t_{ACNT}—With Feedback)			22.2			18.2		MHz
t_{ASU1}	Input Setup Time to Asynch. Clock	10			10			+25	ns
t_{ASU2}	I/O Setup Time to Asynch. Clock	12			12			+25	ns
t_{AH}	Input or I/O Hold After Asynch. Clock	15			15				ns
t_{ACO}	Asynch. CLK to Output Valid			50			58	+25	ns
t_{ACNT}	Register Output Feedback to Register Input—Internal Path	45			55			+25	ns
t_{ACH}	Asynch. CLK High Time	17.5			21.5			+25	ns
t_{ACL}	Asynch. CLK Low Time	17.5			21.5			+25	ns

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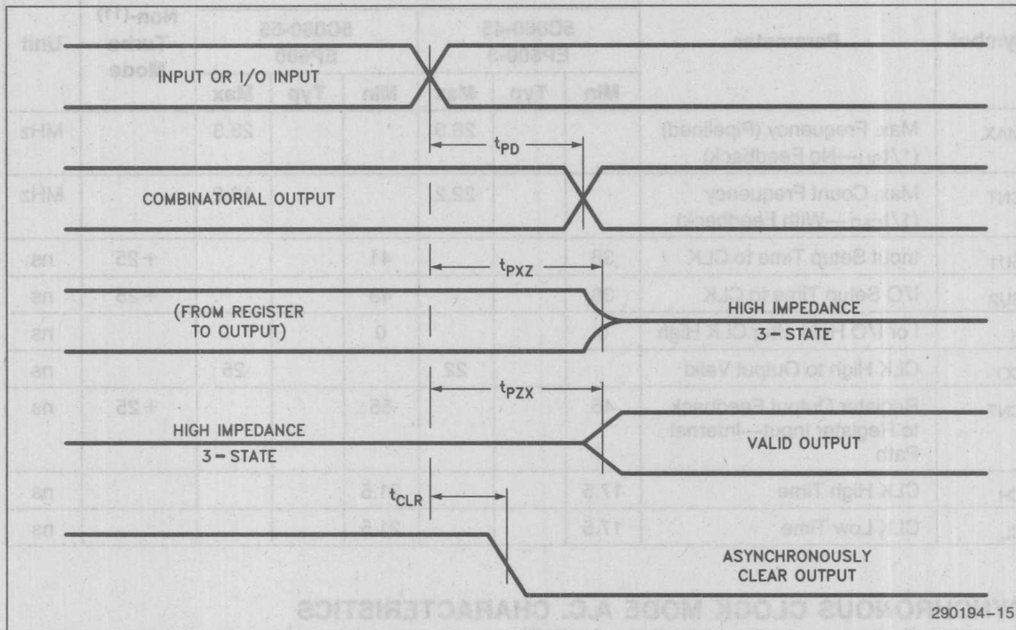
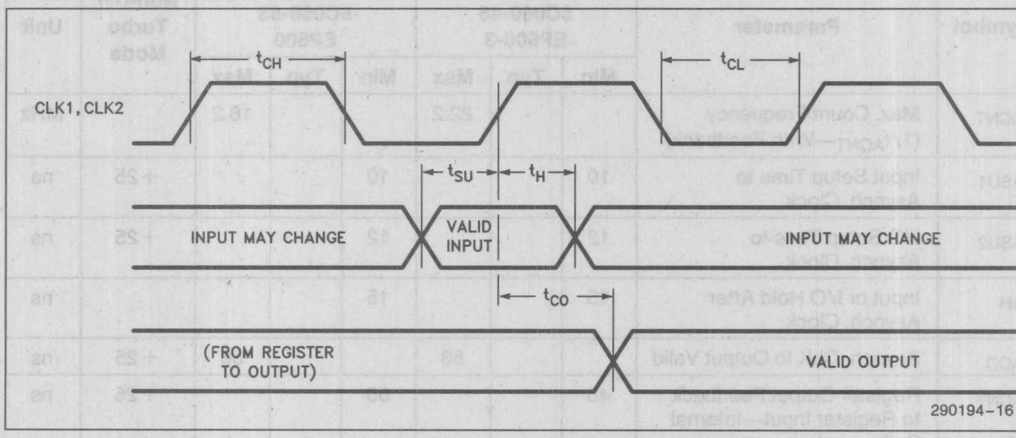
SWITCHING WAVEFORMS

COMBINATORIAL MODE



290194-15

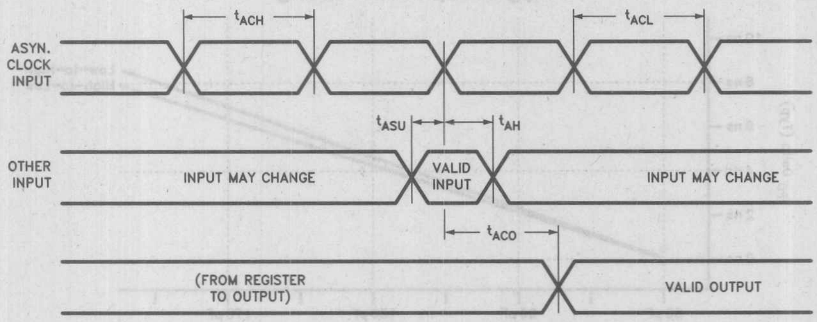
SYNCHRONOUS CLOCK MODE



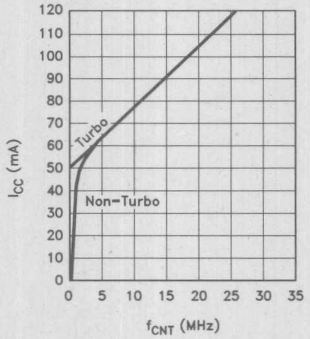
290194-16

SWITCHING WAVEFORMS (Continued)

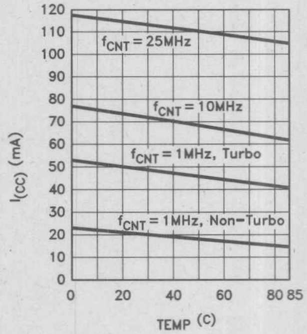
ASYNCHRONOUS CLOCK MODE



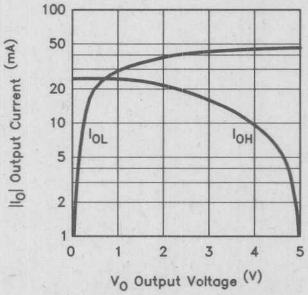
290194–17



Conditions:/T_A = 0°C, V_{CC} = 5.25V 290194–18

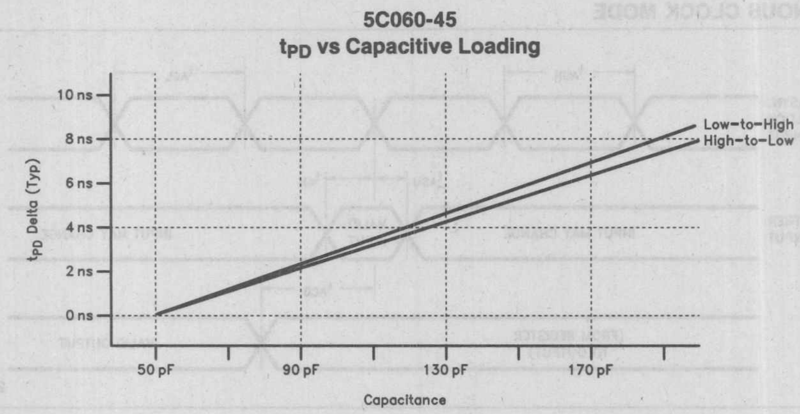


Conditions: V_{CC} = 5.25V, TTL inputs 290194–19



Conditions: T_A = 25°C 290194–20

SWITCHING WAVEFORMS (Continued)



290194-21

$T_A = 25°C$
$V_{CC} = 5.0V$
One output switching; typical path

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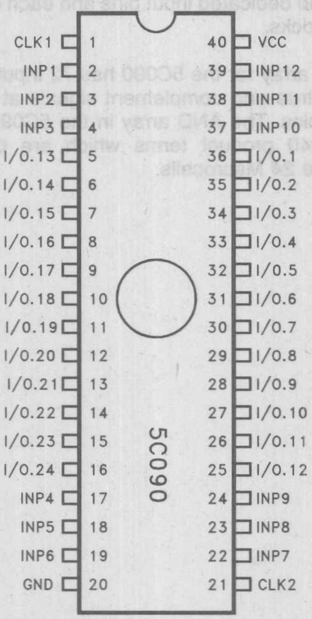
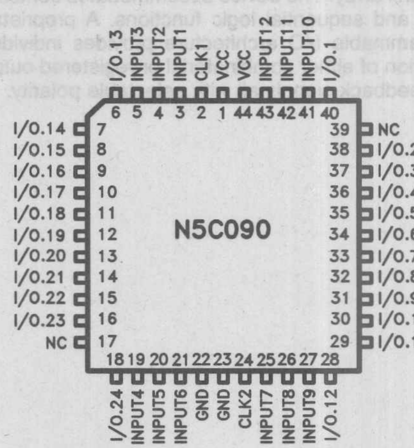
5C090
24-MACROCELL CMOS PLD

- **High-Performance LSI Semi-Custom Logic Alternative to Low-End Gate Arrays, TTL, and 74HC SSI and MSI Logic**
- **24 Macrocells with Programmable I/O Architecture; Up to 36 Inputs (12 Dedicated, 24 I/O) or 24 Outputs**
- **Programmable Output Registers. Can be Configured as D, T, SR, or JK Types**
- **t_{PD} (max) 50 ns, 26.3 MHz Pipelined, 20 MHz w/Feedback**
- **8 P-Terms, Selectable SOP Invert, Clear and OE P-Terms for Each Macrocell**
- **Programmable Clock System with 2 Synchronous Clocks and Asynchronous Clocking Option on all Registers**
- **Programmable Security Bit Allows Total Protection of Proprietary Designs**
- **CMOS EPROM Technology Based. UV Erasable (CerDIP) or OTP**
- **Programmable Low Power Option; 50 μA Typical Standby Current**
- **100% Generically Tested Logic Array**
- **100% Compatible with EP900**
- **40-Pin CerDIP/PDIP and 44-Pin PLCC Packages**
  (See Packaging Specification, Order Number 240800, Package Type D, P, and N)



290195–1



290195–2

Figure 1. 5C090 Pin Configurations

October 1993
Order Number: 290195-005

INTRODUCTION

The Intel 5C090 PLD (Programmable Logic Device) is a 24-macrocell, 40-pin, general-purpose device. The device can be used to replace low-end gate arrays, multiple programmable logic arrays and LS TTL and 74HC (CMOS) SSI and MSI logic devices. With its revolutionary programmable I/O architecture, the device has advanced functional capabilities beyond that of typical programmable logic. Figure 2 shows the global architecture of the device.

The 5C090 PLD uses CMOS EPROM (floating gate) cells as logic control elements instead of fuses. The CMOS EPROM technology reduces power consumption of PLDs to less than 20% of a comparable bipolar device without sacrificing speed performance. In addition, Intel's advanced CMOS II-E EPROM process technology enables greater logic densities to be achieved with superior speed and low-power performance over other comparable devices. Intel's ELPDs add the benefits of "zero" stand-by power not available on other programmable logic devices. EPROM technology allows these devices to be 100% factory tested by programming and erasing all the EPROM logic control elements.

The architecture of the 5C090 is based on the "Sum of Products" PLA (Programmable Logic Array) structure with a programmable AND array feeding into a fixed OR array. The device accommodates combinational and sequential logic functions. A proprietary programmable I/O architecture provides individual selection of either combinatorial or registered output and feedback signals all with selectable polarity.

A feature unique to the 5C090 is the ability to individually program the output registers as a D-, T-, SR-, or JK-type Flip-Flop without sacrificing the utilization of programmable AND logic. Additionally, each output register can be individually clocked from any of the input or feedback paths available within the AND array. With these features, a wide variety of logic functions can be simultaneously implemented—all on the same device.

ARCHITECTURE DESCRIPTION

The 5C090 has 12 dedicated inputs, 24 I/O pins which may be configured for input, output, or bidirectional operations, and 2 synchronous clock inputs. The 5C090 is packaged in a 40-lead windowed ceramic DIP or 44-lead plastic leaded chip carrier package and contains 24 programmable registers.

The basic Macrocell architecture for the 5C090 is shown in Figure 3. The 5C090 has 24 of these macrocells (one for each I/O pin). The Macrocell is organized in the familiar sum-of-products structure with a programmable AND array attached to a fixed OR term. The inputs to the programmable AND array originate from the true and complement signals from each of the dedicated input pins and each of the I/O control blocks.

The AND array for the 5C090 has 72 inputs derived from the true and complement signals at the input and I/O pins. The AND array in the 5C090 encompasses 240 product terms which are distributed among the 24 Macrocells.

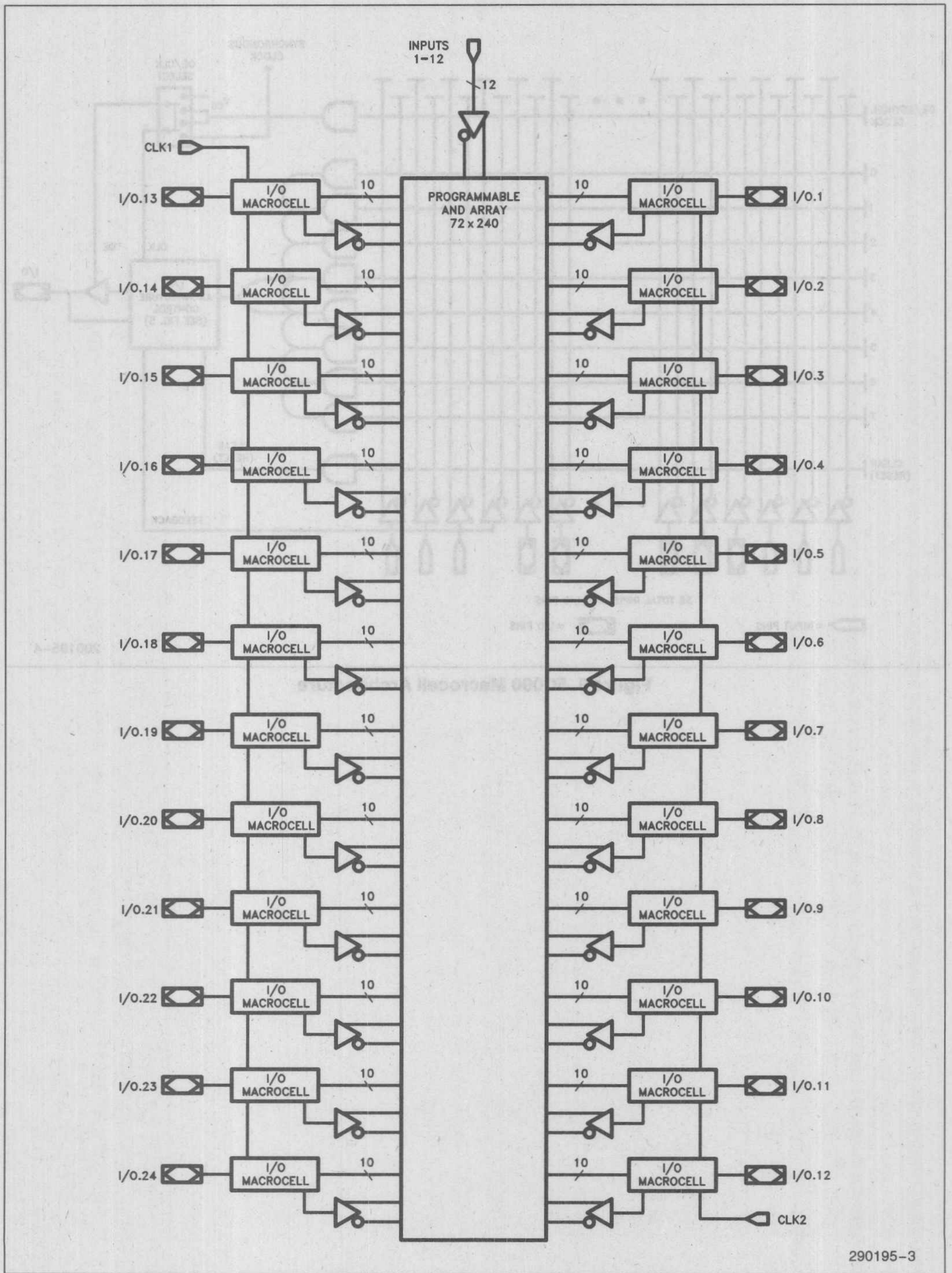


Figure 2. 5C090 Global Architecture

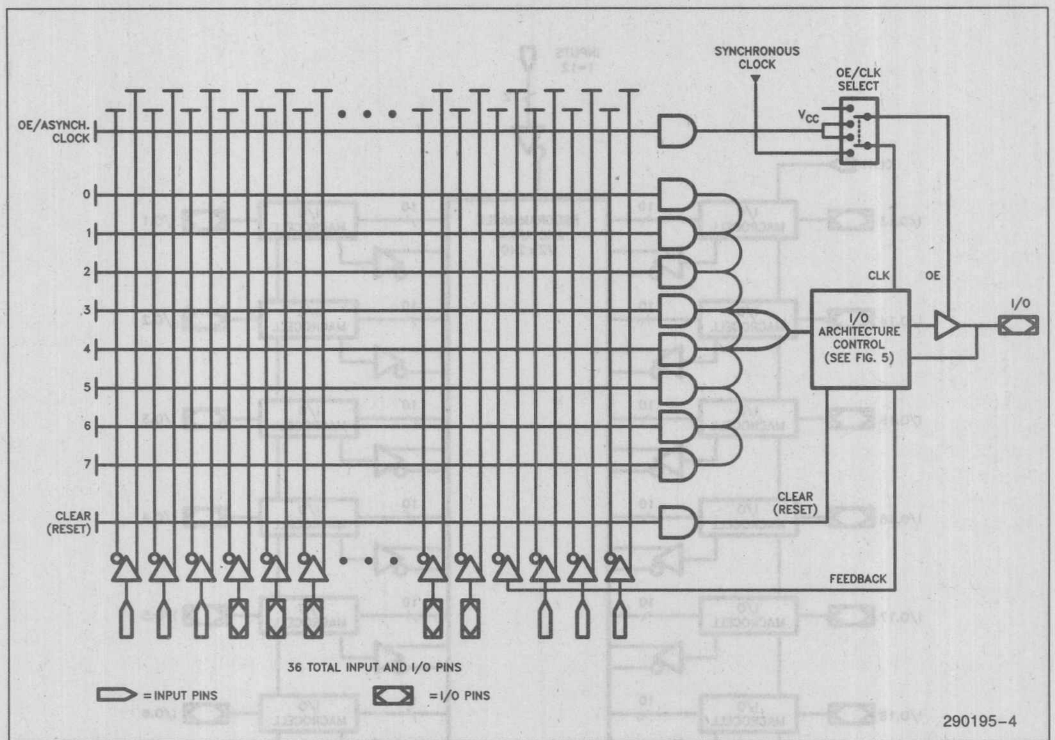


Figure 3. 5C090 Macrocell Architecture

The Macrocells contain ten product terms total. Eight of the ten product terms (AND gates) are dedicated for logic implementation. One product term on each Macrocell is used for RESET control to the output register associated with the Macrocell. The final product term is used for OUTPUT ENABLE/ Asynchronous Clock implementation.

Within the AND array, there is an EPROM connection at every intersection of an input signal (true and complement) and a product term to a given Macrocell. Before programming an erased device, every EPROM connection is made at every intersection. But during the programming process, these connections are opened so that only the desired connections remain. Therefore, the true or complement of any input signal can be connected to any product term. If both the true and complement connections of any signal are left intact, a logical false results on the output of the AND gate. However, if both the true and complement connections are open, then a logic "don't care" results on the AND gate. Lastly, if all the inputs of a product term are programmed open, then a logical true results on the output of the AND gate.

The 5C090 has two dedicated clock inputs to provide synchronous clock signals to the internal registers. Each of the clock signals controls half the total registers within the given device. For example, CLK1 provides synchronous clocking to the registers in Macrocells in the left half of the array while CLK2 controls the registers associated with Macrocells in the right half of the array. The advanced I/O architecture allows for any number of the registers to be synchronously clocked (from none to all). Both of the dedicated clock inputs latch the data into a given register when triggered on a positive edge.

MACROCELL ARCHITECTURE SELECTION

The 5C090 architecture provides each Macrocell with over 50 different possible I/O register configurations. Each I/O pin can be configured for combinatorial or registered output (true or complement) with feedback. In addition, four different types of output registers can be implemented into every I/O pin without any additional logic requirements. The feedback mechanism for each register back into the AND array can be programmed to provide for either registered feedback from the Macrocell or input feedback (treating the pin as an input). Another advantage of the advanced I/O capability of the 5C090 is the ability to individually clock each internal register from asynchronous clock signals.

Output Enable (OE)/Clock Selection

Two modes of operation are provided by the OE/CLK Select Multiplexer as a part of each Macrocell. One mode provides for three-state buffering of outputs while in the other mode, the outputs are always enabled. The operation of the OE/CLK Select Multiplexer sets the mode within a given Macrocell. Therefore, the output mode can be selected individually on every output. Figure 4 illustrates the two modes of OE/CLK operation.

MODE 0: THREE-STATE BUFFERING

In Mode 0, the three-state output buffer is controlled by a single product term originating from the AND array. The output is enabled when the product term is a logical true. Conversely, the output appears as high impedance when the product term is a logical false as shown in Table 1. In Mode 0, the Macrocell Flip-Flop is connected to its associated synchronous clock (either CLK1 or CLK2 depending upon the Macrocell's location within the device). Thus, the Macrocell Flip-Flop may be clocked by its respective synchronous clock but its output will not become valid until the output is enabled.

Table 1. Mode 0 Output Selection

Product Term	Output Buffer
FALSE	Three-State
TRUE	Enabled

MODE 1: OUTPUT BUFFER ENABLED

In Mode 1, the Output Buffer is always enabled. In addition, the Macrocell Flip-Flop is connected to the AND array. The Macrocell Flip-Flop may now be triggered from an asynchronous clock signal generated by the AND array logic to the OE/CLK multiplexable term. Mode 1 allows the Macrocell Flip-Flops to be individually clocked from any of the available signals in the AND array. Since both true and complement values appear in the AND array, the Flip-Flop may be clocked by positive-or negative-going signals at any input pin. Gated clock structures can be created since the Flip-Flop clock is created by a product term.

Invert Select EPROM Bit

The Invert Select EPROM bit is used to invert the product term input into the register. This applies to all inputs including double inputs on the JK and SR registers.

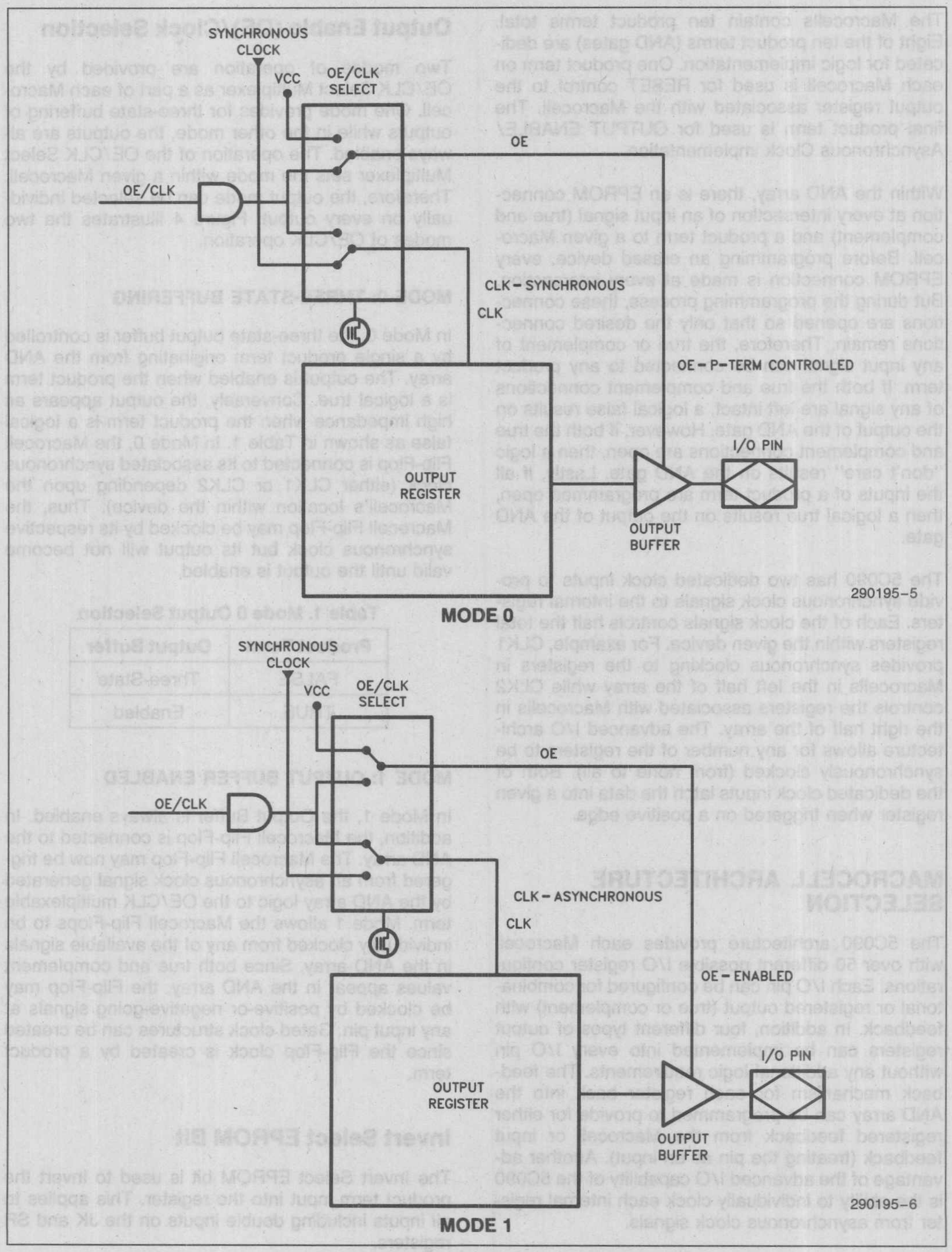


Figure 4. Output Enable/Clock Configuration

REGISTER SELECTION

The advanced I/O architecture of the 5C090 allows four different register types along with combinatorial output as illustrated in Figure 5a through e. The register types include a T, D, JK, or SR Flip-Flop and each Macrocell I/O structure may be independently configured. In addition, all registers have an individual asynchronous RESET control from a dedicated product term derived in the AND array. When this dedicated product term is a logical one, the Macrocell register is immediately cleared to a logical zero independent of the register clock. The RESET function occurs automatically on power-up.

Output Register Configuration

The four different register types shown in Figure 5 are described below.

D- or T-type Flip-Flops

When either a D- or T-type Flip-Flop is configured as part of the I/O structure, all eight of the product terms into the Macrocell are ORed together and fed into the register input.

JK or SR Registers

When either a JK or SR register is configured, the eight product terms are shared among two OR gates (one for the J or S input and the other for the K or R input). The allocation for these product terms for each of the register inputs is optimized by the iPLDS II development software.

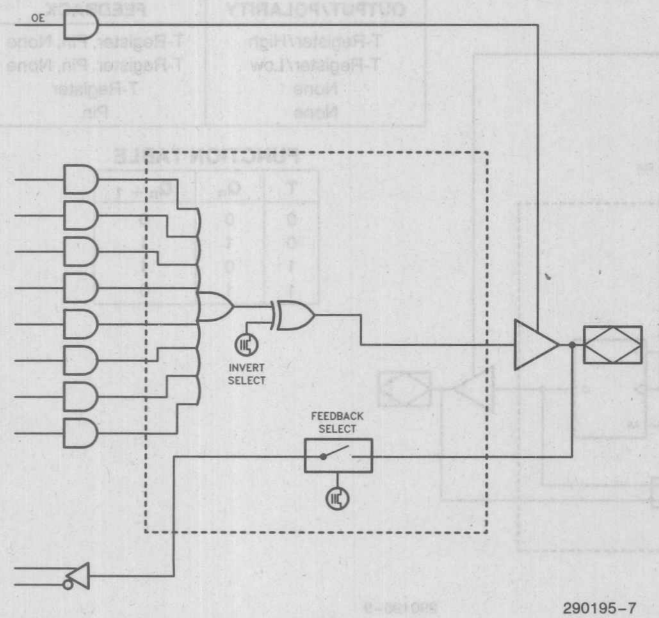
OUTPUT/FEEDBACK

The Output Select Multiplexer allows for either registered, combinatorial or no output.

The Feedback Select Multiplexer EPROM bit enables registered, I/O (using the pin for bidirectional input or just input), or no feedback to the AND array.

The Feedback Select is also important for building product terms with more than 8 products. The 8-product product term of a Macrocell can be fed back into the AND array and combined with still more signals to create a much larger product term (of more than 8-inputs). In addition, if the feedback product term is not to be output, then the iPLDS II will reserve the associated Macrocell pin and indicate it in the REPORT file. A reserved pin should be left floating (no connect) when assembled onto a circuit board.

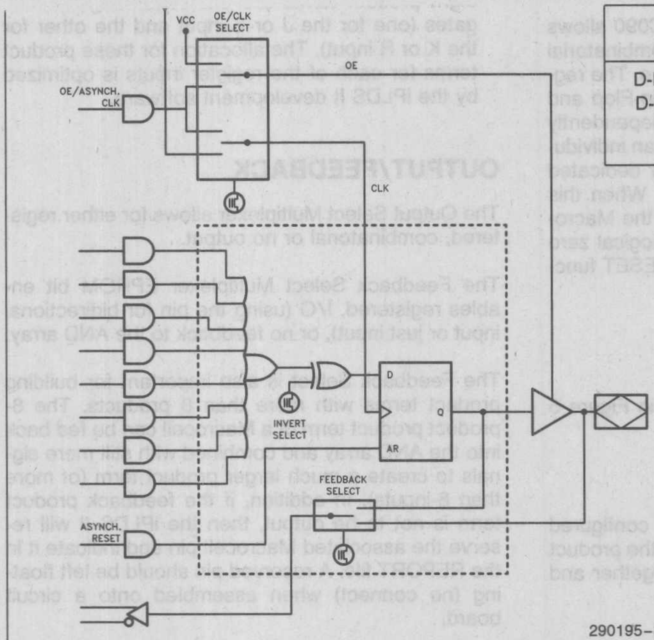
Any I/O pin may be configured as a dedicated input by selecting no output and pin feedback through the appropriate multiplexers.



I/O SELECTION

OUTPUT/POLARITY	FEEDBACK
Combinatorial/High	Pin, None
Combinatorial/Low	Pin, None
None	Pin

Figure 5a. Combinatorial I/O Configuration



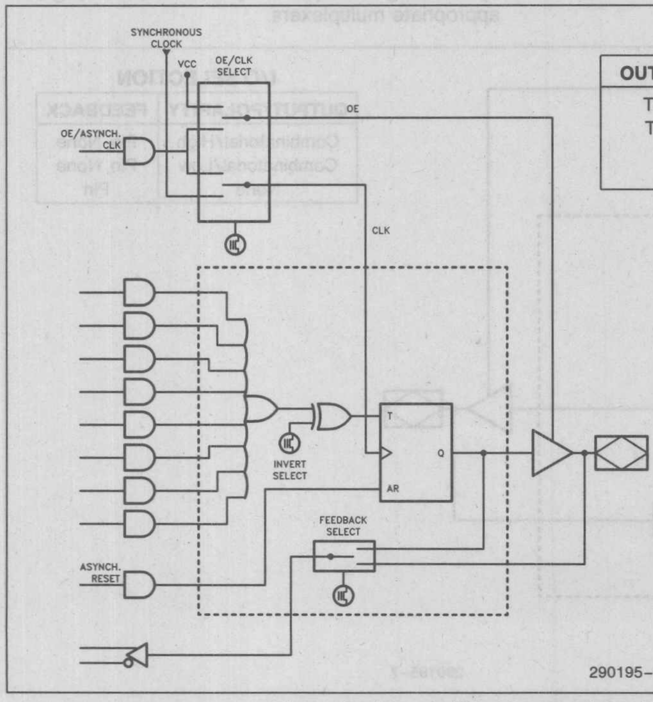
OUTPUT/ POLARITY	FEEDBACK
D-Register/High	D-Register, Pin, None
D-Register/Low	D-Register, Pin, None
None	D-Registered
None	Pin

FUNCTION TABLE

D	Q_n	Q_{n+1}
0	0	0
0	1	0
1	0	1
1	1	1

290195-8

Figure 5b. D-Type Flip-Flop Register Configuration



I/O SELECTION

OUTPUT/POLARITY	FEEDBACK
T-Register/High	T-Register, Pin, None
T-Register/Low	T-Register, Pin, None
None	T-Register
None	Pin

FUNCTION TABLE

T	Q_n	Q_{n+1}
0	0	0
0	1	1
1	0	1
1	1	0

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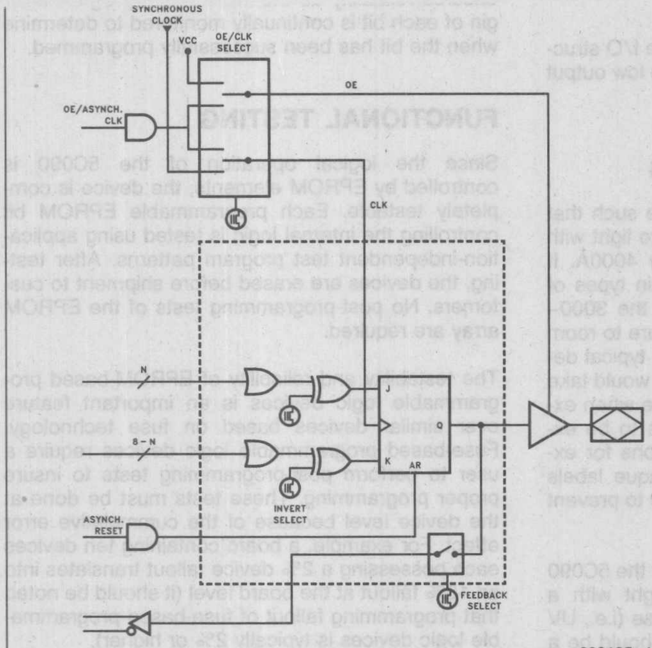
Figure 5c. Toggle Flip-Flop Register Configuration



I/O SELECTION

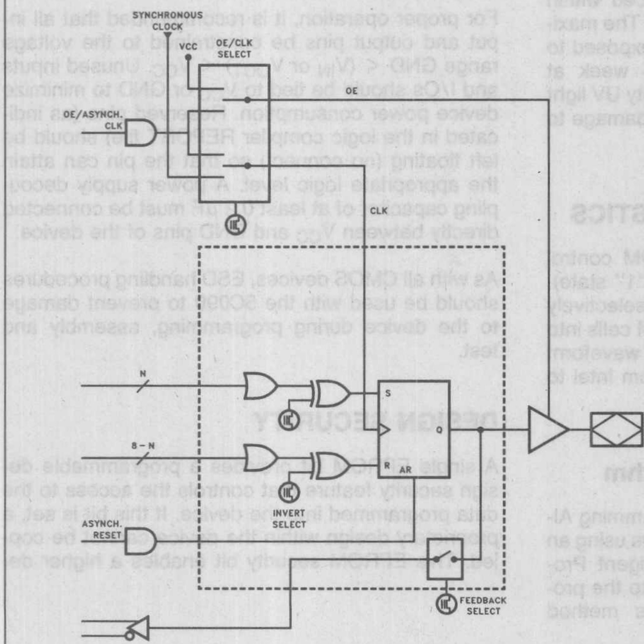
OUTPUT/POLARITY	FEEDBACK
JK Register/High	JK Register, None
JK Register/Low	JK Register, None
None	JK Register

FUNCTION TABLE

J	K	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

290195–10

Figure 5d. JK Flip-Flop Register Configuration



I/O SELECTION

OUTPUT/POLARITY	FEEDBACK
SR Register/High	SR Register, None
SR Register/Low	SR Register, None
None	SR Register

FUNCTION TABLE

S	R	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	Illegal	

290195–11

Figure 5e. SR Flip-Flop Register Configuration

Erased-State Configuration

Prior to programming or after erasing, the I/O structure is configured for combinatorial active low output with input (pin) feedback.

ERASURE CHARACTERISTICS

Erasure characteristics of the device are such that erasure begins to occur upon exposure to light with wavelengths shorter than approximately 4000Å. It should be noted that sunlight and certain types of flourescent lamps have wavelengths in the 3000–4000Å. Data shows that constant exposure to room level flourescent lighting could erase the typical device in approximately three years, while it would take approximately one week to cause erasure when exposed to direct sunlight. If the 5C090 is to be exposed to these types of lighting conditions for extended periods of time, conductive opaque labels should be placed over the device window to prevent unintentional erasure.

The recommended erasure procedure for the 5C090 is exposure to shortwave ultraviolet light with a wavelength of 2537Å. The integrated dose (i.e., UV intensity $\times$ exposure time) for erasure should be a minimum of fifteen (15) Wsec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 12,000 μW/cm^2 power rating. The 5C090 should be placed within one inch of the lamp tubes during erasure. The maximum integrated dose the 5C090 can be exposed to without damage is 7258 Wsec/cm^2 (1 week at 12,000 μW/cm^2). Exposure to high intensity UV light for longer periods may cause permanent damage to the device.

PROGRAMMING CHARACTERISTICS

Initially, and after erasure, all the EPROM control bits of the 5C090 are connected (in the "1" state). Each of the connected control bits are selectively disconnected by programming the EPROM cells into their "0" state. Programming voltage and waveform specifications are available by request from Intel to support programming of the 5C090.

Intelligent Programming Algorithm

The 5C090 supports the Intelligent Programming Algorithm which rapidly programs Intel ELPDs using an efficient and reliable method. The Intelligent Programming Algorithm is particularly suited to the production programming environment. This method ensures reliability as the incremental program margin of each bit is continually monitored to determine when the bit has been successfully programmed.

FUNCTIONAL TESTING

Since the logical operation of the 5C090 is controlled by EPROM elements, the device is completely testable. Each programmable EPROM bit controlling the internal logic is tested using application-independent test program patterns. After testing, the devices are erased before shipment to customers. No post-programming tests of the EPROM array are required.

The testability and reliability of EPROM-based programmable logic devices is an important feature over similar devices based on fuse technology. Fuse-based programmable logic devices require a user to perform post-programming tests to insure proper programming. These tests must be done at the device level because of the cummulative error effect. For example, a board containing ten devices each possessing a 2% device fallout translates into an 18% fallout at the board level (it should be noted that programming fallout of fuse-based programmable logic devices is typically 2% or higher).

DESIGN RECOMMENDATIONS

For proper operation, it is recommended that all input and output pins be constrained to the voltage range GND < (V_{IN} or V_{OUT}) < V_{CC}. Unused inputs and I/Os should be tied to V_{CC} or GND to minimize device power consumption. Reserved pins (as indicated in the logic compiler REPORT file) should be left floating (no connect) so that the pin can attain the appropriate logic level. A power supply decoupling capacitor of at least 0.2 μF must be connected directly between V_{CC} and GND pins of the device.

As with all CMOS devices, ESD handling procedures should be used with the 5C090 to prevent damage to the device during programming, assembly and test.

DESIGN SECURITY

A single EPROM bit provides a programmable design security feature that controls the access to the data programmed into the device. If this bit is set, a proprietary design within the device cannot be copied. This EPROM security bit enables a higher de-

gree of design security than fused-based devices since programmed data within EPROM cells is invisible even to microscopic evaluation. The EPROM security bit, along with all the other EPROM control bits, will be reset by erasing the device.

AUTOMATIC STAND-BY MODE

The 5C090 contains a programmable bit, the Turbo Bit, that optimizes operation for speed or for power savings. When the Turbo Bit is programmed (TURBO = ON), the device is optimized for maximum speed. When the Turbo Bit is not programmed (TURBO = OFF), the device is optimized for power savings by entering standby mode during periods of inactivity.

Figure 6 shows the device entering standby mode approximately 100 ns after the last input transition. When the next input transition is detected, the device returns to active mode. Wakeup time adds an additional 25 ns to the propagation delay through the device as measured from the first input. No delay will occur if an output is dependent on more than one input and the last of the inputs changes after the device has returned to active mode.

After erasure, the Turbo Bit is unprogrammed (OFF); automatic standby mode is enabled. When the Turbo Bit is programmed (ON), the device never enters standby mode.

LATCH-UP IMMUNITY

All of the input, I/O, and clock pins of the 5C090 have been designed to resist latch-up which is inherent in inferior CMOS structures. The 5C090 is designed with Intel's proprietary CMOS II-E EPROM process. Thus, each of the pins will not experience latch-up with currents up to ±100 mA and voltages ranging from −1V to (V_{CC} + 1V). Furthermore, the programming pin is designed to resist latch-up to the 13.5V maximum device limit.

SOFTWARE SUPPORT

Full logic compilation and functional simulation for the 5C090 is supported by PLDshell Plus software.

PLDshell Plus design software is Intel's user-friendly design tool for μPLD design. PLDshell Plus allows users to incorporate their preferred text editor, programming software, and additional design tools into an easy-to-use, menued design environment that includes Intel's PLDasm logic compiler and simulation software along with disassembly, conversion, and translation utilities. The PLDasm compiler and simulator software accepts industry-standard PDS source files that express designs as Boolean equations, truth tables, or state machines. On-line help, data sheet briefs, technical notes, and error message information, along with waveform viewing/printing capability make the design task as easy as possible. PLDshell Plus software is available from Intel Literature channels or from your local Intel sales representative.

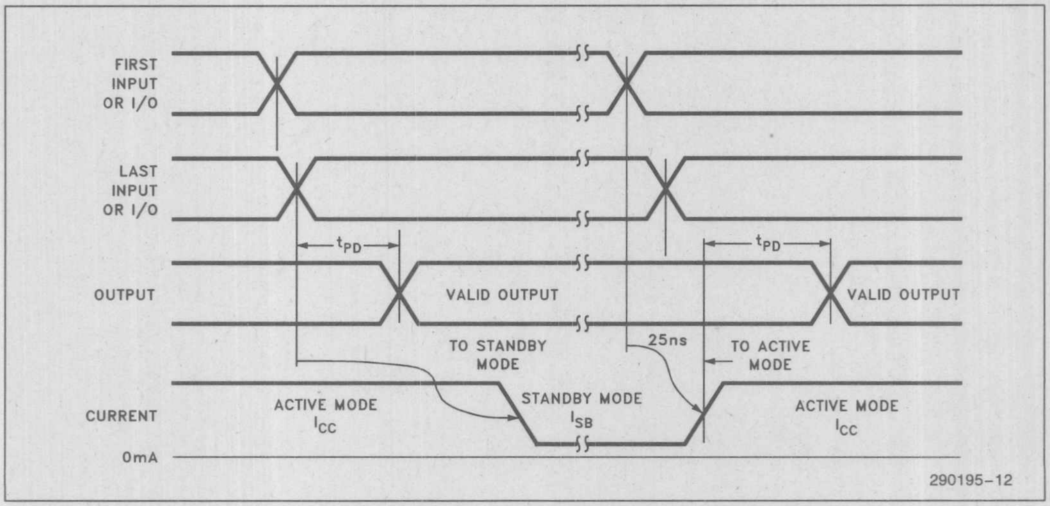


Figure 6. 5C090 Standby and Active Mode Transitions

Tools that support schematic capture and timing simulation for the 5C060 are available. Please refer to the "Development Tools" section of the Programmable Logic Handbook.

The 5C090 is also supported by third-party logic compilers such as ABEL*, CUPL*, PLDesigner, Log/IC*, etc. Programming support is provided by third-party programmer companies such as Data I/O, Logical Devices, STAG, etc. Please refer to the "Third-Party Support" lists in the *Programmable Logic* handbook for complete information and vendor contacts.

ORDERING INFORMATION

t_{PD} (ns)	t_{CO} (ns)	f_{MAX} (MHz)	Order Code	Package	Operating Range
50	23	26.3	D5C090-50	CERDIP	Commercial
			P5C090-50	PDIP	
			N5C090-50	PLCC	
60	25	21.7	D5C090-60	CERDIP	Commercial
			P5C090-60	PDIP	
			N5C090-60	PLCC	
50	23	26.3	TN5C090-50	PLCC	Industrial

*ABEL is a trademark of Data I/O, Corporation. CUPL is a trademark of Logical Devices, Inc. PLDesigner is a trademark of MINC, Inc. Log/IC is trademark of ISDATA, Inc.

ABSOLUTE MAXIMUM RATINGS*

Symbol	Parameter	Min	Max	Units
V_{CC}	Supply Voltage(1)	−2.0	7.0	V
V_{PP}	Programming Supply Voltage(1)	−2.0	13.5	V
V_I	DC Input Voltage(1)(2)	−0.5	$V_{CC}+0.5$	V
t_{stg}	Storage Temperature	−65	+150	°C
t_{amb}	Ambient Temperature(3)	−10	+85	°C

NOTES:
1. Voltages with respect to ground.
2. Minimum DC input is −0.5V. During transitions, the inputs may undershoot to −2.0V or overshoot to +7.0V for periods less than 20 ns under no load conditions.
3. Under bias. Extended temperature versions are also available.

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage	4.75	5.25	V
V_{IN}	Input Voltage	0	V_{CC}	V
V_O	Output Voltage	0	V_{CC}	V
T_A	Operating Temperature	0	+70	°C
t_R	Input Rise Time		500	ns
t_F	Input Fall Time		500	ns

NOTE:
4. t_R, t_F for CLK is 250 ns max.

2

D.C. CHARACTERISTICS $T_A = 0°C$ to $70°C$, $V_{CC} = 5.0V \pm 5\%$

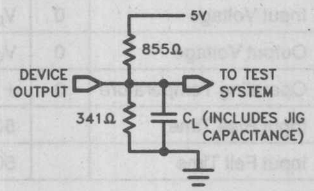
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}(5)	HIGH Level Input Voltage		2.0		$V_{CC} + 0.3$	V
V_{IL}(5)	LOW Level Input Voltage		−0.3		0.8	V
V_{OH}(6)	HIGH Level Output Voltage	$I_O = -4.0$ mA DC, $V_{CC} =$ Min.	2.4			V
V_{OL}	LOW Level Output Voltage	$I_O = 4.0$ mA DC, $V_{CC} =$ Min.			0.45	V
I_I	Input Leakage Current	$V_{CC} =$ Max., GND $< V_{IN} < V_{CC}$			±10.0	μA
I_{OZ}	Output Leakage Current	$V_{CC} =$ Max., GND $< V_{OUT} < V_{CC}$			±10.0	μA
I_{SC}(7)	Output Short Circuit Current	$V_{CC} =$ Max., $V_{OUT} = 0.5V$		20	30	mA
I_{SB}(8)	Standby Current (Standby)	$V_{CC} =$ Max., $V_{IN} = V_{CC}$ or GND		50	150	μA

D.C. CHARACTERISTICS $T_A = 0°C$ to $70°C$, $V_{CC} = 5.0V \pm 5\%$ (Continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{CC}	Power Supply Current (Active) (Turbo Bit Off) Device Prog. as Two 12-Bit Ctrs. (See I_{CC} vs. Freq. Graph)	V_{CC} = Max., $V_{IN} = V_{CC}$ or GND	No Load, Input Freq. = 1 MHz		15	25	mA

NOTES:
5. Absolute values with respect to device GND; all over and undershoots due to system or tester noise are included.
6. I_O at CMOS levels (3.84V) = −2 mA.
7. Not more than 1 output should be tested at a time. Duration of that test must not exceed 1 second.
8. With Turbo Bit Off, device automatically enters standby mode approximately 100 ns after last input transition.

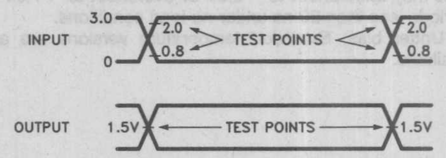
A.C. TESTING LOAD CIRCUIT



290195-13

C_L = 50 pF

A.C. TESTING INPUT, OUTPUT WAVEFORM



290195-14

A.C. Testing: Inputs are Driven at 3.0V for a Logic "1" and 0V for a Logic "0". Timing Measurements are made at 2.0V for a Logic "1" and 0.8V for a Logic "0" on inputs. Outputs are measured at a 1.5V point. Device input rise and fall times < 6 ns.

CAPACITANCE

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V, f = 1.0 MHz			20	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V, f = 1.0 MHz			20	pF
C_{CLK}	Clock Pin Capacitance	V_{IN} = 0V, f = 1.0 MHz			20	pF
C_{VPP}	V_{PP} Pin	CLK2 on 5C090, f = 1.0 MHz			80	pF

A.C. CHARACTERISTICS $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$, Turbo Bit On(9)

Symbol	From	To	Device 5C090-50 EP900-2			5C090-60 EP900			Non-(11) Turbo Mode	Unit
			Min	Typ	Max	Min	Typ	Max		
t_{PD1}	Input	Comb. Output			45			55	+25	ns
t_{PD2}	I/O	Comb. Output			50			60	+25	ns
t_{PZX}(10)	I or I/O	Output Enable			50			60	+25	ns
t_{PXZ}(10)	I or I/O	Output Disable			50			60	+25	ns
t_{CLR}	Asynch. Reset	Q Reset			50			60	+25	ns

NOTES:
9. Typical Values are at T_A = 25°C, V_{CC} = 5V, Active Mode.
10. t_{PZX} and t_{PXZ} are measured at ±0.5V from steady state voltage as driven by spec. output load. t_{PXZ} is measured with C_L = 5 pF.
11. If device is operated with Turbo Bit Off (Non-Turbo Mode) and the device has been inactive for approx. 100 ns, increase time by amount shown.

SYNCHRONOUS CLOCK MODE A.C. CHARACTERISTIC

T_A = 0°C to 70°C, V_{CC} = 5.0V ±5%, Turbo Bit On[9]

Symbol	Parameter	Device						Non-[11] Turbo Mode	Unit
		5C090-50 EP900-2			5C090-60 EP900				
		Min	Typ	Max	Min	Typ	Max		
f_{MAX}	Max. Frequency (Pipelined) (1/t_{SU}—No Feedback)			26.3			21.7		MHz
f_{CNT}	Max. Count Frequency (1/t_{CNT}—With Feedback)			20			16.7		MHz
t_{SU1}	Input Setup Time to CLK	36			43			+25	ns
t_{SU2}	I/O Setup Time to CLK	38			46			+25	ns
t_H	I or I/O Hold after CLK High	0			0				ns
t_{CO}	CLK High to Output Valid			23			25		ns
t_{CNT}	Register Output Feedback to Register Input—Internal Path	50			60			+25	ns
t_{CH}	CLK High Time	17.5			23				ns
t_{CL}	CLK Low Time	17.5			23				ns

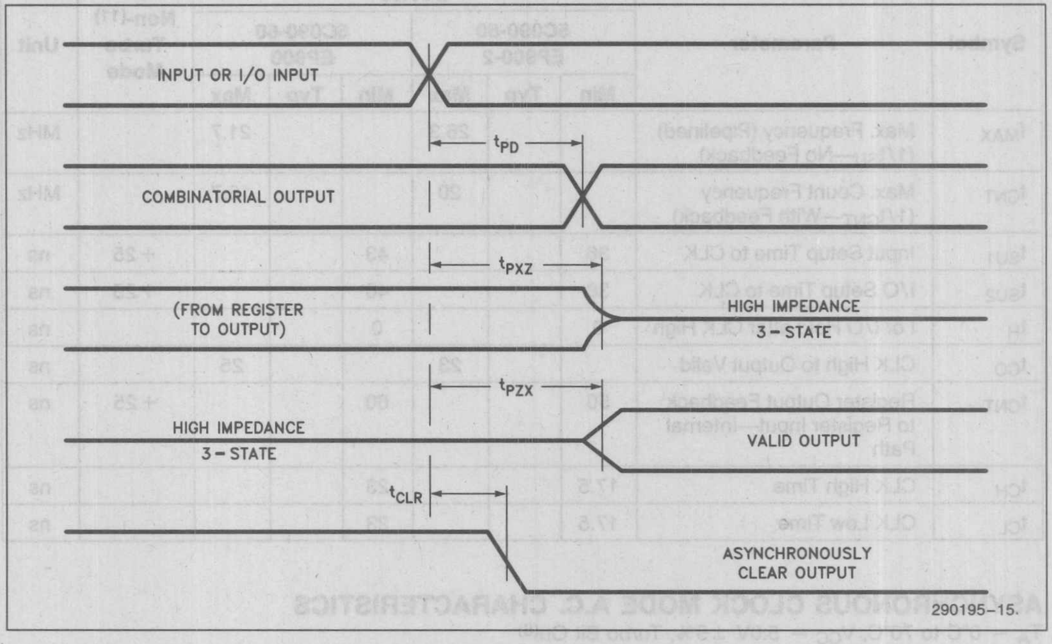
ASYNCHRONOUS CLOCK MODE A.C. CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = 5.0V ±5%, Turbo Bit On[8]

Symbol	Parameter	Device						Non-[11] Turbo Mode	Unit
		5C090-50 EP900-2			5C090-60 EP900				
		Min	Typ	Max	Min	Typ	Max		
f_{ACNT}	Max. Count Frequency (1/t_{ACNT}—With Feedback)			20			16.7		MHz
t_{ASU1}	Input Setup Time to Asynch. Clock	10			10			+25	ns
t_{ASU2}	I/O Setup Time to Asynch. Clock	13			15			+25	ns
t_{AH}	Input or I/O Hold After Asynch. Clock	15			15				ns
t_{ACO}	Asynch. CLK to Output Valid			48			59	+25	ns
t_{ACNT}	Register Output Feedback to Register Input—Internal Path	50			60			+25	ns
t_{ACH}	Asynch. CLK High Time	17.5			23			+25	ns
t_{ACL}	Asynch. CLK Low Time	17.5			23			+25	ns

SWITCHING WAVEFORMS

COMBINATORIAL MODE



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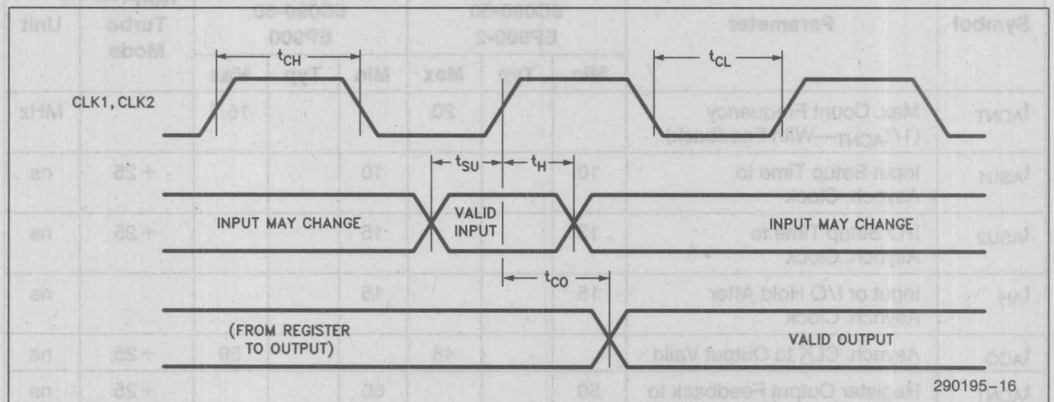
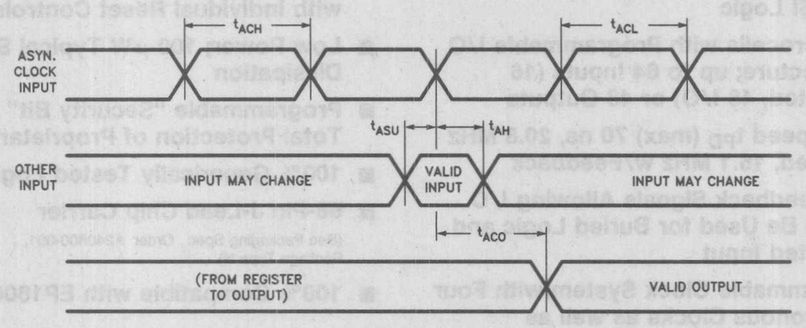
SYNCHRONOUS CLOCK MODE



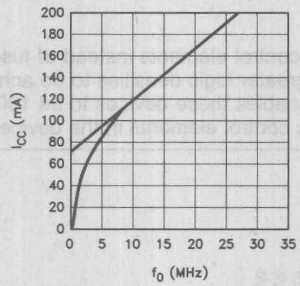
290195–16

ASYNCHRONOUS CLOCK MODE



290195–17

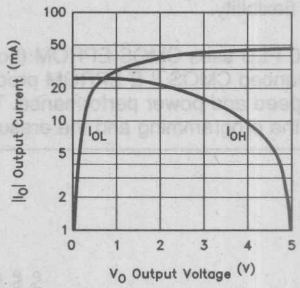
5C090
Current in Relation to Frequency



290195–18

Conditions: $T_A = 0°C$, $V_{CC} = 5.25V$

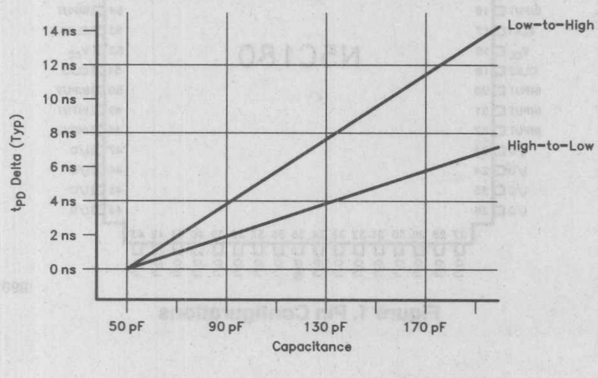
5C090
Output Drive Current in Relation to Voltage



290195–19

Conditions: $T_A = 25°C$

5C090
t_{PD} Derating vs. Capacative Loading



290195–20

CONDITIONS:
$T_A = 25°C$, $V_{CC} = 5.0V$

intel®

5C180
48-MACROCELL CMOS PLD

- **High-Performance LSI Semicustom Logic Alternative for TTL and 74HC SSI and MSI Logic**
- **48 Macrocells with Programmable I/O Architecture; up to 64 Inputs (16 Dedicated, 48 I/O) or 48 Outputs**
- **High Speed t_{PD} (max) 70 ns, 20.8 MHz Pipelined, 16.1 MHz w/Feedback**
- **Dual Feedback Signals Allowing I/O Pins to Be Used for Buried Logic and Dedicated Input**
- **Programmable Clock System with Four Synchronous Clocks as well as Asynchronous Clocking Option on All Registers**
- **Programmable Registers. Can Be Configured as D, T, SR or JK Types with Individual Reset Controls**
- **Low Power; 100 μW Typical Standby Dissipation**
- **Programmable "Security Bit" Allows Total Protection of Proprietary Designs**
- **100% Generically Tested Logic Array**
- **68-Pin J-Lead Chip Carrier**
  (See Packaging Spec., Order #240800-001, Package Type N)
- **100% Compatible with EP1800**

The Intel 5C180 PLD (Programmable Logic Device) is a CMOS, 48-macrocell, general-purpose PLD. This user-customizable Logic Device is available in a 68-pin PLCC package and has the benefits of low power and increased flexibility.

The 5C180 PLD uses CMOS EPROM (floating gate) cells as logic control elements instead of fuses. Use of Intel's advanced CMOS II-E EPROM process technology enables greater logic densities to be achieved with superior speed and power performance. The EPROM technology enables these devices to be 100% factory tested by the programming and the erasure of all the EPROM logic control elements in the device.

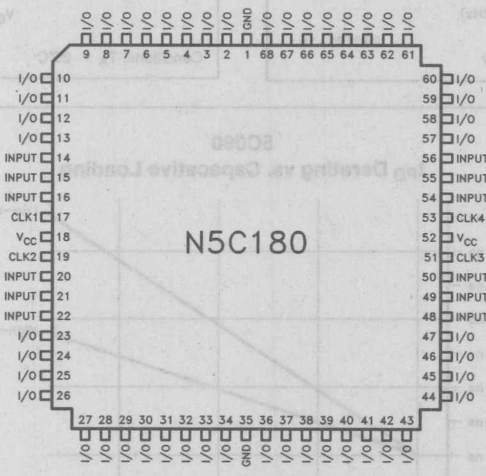


Figure 1. Pin Configurations

September 1993
Order Number: 290111-009

INTRODUCTION

The architecture of the 5C180 is based on the "Sum of Products" PLA (Programmable Logic Array) structure with a programmable AND array feeding into a fixed OR array. The 48 macrocells of the 5C180 can be partitioned into 4 identical quandrants each containing 12 macrocells. This device makes use of a segmented PLA structure with local and global bus structures to provide for increased performance and greater device utilization. The 5C180 has unique architectural features that allow programming of all 48 registers to D, T, SR or JK configurations without sacrificing product terms. These registers can be either clocked asynchronously or in banks with four synchronous clocks. In addition, the 16 global macrocells have two independent feedback paths to the array that allow for buried logic implementation together with use of the I/O pin for input functions.

ARCHITECTURE DESCRIPTION

Externally, the 5C180 provides 12 dedicated data inputs, 4 synchronous clock inputs, and 48 I/O pins which may be individually programmed for input, output, or bi-directional operation.

The Block Diagram is shown in Figure 2 with pin numbers for the PLCC package. The internal architecture is organized in familiar sum-of-products (AND-OR) structure. The 5C180 houses a total of 480 product terms distributed among 48 Macrocells. The basic Macrocell structure is shown in Figure 3. Input and feedback signals are selectively connected to product terms via EPROM cells. The output of the AND array feeds a fixed OR gate to produce sum-of-products logic. The final output may be combinatorial or registered, programmed active high or low. Combinatorial, registered, or pin feedback is also user-defined.

The 5C180 is partitioned into 4 identical quadrants. Each quadrant contains 12 Macrocells. Input signals to the Macrocells come from the 5C180 Local and Global bus structures. These two buses comprise an 88-input AND array for each quadrant. The output of each Macrocell feeds an I/O Architecture Control Block which contains output and feedback selection.

Four dedicated clock inputs provide synchronous clock signals to the 5C180 internal registers. There is one synchronous clock per quadrant. Therefore each clock signal controls a bank of 12 registers. CLK1 may be connected to registers in Macrocells 1–12, CLK2 with Macrocells 13–24, CLK3 with Macrocells 25–36, and CLK4 with Macrocells 37–48. With synchronous clocks, the flip-flops are positive edge triggered. Both true and complement signals for each dedicated clock input may also be used within the AND array. All 48 internal registers may be individually programmed for synchronous or asynchronous clocking. Asynchronous clocking is possible via a Macrocell product term. Clock inputs not used for synchronous clock signals may be used as global bus inputs.

Invert Select EPROM Bit

The Invert Select EPROM bit is used to invert the product term input into the register. This applies to all inputs including double inputs on JK and SR registers. The invert option allows the highest possible logic utilization by use of deMorgan logic inversion.

At each intersecting point in the logic array there exists an EPROM-type programmable connection. Initially, all connections are complete. This means that both the true and complement of all inputs are connected to each product term. Connections are opened during the programming process. Therefore any product term can be connected to the true or complement of any input. When both the true and complement connections of any input are left intact, a logical false results on the output of the AND gate. If both the true and complement connections of any input are programmed open, then a logical "don't care" results for that input. If all inputs for a product term are programmed open, then a logical true results on the output of the AND gate.

BUS STRUCTURE

Input and feedback signals are connected to each 5C180 Macrocell via a Local and Global Bus. Figure 4 shows the Macrocell-Bus interface for Quadrant D. The Global Bus contains 64 input signals while the Local Bus has 24.

Within the 5C180 Macrocell, the product-terms share the entire bus structure. Therefore, a logical AND of any of the variables (or their complements) that is present on the buses may be produced by each product term.

All quadrants share the same Global Bus. Inputs to the bus come from the true and complement signals of the 12 dedicated data inputs, 4 clock inputs, and the 16 Global Macrocell pin feedback signals.

Each quadrant has its own Local Bus. Inputs to this bus come from the 12 quadrant Macrocells. For the eight Local Macrocells, the signals can be either from the Macrocell internal logic or from the pin. For the four Global Macrocells, the signals come from the Macrocell internal logic only.

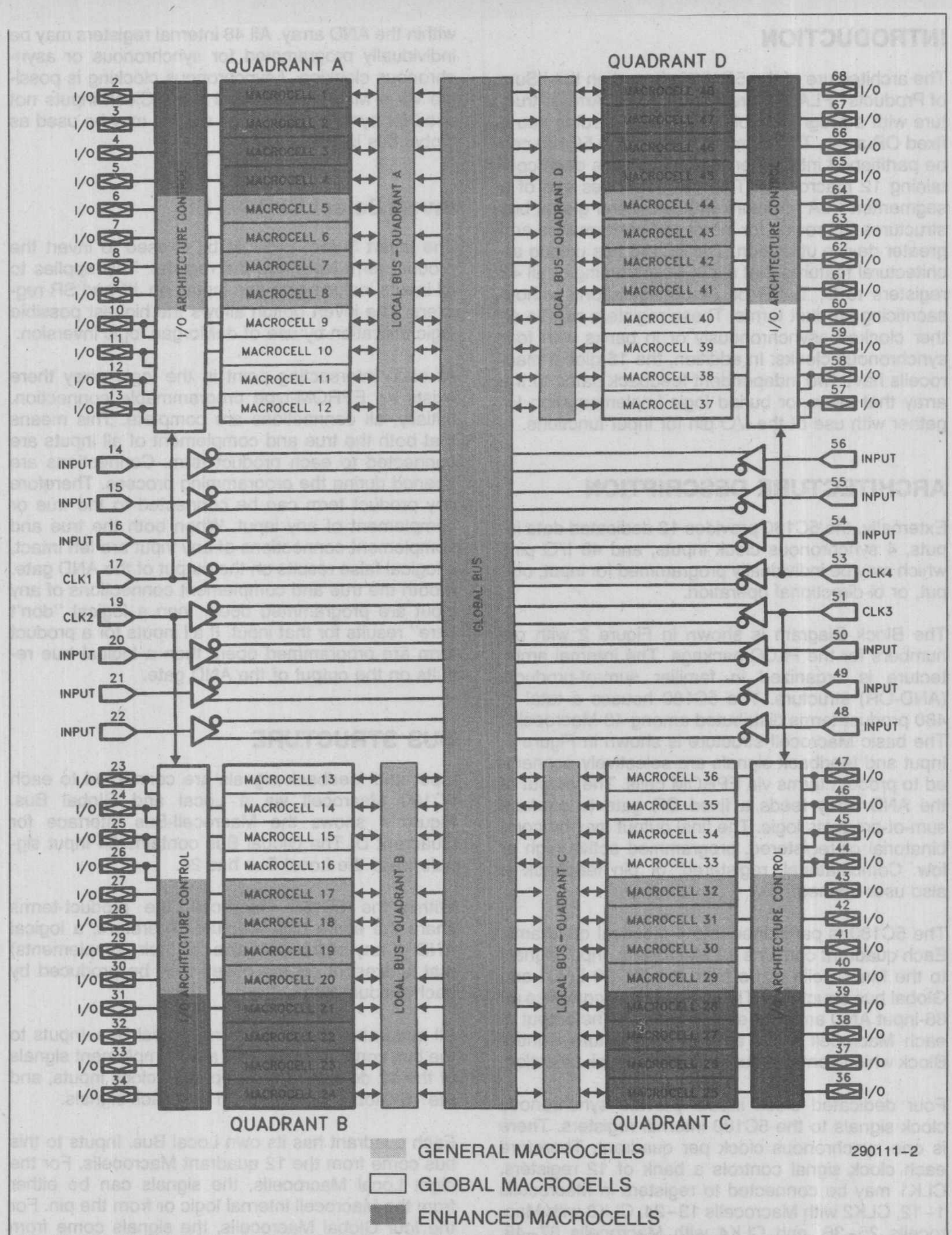


Figure 2. 5C180 Block Diagram—PLCC Package

Table 1 summarizes the Macrocell interconnect.

Table 1. Macrocell Interconnect

	Pin #	Macro-cell #	Feedback Structure	Feedback Interconnect
Quad A	2–9 10–13	1–8 9–12	Local Local Global	Quad A Quad A All
Quad B	23–26 27–34	13–16 17–24	Local Global Local	Quad B All Quad B
Quad C	36–43 44–47	25–32 33-36	Local Local Global	Quad C Quad C All
Quad D	57–60 61–68	37–40 41–48	Local Global Local	Quad D All Quad D

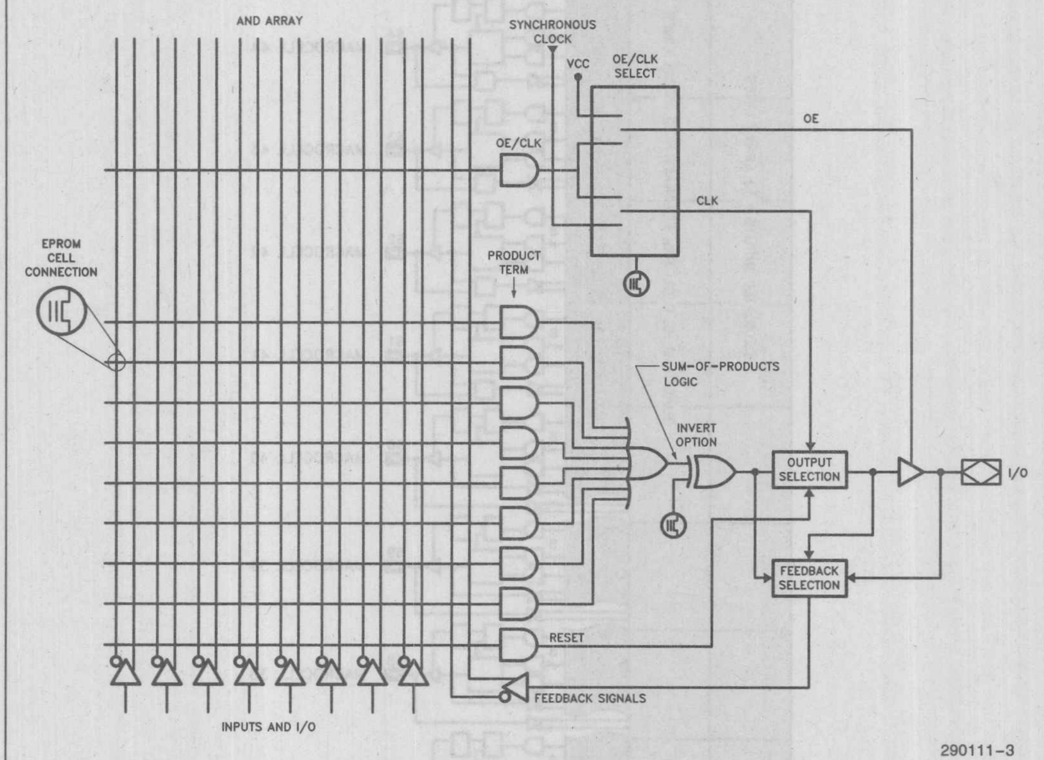


Figure 3. Basic Macrocell Architecture of the 5C180

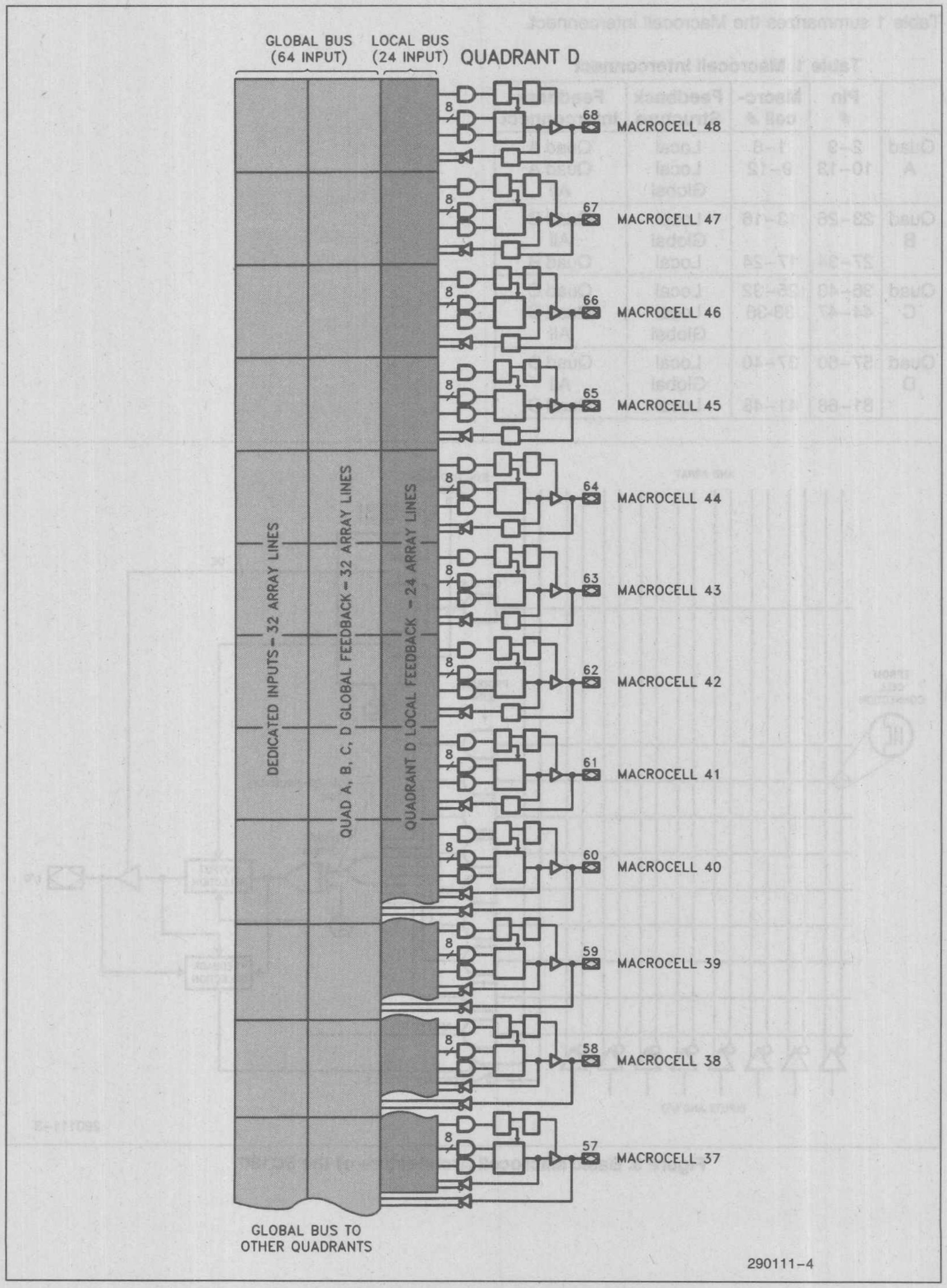


Figure 4. Quadrant "D" Bus Interface

5C180 MACROCELLS

Within each 5C180 quadrant there are two different types of Macrocells; Local Macrocells, Figure 5, and Global Macrocells, Figure 6. Both types share an 88-input AND array and contain a total of ten product terms. Eight product terms are dedicated for logic implementation. One product term is reserved for Asynchronous Clear to the Macrocell register. The remaining product term is used for Output Enable/ Asynchronous Clock implementation. Each 5C180 product term represents an 88-input AND gate. The I/O Architecture Control Block provides each Macrocell with both combinatorial and registered I/O configurations.

Local Macrocells provide one feedback path into the AND array. Combinatorial, registered or pin feedback may be selected from the Feedback Select Multiplexer. The selected feedback signal is then routed to the quadrant local bus. Therefore, the Local Macrocell feedback communicates only to Macrocells within the same quadrant. There are a total of 32 Local Macrocells within the 5C180, with eight per quadrant.

Local macrocells are divided into two groups: General Macrocells and Enchanced Macrocells. The Enhanced Macrocells are architecturally identical to the General Macrocells but operate at higher speeds. These speed differences are reflected in the specification tables.

Global Macrocells contain two independent feedback paths to the AND array. Combinatorial or registered feedback is supplied to the local bus and pin feedback is supplied to the global bus. The "dual feedback" capability allows the Macrocell to be used for internal logic functions as well as a dedicated input pin. To obtain this configuration, the output buffer must be disabled. If the Global Macrocell I/O pin is not being used as a dedicated input, the Macrocell logic may be fed back along the global bus allowing routing to any of the 5C180's 48 Macrocells. There are 16 Global Macrocells contained in the 5C180, four per quadrant.

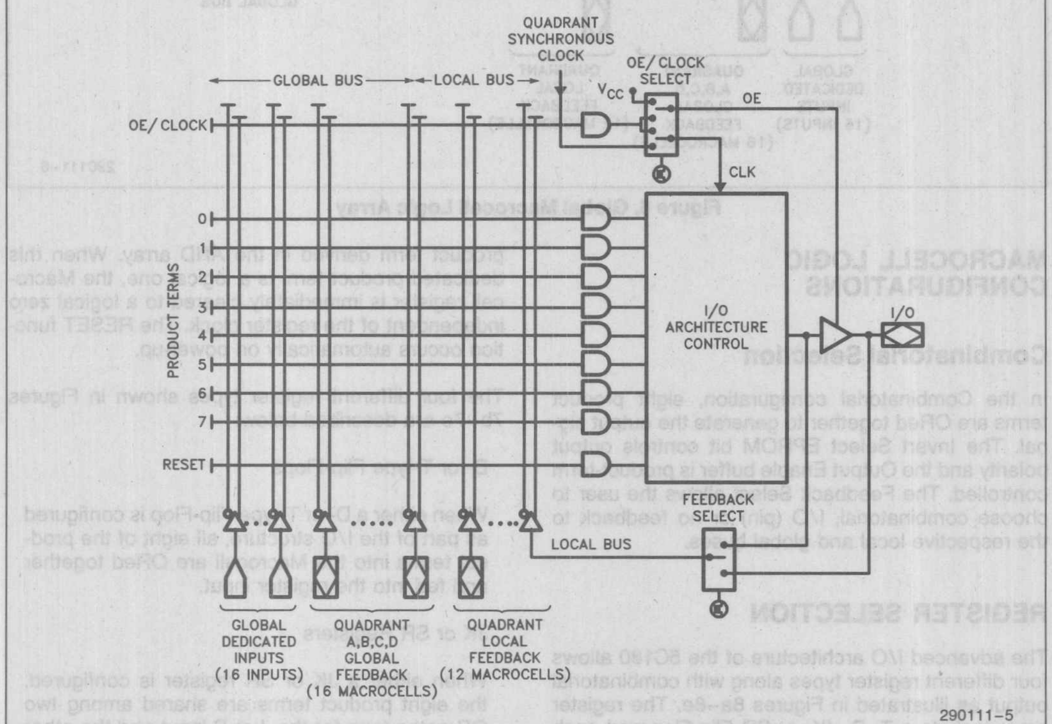


Figure 5. Local Macrocell Logic Array

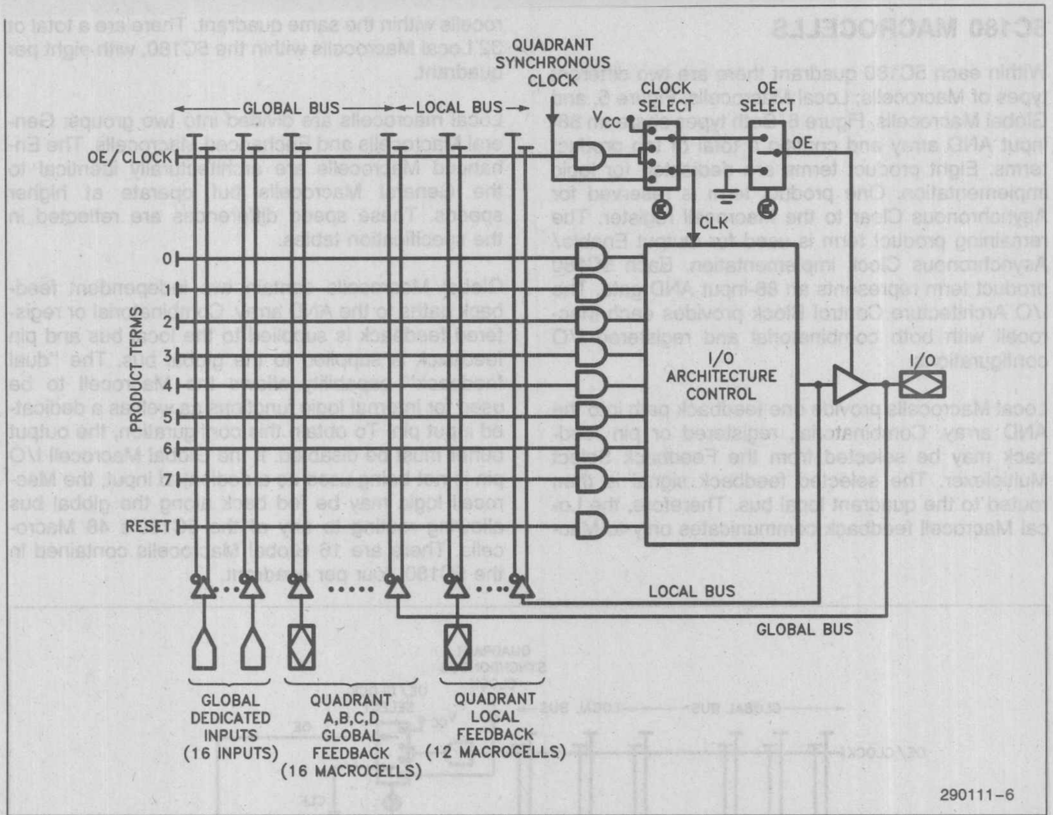


Figure 6. Global Macrocell Logic Array

MACROCELL LOGIC CONFIGURATIONS

Combinatorial Selection

In the Combinatorial configuration, eight product terms are ORed together to generate the output signal. The Invert Select EPROM bit controls output polarity and the Output Enable buffer is product-term controlled. The Feedback Select allows the user to choose combinatorial, I/O (pin) or no feedback to the respective local and global buses.

REGISTER SELECTION

The advanced I/O architecture of the 5C180 allows four different register types along with combinatorial output as illustrated in Figures 8a–8e. The register types include a T, D, JK, or SR Flip-Flop and each Macrocell I/O structure may be independently configured. In addition, all registers have an individual asynchronous RESET control from a dedicated product term derived in the AND array. When this dedicated product term is a logical one, the Macrocell register is immediately cleared to a logical zero independent of the register clock. The RESET function occurs automatically on power-up.

The four different register types shown in Figures 7b–7e are described below:

D- or T-type Flip-Flops

When either a D- or T-type Flip-Flop is configured as part of the I/O structure, all eight of the product terms into the Macrocell are ORed together and fed into the register input.

JK or SR Registers

When either a JK or SR register is configured, the eight product terms are shared among two OR gates (one for the J or S input and the other for the K or R input). The allocation for these product terms for each of the register inputs is optimized by the iPLDS II development software.

Buried Logic Selection

For Global Macrocells, if no output is selected, the logic may be "buried" and the I/O pin can be used as an additional dedicated input. The use of "dual feedback" is accomplished by tri-stating the Output Enable Buffer. Thus, up to 16 additional dedicated inputs may be added without sacrificing the Macrocell internal logic.

In the erased state, the I/O architecture is configured for combinatorial active low output with I/O (pin) feedback.

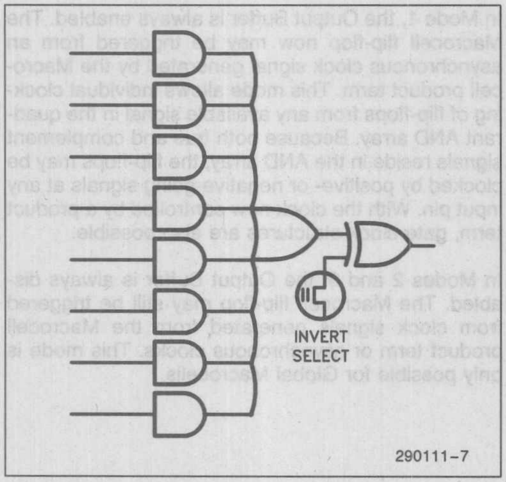


Figure 7a. Combinatorial I/O Configuration

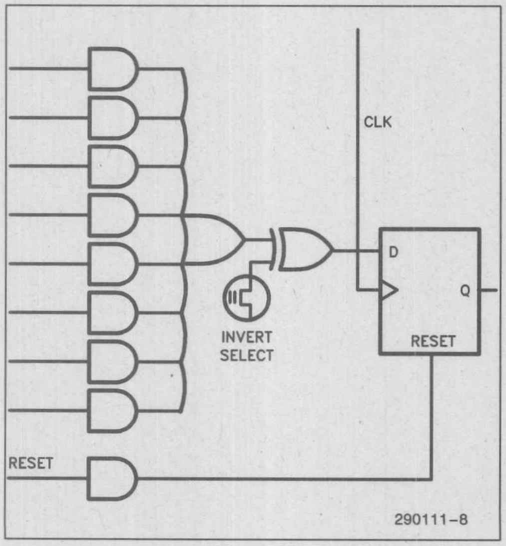


Figure 7b. D-Type Flip-Flop Register Configuration

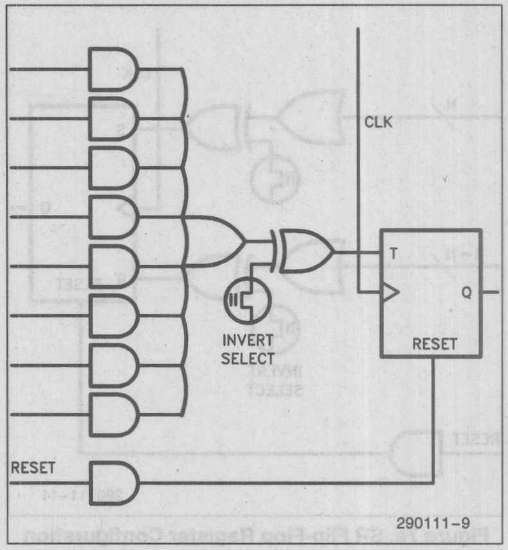


Figure 7c. Toggle (T-Type) Flip-Flop Register Configuration

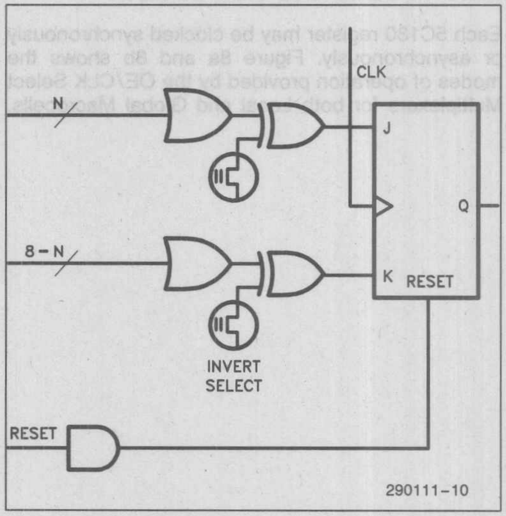


Figure 7d. JK Flip-Flop Register Configuration

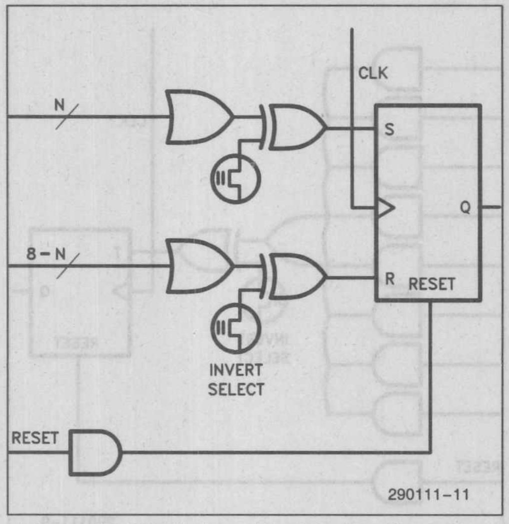


Figure 7e. SR Flip-Flop Register Configuration

MACROCELL OE/CLK SELECT

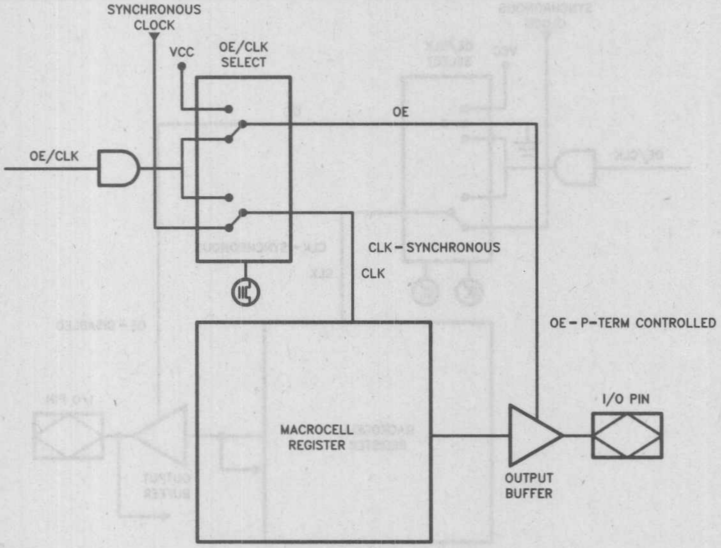
Each 5C180 register may be clocked synchronously or asynchronously. Figure 8a and 8b shows the modes of operation provided by the OE/CLK Select Multiplexers for both Local and Global Macrocells.

The operation of each multiplexer is controlled by EPROM bits and may be individually configured for each 5C180 Macrocell.

In Mode 0, the three-state output buffer is controlled by a single product term. If the output of the AND gate is a logical true then the output buffer is enabled. If a logical false resides on the output of the AND gate then the output buffer is seen as high impedance. In this mode the Macrocell flip-flop may be clocked by its quadrant synchronous clock input. In the erased state, the 5C180 is configured as Mode 0.

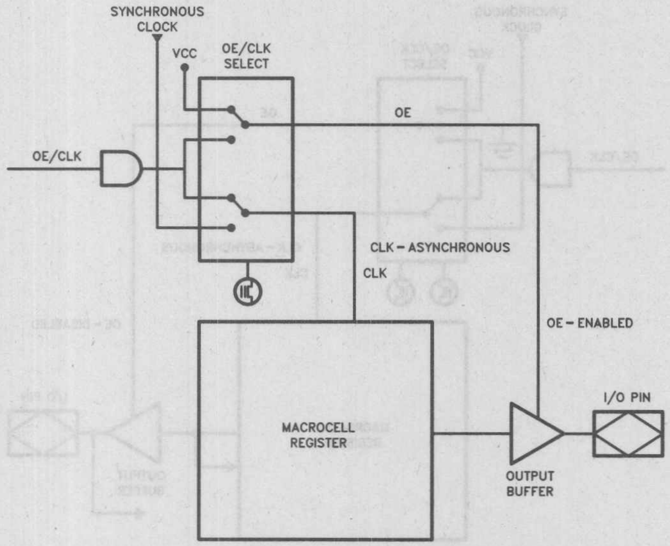
In Mode 1, the Output Buffer is always enabled. The Macrocell flip-flop now may be triggered from an asynchronous clock signal generated by the Macrocell product term. This mode allows individual clocking of flip-flops from any available signal in the quadrant AND array. Because both true and complement signals reside in the AND array, the flip-flops may be clocked by positive- or negative-going signals at any input pin. With the clock now controlled by a product term, gate clock structures are also possible.

In Modes 2 and 3, the Output Buffer is always disabled. The Macrocell flip-flop may still be triggered from clock signals generated from the Macrocell product term or asynchronous clocks. This mode is only possible for Global Macrocells.



290111-12

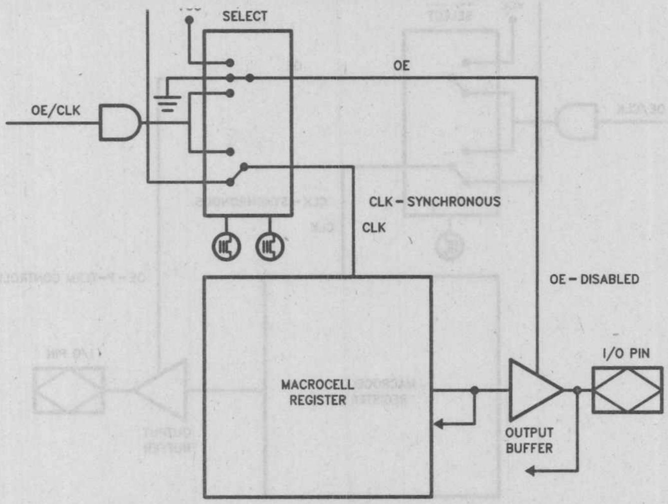
The register is clocked by the quadrant synchronous clock signal which is common to 11 other Macrocells. The output is enabled by the logic from the product term.



290111-13

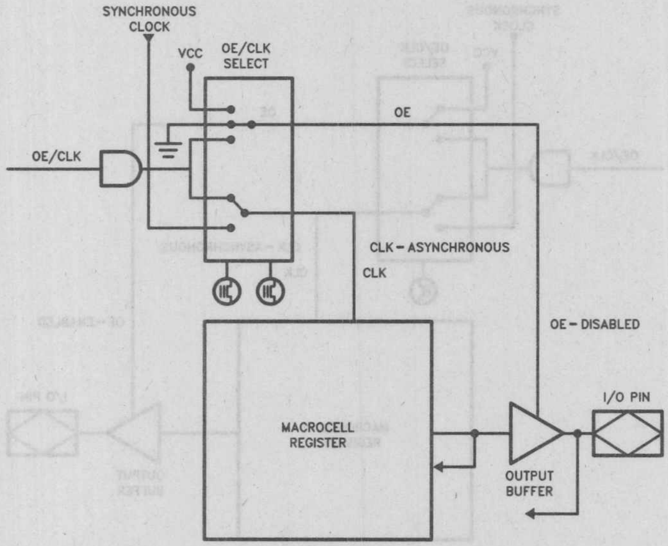
The output is permanently enabled and the register is clocked via the product term. This allows for gated clocks that may be generated from elsewhere in the 5C180.

Figure 8a. Local Macrocell OE/CLK Selection



290111–14

The output is permanently disabled and the register clocked by the quadrant synchronous clock signal. The pin can be used as an input while the register or combinational output can be fed back.



290111–15

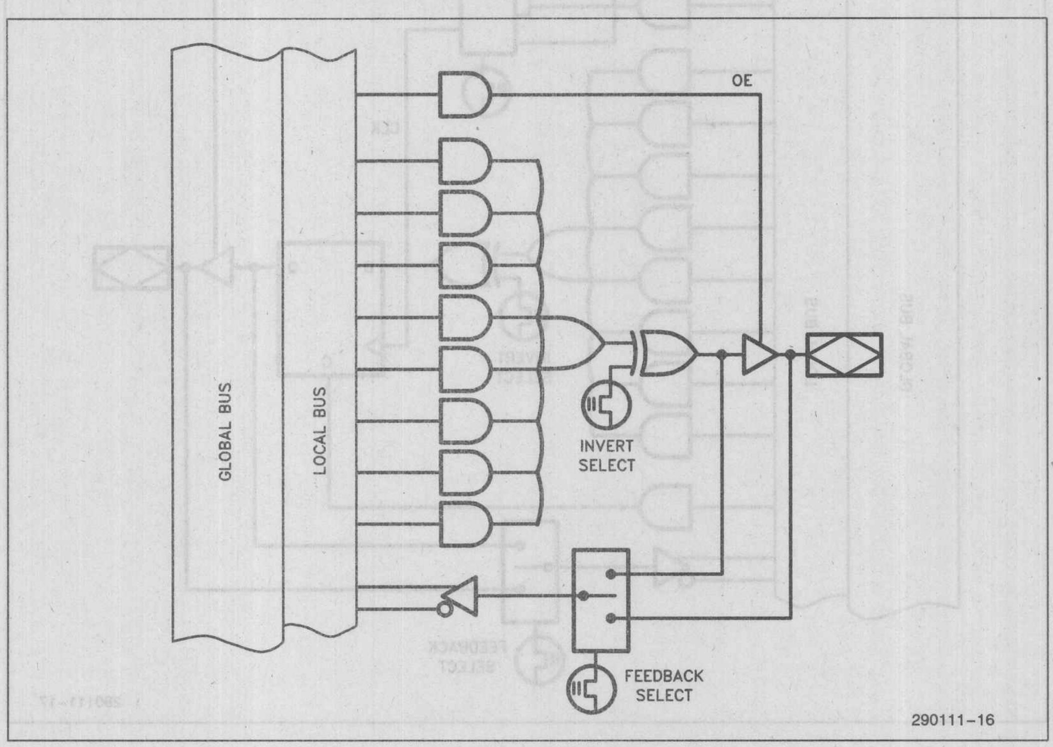
The output is permanently disabled and the register is clocked via the product term. This allows gated clocks that may be generated elsewhere in the 5C180. The pin can be used as in input while the register or combinational output can be fed back.

Figure 8b. Global Macrocell Additional OE/CLK Selection

MACROCELL LOGIC + I/O CONFIGURATIONS

The 5C180 Input/Output Architecture provides each Macrocell with over 50 possible I/O configurations.

Figures 9 and 10 show the 5C180 basic I/O configurations for both the Local and Global Macrocells. Along with combinatorial, four register types are available. Each Macrocell may be independently programmed.

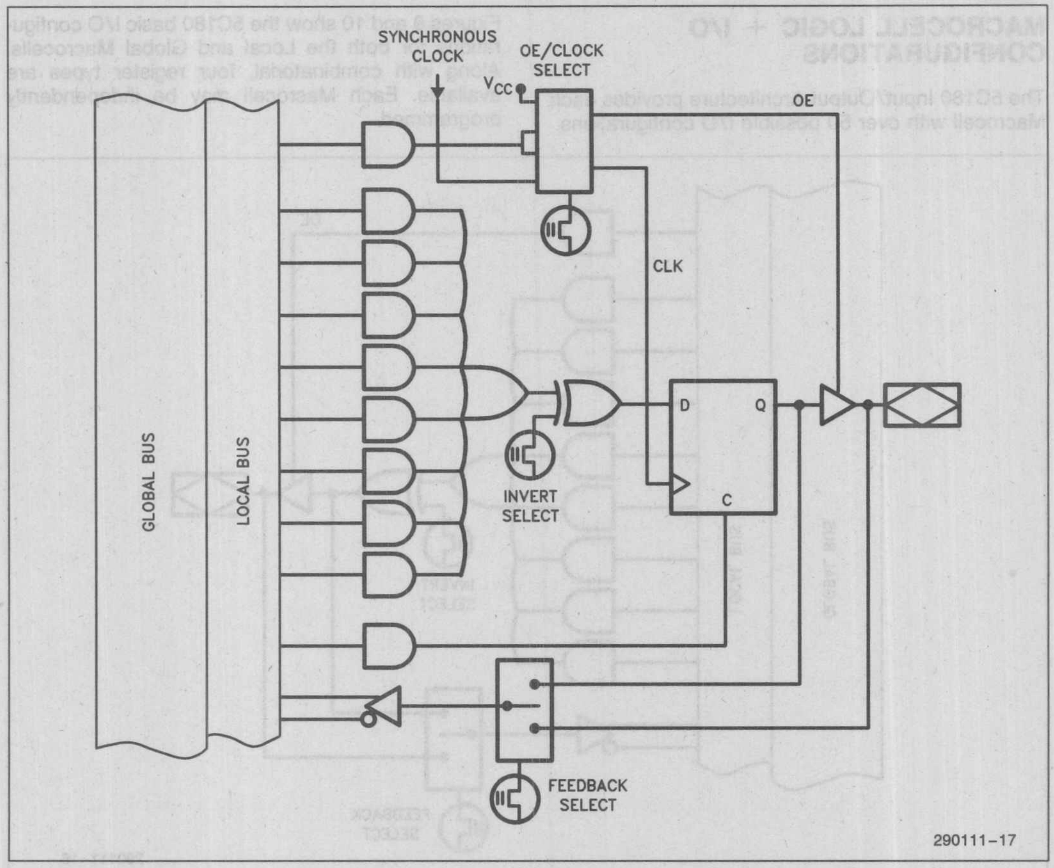


COMBINATORIAL

I/O Selection

Output/Polarity	Feedback	Bus
Combinatorial/High	Comb, Pin, None	Local
Combinatorial/Low	Comb, Pin, None	Local
None	Comb	Local
None	Pin	Local

Figure 9. Local Macrocell I/O Configurations



D-TYPE FLIP-FLOP

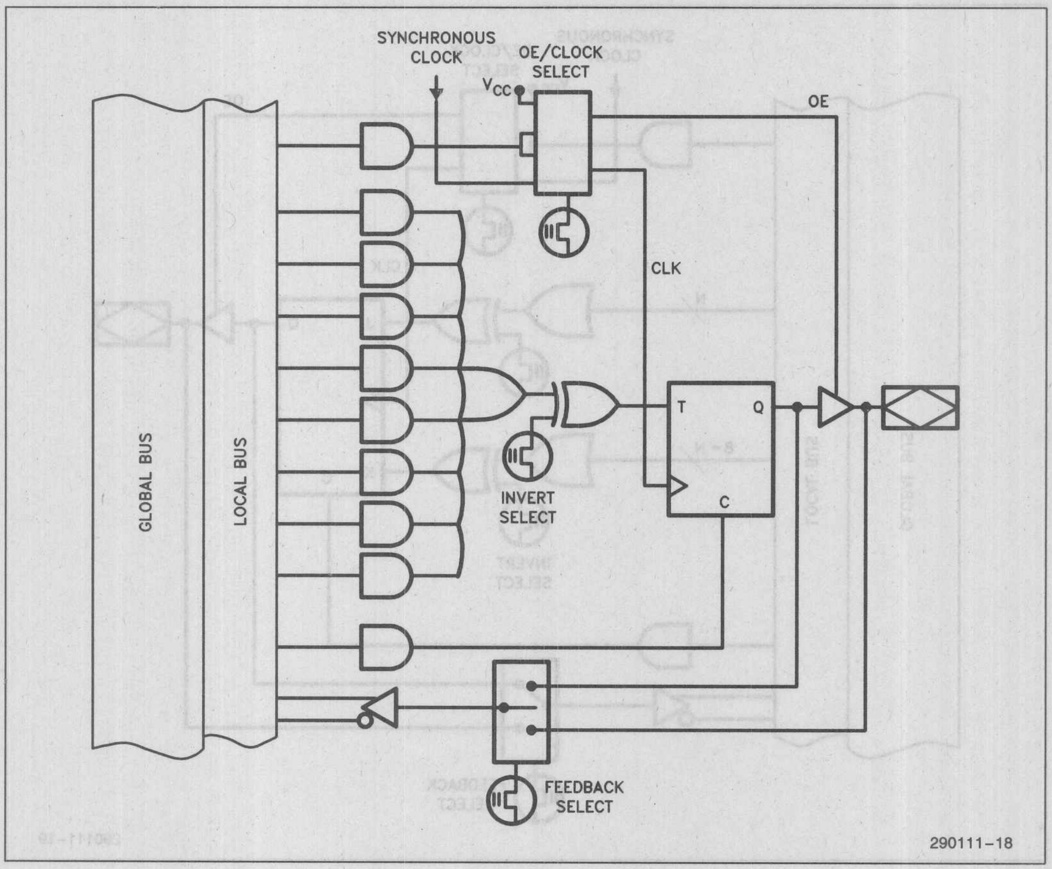
I/O Selection

Output/Polarity	Feedback	Bus
D-Register/High	D-Register, Pin, None	Local
D-Register/Low	D-Register, Pin, None	Local
None	D-Register	Local
None	Pin	Local

Function Table

D	Q_n	Q_{n+1}
0	0	0
0	1	0
1	0	1
1	1	1

Figure 9. Local Macrocell I/O Configurations (Continued)



TOGGLE FLIP-FLOP

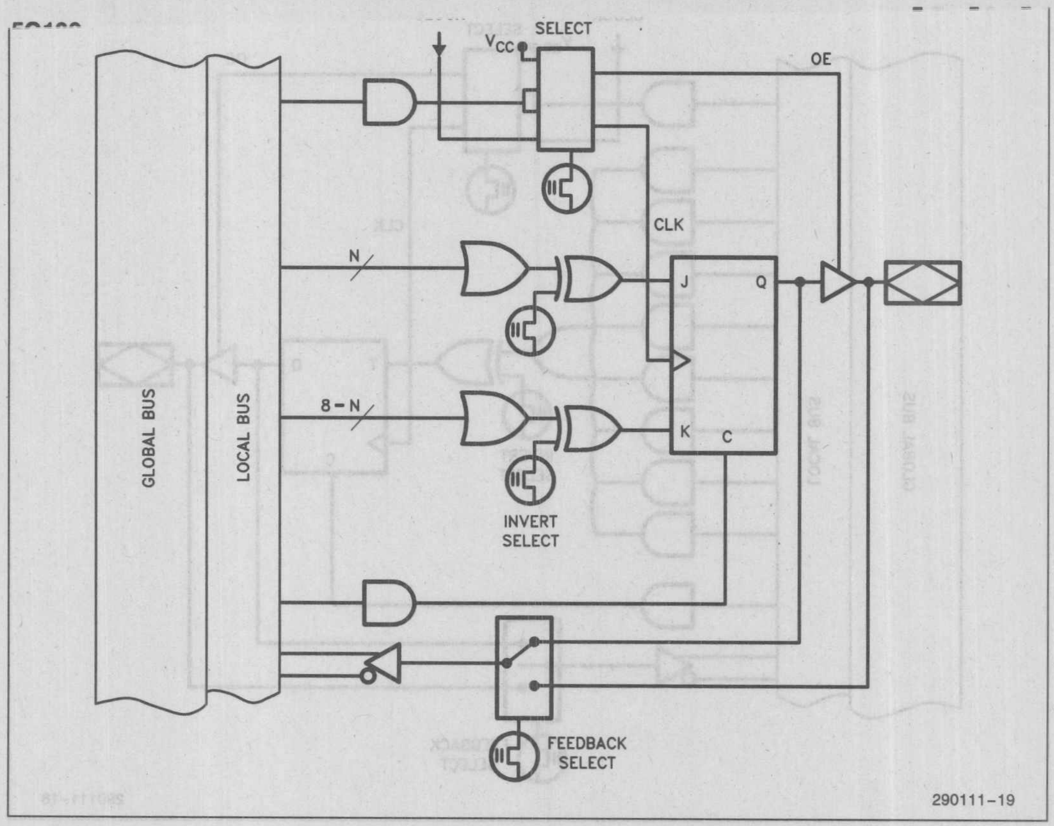
I/O Selection

Output/Polarity	Feedback	Bus
T-Register/High	T-Register, Pin, None	Local
T-Register/Low	T-Register, Pin, None	Local
None	T-Register	Local
None	Pin	Local

Function Table

T	Q_n	Q_{n+1}
0	0	0
0	1	1
1	0	1
1	1	0

Figure 9. Local Macrocell I/O Configurations (Continued)



JK FLIP-FLOP

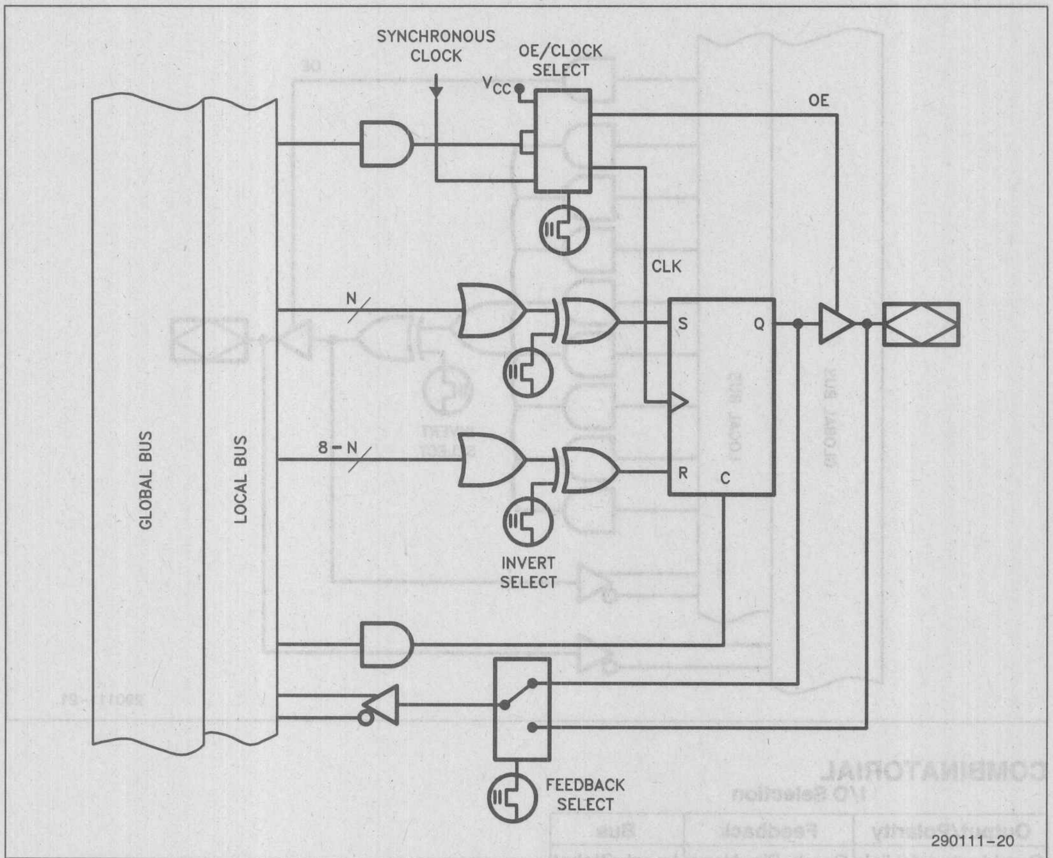
I/O Selection

Output/Polarity	Feedback	Bus
JK Register/High	JK Register, None	Local
JK Register/Low	JK Register, None	Local
None	JK Register	Local

Function Table

J	K	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Figure 9. Local Macrocell I/O Configurations (Continued)



SR FLIP-FLOP

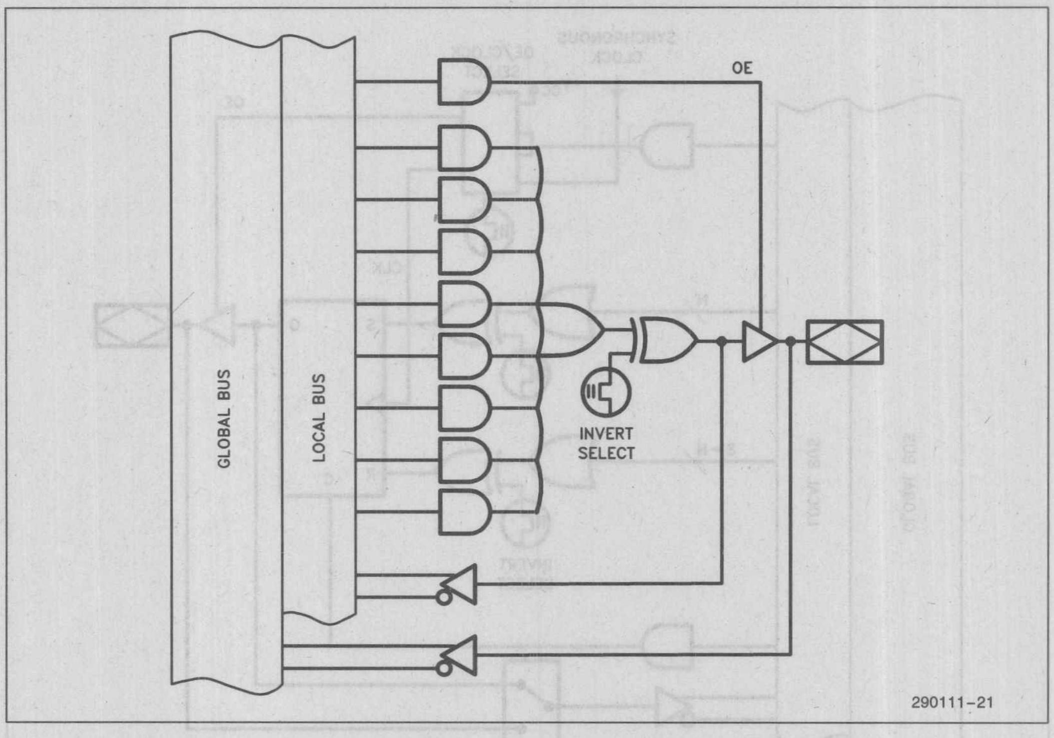
I/O Selection

Output/Polarity	Feedback	Bus
SR Register/High	SR Register, None	Local
SR Register/Low	SR Register, None	Local
None	SR Register	Local

Function Table

S	R	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1

Figure 9. Local Macrocell I/O Configurations (Continued)

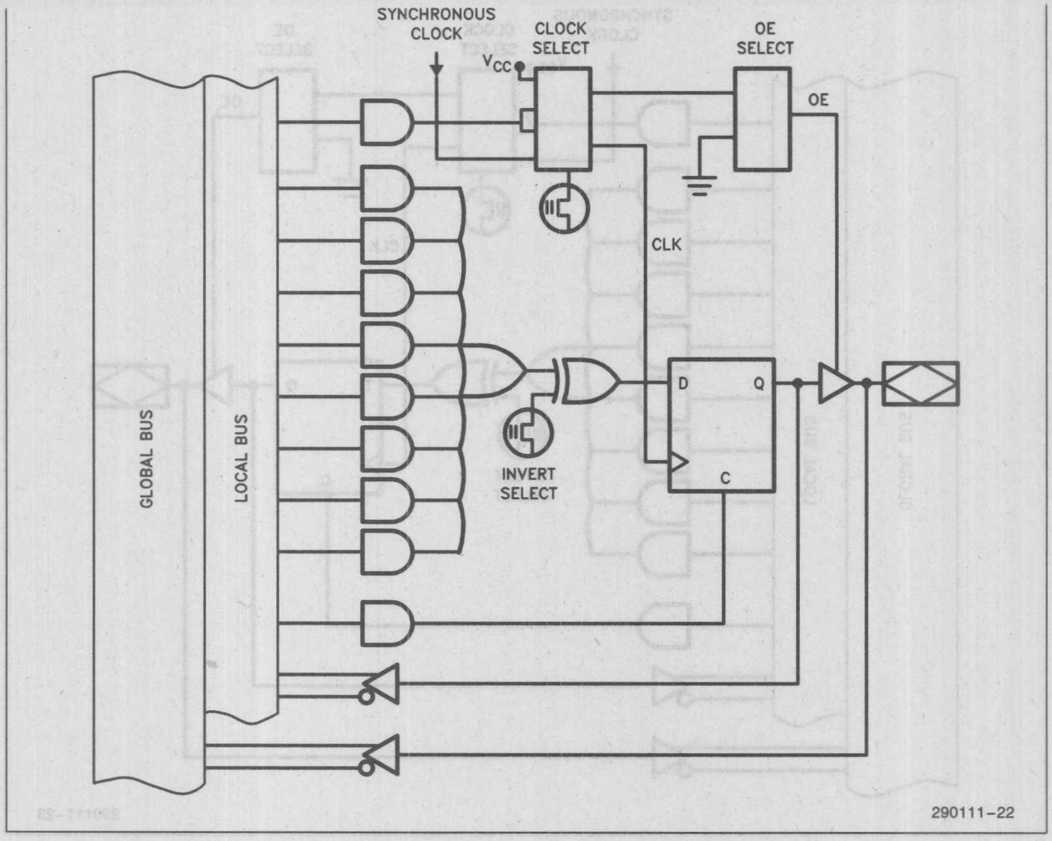


COMBINATORIAL

I/O Selection

Output/Polarity	Feedback	Bus
Combinatorial/High	Comb, Pin, None	Local, Global
Combinatorial/Low	Comb, Pin, None	Local, Global
None	Comb	Local, Global
None	Pin	Global
None	Comb/Pin	Local/Global

Figure 10. Global Macrocell I/O Configurations



D-TYPE FLIP-FLOP

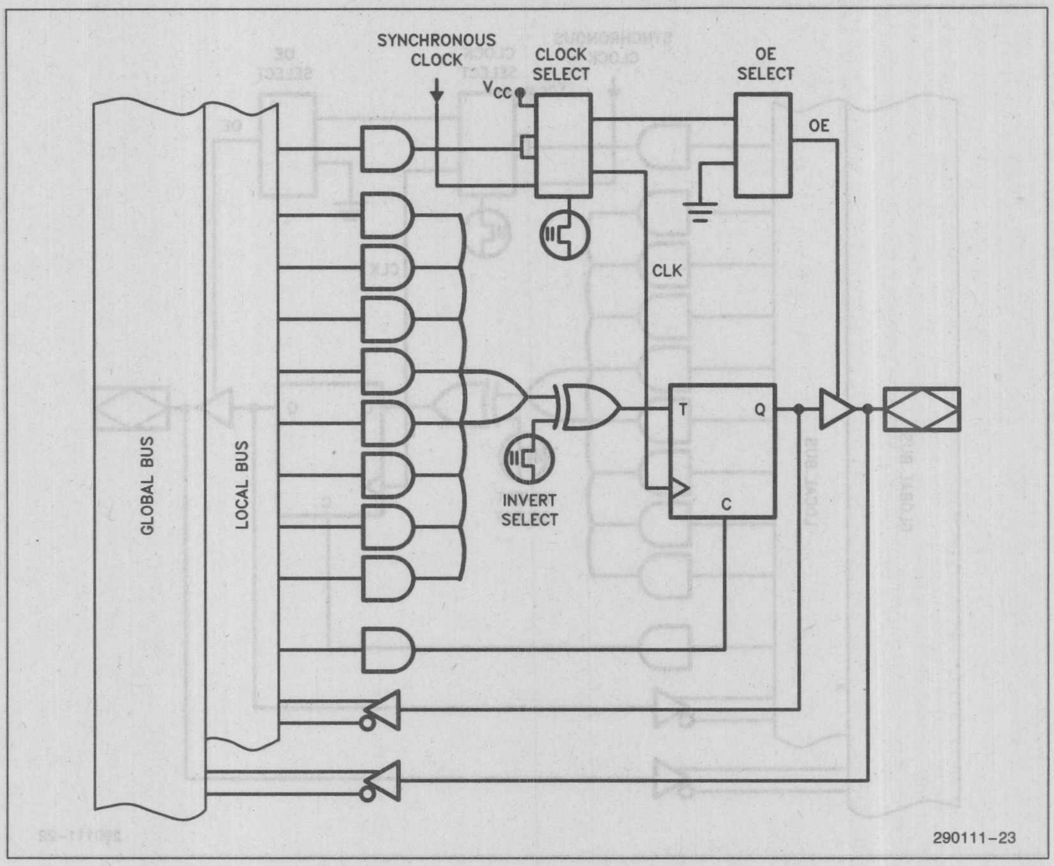
I/O Selection

Output/Polarity	Feedback	Bus
D-Register/High	D-Register, Pin, None	Local, Global
D-Register/Low	D-Register, Pin, None	Local, Global
None	D-Register	Local, Global
None	Pin	Global
None	D-Register/Pin	Local/Global

Function Table

D	Q_n	Q_{n+1}
0	0	0
0	1	0
1	0	1
1	1	1

Figure 10. Global Macrocell I/O Configurations (Continued)



TOGGLE FLIP-FLOP

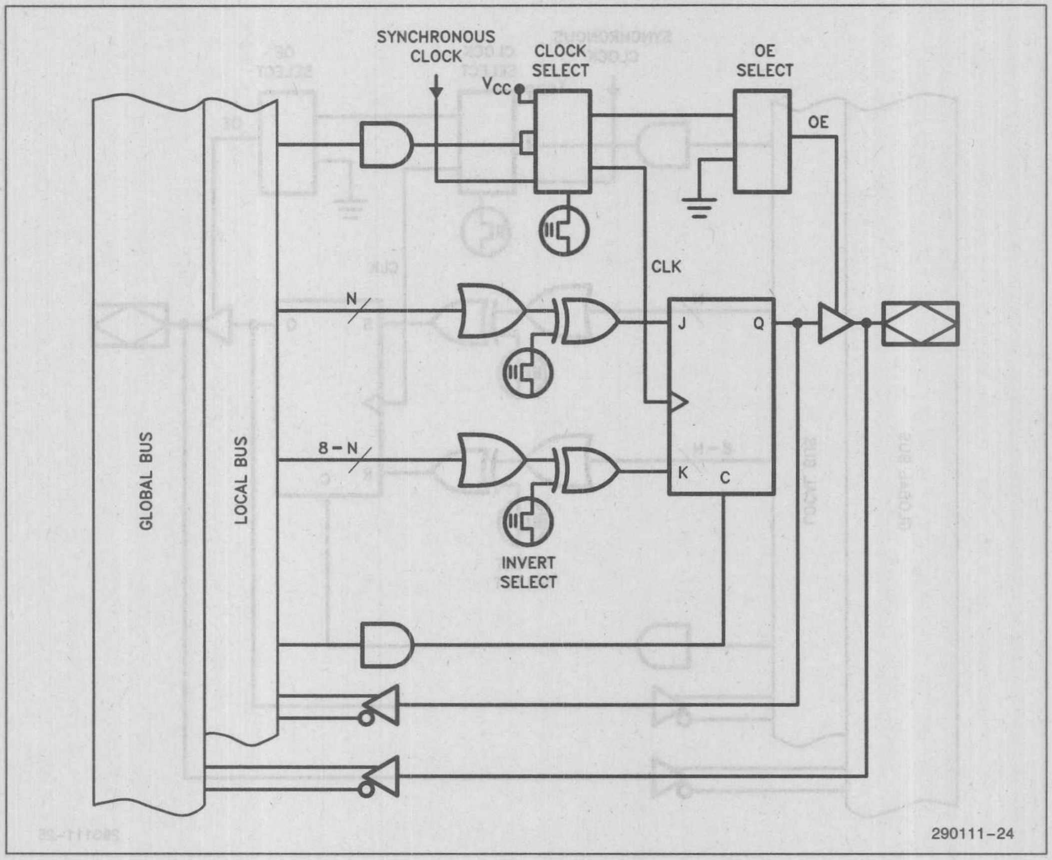
I/O Selection

Output/Polarity	Feedback	Bus
T-Register/High	T-Register, Pin, None	Local, Global
T-Register/Low	T-Register, Pin, None	Local, Global
None	T-Register	Local, Global
None	Pin	Global
None	T-Register/Pin	Local/Global

Function Table

T	Q_n	Q_{n+1}
0	0	0
0	1	1
1	0	1
1	1	0

Figure 10. Global Macrocell I/O Configurations (Continued)



JK FLIP-FLOP

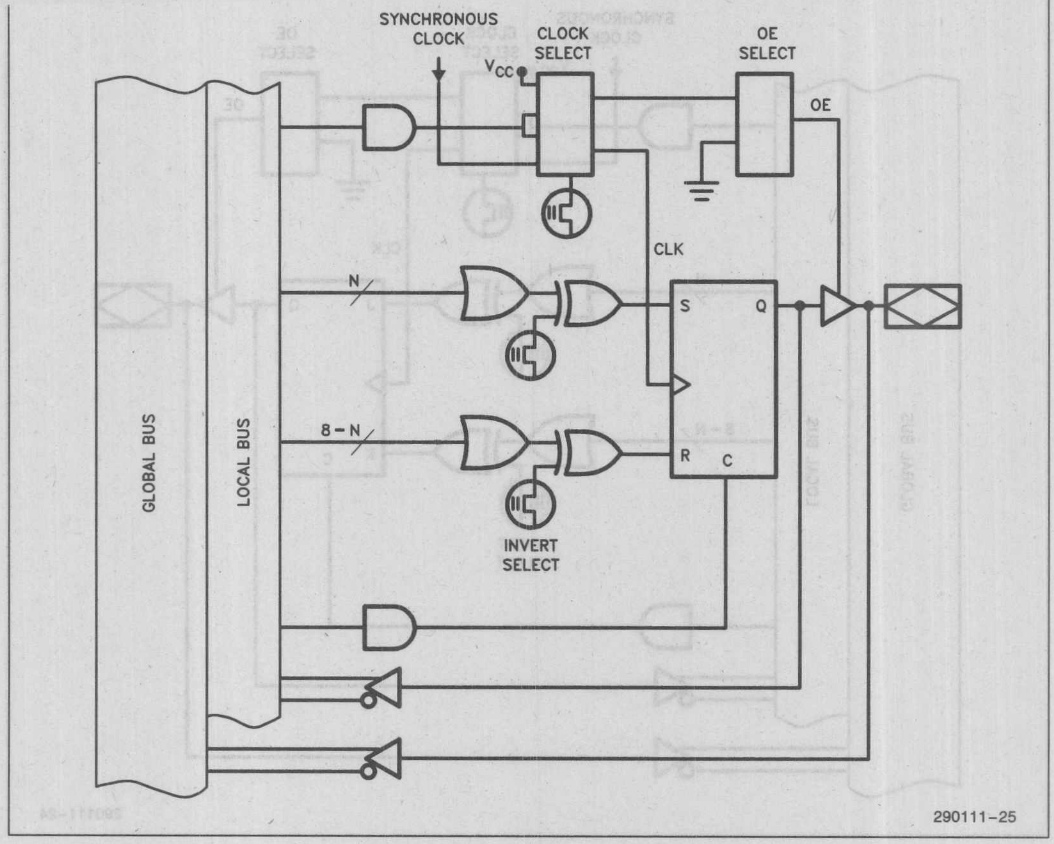
I/O Selection

Output/Polarity	Feedback	Bus
JK Register/High	JK Register, None	Local, Global
JK Register/Low	JK Register, None	Local, Global
None	JK Register	Local
None	JK Register/Pin	Local/Global

Function Table

J	K	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Figure 10. Global Macrocell I/O Configurations (Continued)



SR FLIP-FLOP

I/O Selection

Output/Polarity	Feedback	Bus
SR Register/High	SR Register, None	Local, Global
SR Register/Low	SR Register, None	Local, Global
None	SR Register	Local
None	SR Register/Pin	Local/Global

Function Table

S	R	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1

Figure 10. Global Macrocell I/O Configurations (Continued)

AUTOMATIC STAND-BY MODE

The 5C180 contains a programmable bit, the Turbo Bit, that optimizes operation for speed or for power savings. When the Turbo Bit is programmed (TURBO = ON), the device is optimized for maximum speed. When the Turbo Bit is not programmed (TURBO = OFF), the device is optimized for power savings by entering standby mode during periods of inactivity.

Figure 11 shows the device entering standby mode approximately 100 ns after the last input transition. When the next input transition is detected, the device returns to active mode. Wakeup time adds an additional 30 ns to the propagation delay through the device as measured from the first input. No delay will occur if an output is dependent on more than one input and the last of the inputs changes after the device has returned to active mode.

After erasure, the Turbo Bit is unprogrammed (OFF); automatic standby mode is enabled. When the Turbo Bit is programmed (ON), the device never enters standby mode.

Erased-State Configuration

Prior to programming, the I/O structure is configured for combinatorial active low output with input (pin) feedback.

PROGRAMMING CHARACTERISTICS

Initially, all the EPROM control bits of the 5C180 are connected. Each of the connected control bits are selectively disconnected by programming the EPROM cells into their "on" state. Programming voltage and waveform specifications are available by request from Intel to support programming of the 5C180.

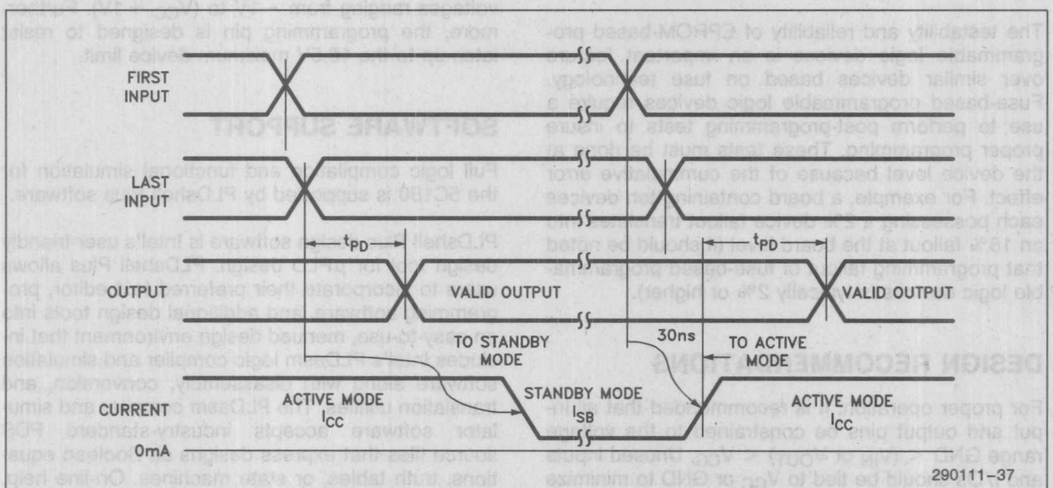


Figure 11. 5C180 Standby and Active Mode Transitions

Intelligent Programming Algorithm

The 5C180 supports the Intelligent Programming Algorithm which rapidly programs Intel PLDs using an efficient and reliable method. The Intelligent Programming Algorithm is particularly suited to the production programming environment. This method ensures reliability as the incremental program margin of each bit is continually monitored to determine when the bit has been successfully programmed.

FUNCTIONAL TESTING

Since the logical operation of the 5C180 is controlled by EPROM elements, the device is completely testable. Each programmable EPROM bit controlling the internal logic is tested using application-independent test program patterns. After testing, the devices are erased before shipment to customers. No post-programming tests of the EPROM array are required.

The testability and reliability of EPROM-based programmable logic devices is an important feature over similar devices based on fuse technology. Fuse-based programmable logic devices require a use to perform post-programming tests to insure proper programming. These tests must be done at the device level because of the cummulative error effect. For example, a board containing ten devices each possessing a 2% device fallout translates into an 18% fallout at the board level (it should be noted that programming fallout of fuse-based programmable logic devices is typically 2% or higher).

DESIGN RECOMMENDATIONS

For proper operation, it is recommended that all input and output pins be constrained to the voltage range GND < (V_{IN} or V_{OUT}) < V_{CC}. Unused inputs and I/Os should be tied to V_{CC} or GND to minimize device power consumption. Reserved pins (as indicated in the logic compiler REPORT file) should be left floating (no connect) so that the pin can attain the appropriate logic level. A power supply decoupling capacitor of at least 0.2 μf must be connected directly between V_{CC} and GND.

As with all CMOS devices, ESD handling procedures should be used with this device to prevent damage during programming, assembly, and test.

DESIGN SECURITY

A single EPROM bit provides a programmable design security feature that controls the access to the data programmed into the device. If this bit is set, a proprietary design within the device cannot be copied. This EPROM security bit enables a higher degree of design security than fused-based devices since programmed data within EPROM cells is invisible even to microscopic evaluation. The EPROM security bit, along with all the other EPROM control bits, will be reset by erasing the device.

LATCH-UP IMMUNITY

All of the input, I/O, and clock pins of the 5C180 have been designed to resist latch-up which is inherent in inferior CMOS structures. The 5C180 is designed with Intel's proprietary CMOS II-E EPROM process. Thus, each of the 5C180 pins will not experience latch-up with currents up to ± 100 mA and voltages ranging from -1V to (V_{CC} $+1$V). Furthermore, the programming pin is designed to resist latch-up to the 13.5V maximum device limit.

SOFTWARE SUPPORT

Full logic compilation and functional simulation for the 5C180 is supported by PLDshell Plus software.

PLDshell Plus design software is Intel's user-friendly design tool for μPLD design. PLDshell Plus allows users to incorporate their preferred text editor, programming software, and additional design tools into an easy-to-use, menued design environment that includes Intel's PLDasm logic compiler and simulation software along with disassembly, conversion, and translation utilities. The PLDasm compiler and simulator software accepts industry-standard PDS source files that express designs as Boolean equations, truth tables, or state machines. On-line help, datasheet briefs, technical notes, and error message information, along with waveform viewing/printing capability make the design task as easy as possible. PLDshell Plus software is available from Intel Literature channels or from your local Intel sales representative.

Tools that support schematic capture and timing simulation for the 5C180 are available. Please refer to the "Development Tools" section of the Programmable Logic handbook.

The 5C180 is also supported by third-party logic compilers such as ABEL*, CUPL*, PLDesigner*, Log/IC, etc. Programming support is provided by third-party programmer companies such as Data I/O, Logic Devices, STAG, etc. Please refer to the "Third-Party Support" lists in the *Programmable Logic* handbook for complete information and vendor contacts.

ORDERING INFORMATION

t_{PD} (ns)	t_{CO} (ns)	f_{MAX} (MHz)	Order Code	Package	Operating Range
70	29	20.8	N5C180-70	PLCC	Commercial
75	30	19.6	N5C180-75	PLCC	Commercial
90	35	16.1	N5C180-90	PLCC	Commercial
75	30	19.6	TN5C180-75	PLCC	Industrial

*ABEL is a trademark of Data I/O Corp. CUPL is a trademark of Logical Devices, Inc. PLDesigner is a trademark of MINC, Inc. Log/IC is a trademark of ISDATA, Inc.

ABSOLUTE MAXIMUM RATINGS*

Symbol	Parameter	Min	Max	Units
V_{CC}	Supply Voltage(1)	−2.0	7.0	V
V_{PP}	Programming Supply Voltage(1)	−2.0	13.5	V
V_I	DC Input Voltage(1)(2)	−0.5	$V_{CC}+0.5$	V
t_{stg}	Storage Temperature	−65	+150	°C
t_{amb}	Ambient Temperature(3)	−10	+85	°C

NOTES:
1. Voltages with respect to ground.
2. Minimum DC input is −0.5V. During transitions, the inputs may undershoot to −2.0V or overshoot to +7.0V for periods less than 20 ns under no load conditions.
3. Under bias. Extended temperature versions are also available.

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Units
V_{CC}	Supply Voltage	4.75	5.25	V
V_{IN}	Input Voltage	0	V_{CC}	V
V_O	Output Voltage	0	V_{CC}	V
T_A	Operating Temperature	0	+70	°C
t_R(4)	Input Rise Time		500	ns
t_F(4)	Input Fall Time		500	ns

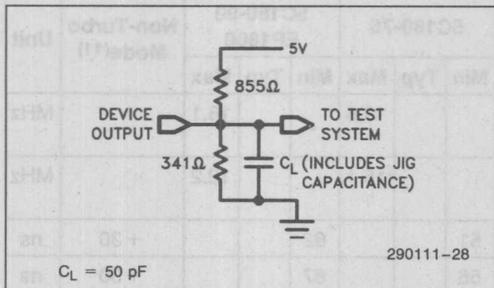
NOTE:
4. t_R and t_F for clocks is 250 ns.

D.C. CHARACTERISTICS $T_A = 0°$ to $+70°C$, $V_{CC} = 5V \pm 5\%$

Symbol	Parameter/Test Conditions	Min	Typ	Max	Unit
V_{IH}(5)	High Level Input Voltage	2.0		$V_{CC} + 0.3$	V
V_{IL}(5)	Low Level Input Voltage	−0.3		0.8	V
V_{OH}(6)	High Level Output Voltage $I_O = -4.0$ mA D.C., V_{CC} = min.	2.4			V
V_{OL}	Low Level Output Voltage $I_O = 4.0$ mA D.C., V_{CC} = min.			0.45	V
I_I	Input Leakage Current V_{CC} = max., GND $< V_{IN} < V_{CC}$			±10	μA
I_{OZ}	Output Leakage Current V_{CC} = max., GND $< V_{OUT} < V_{CC}$			±10	μA
I_{SC}(7)	Output Short Circuit Current V_{CC} = max., $V_{OUT} = 0.5V$		20	30	mA
I_{SB}(8)	Standby Current V_{CC} = max., $V_{IN} = V_{CC}$ or GND, Standby mode		35	150	μA
I_{CC}	Power Supply Current V_{CC} = max., $V_{IN} = V_{CC}$ or GND, No load, Input Freq. = 1 MHz Active mode (Turbo = Off), Device prog. as four 12-bit Ctrs.		30	45	mA

NOTES:
5. Absolute values with respect to device GND; all over and undershoots due to system or tester noise are included.
6. I_O at CMOS levels (3.84 V) = −2 mA
7. Not more than 1 output should be tested at a time. Duration of that test must not exceed 1 second.
8. With Turbo Bit Off, device automatically enters standby mode approximately 100 ns after last input transition.

A.C. TESTING LOAD CIRCUIT



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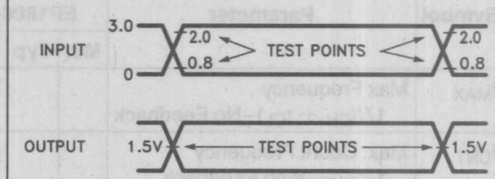
A.C. TESTING INPUT, OUTPUT WAVEFORM



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A.C. Testing: Inputs are Driven at 3.0V for a Logic "1" and 0V for a Logic "0". Timing Measurements are made at 2.0V for a Logic "1" and 0.8V for a Logic "0" on inputs. Outputs are measured at a 1.5V point. Device rise and fall times <6 ns.

CAPACITANCE

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
C_{IN}	Input Capacitance			15	pF	$V_{IN} = 0V, f = 1.0$ MHz
C_{OUT}	Output Capacitance			15	pF	$V_{OUT} = 0V, f = 1.0$ MHz
C_{CLK}	Clock Pin Capacitance			25	pF	$V_{OUT} = 0V, f = 1.0$ MHz
C_{VPP}	V_{PP} Pin Capacitance			160	pF	CLK2, $V_{OUT} = 0V, f = 1.0$ MHz

A.C. CHARACTERISTICS $T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 5\%$, Turbo Bit On(9)

Symbol	From	To	5C180-70 EP1800-2			5C180-75			5C180-90 EP1800			Non-Turbo Mode(11)	Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
t_{PD1}	Input(12)	Comb. Output			65			70			85	+30	ns
t_{PD2}	I/O(12)	Comb. Output			70			75			90	+30	ns
t_{PD2e}	I/O(13)	Comb. Output			65			70			85	+30	ns
t_{PZX}(10)	I or I/O	Output Enable			70			75			90	+30	ns
t_{PXZ}(10)	I or I/O	Output Disable			70			75			90	+30	ns
t_{CLR}	Asynch. Reset	Q Reset			70			75			90	+30	ns

NOTES:

9. Typ. Values are at $T_A = 25°C$, $V_{CC} = 5V$, Active Mode.
10. t_{PZX} and t_{PXZ} are measured at $\pm 0.5V$ from steady state voltage as driven by spec. output load. t_{PXZ} is measured with $C_L = 5$ pF.
11. If device is operated with Turbo Bit Off (Non-Turbo Mode) and the device has been inactive for approx. 100 ns, increase time by amount shown.

SYNCHRONOUS CLOCK MODE A.C. CHARACTERISTICS

$T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 5\%$, Turbo Bit On(9)

Symbol	Parameter	5C180-70 EP1800-2			5C180-75			5C180-90 EP1800			Non-Turbo Mode(11)	Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
f_{MAX}	Max Frequency $1/(t_{CH} + t_{CL})$–No Feedback			20.8			19.6			16.1		MHz
f_{CNT}	Max. Count Frequency $1/t_{CNT}$–With Feedback			16.1			15.1			12.2		MHz
t_{SU1}	Input Setup Time to Clk(12)	48			51			62			+30	ns
t_{SU2}	I/O Setup Time to Clk(12)	53			56			67			+30	ns
t_{SU2e}	I/O Setup Time to Clk(13)	48			51			62			+30	ns
t_H	I or I/O Hold after Clk High	0			0			0				ns
t_{CO}	Clk High to Output Valid			29			30			35		ns
t_{CNT}	Register Output Feedback to Register Input–Internal Path	62			66			82			+30	ns
t_{CH}	Clk High Time	24			25			30				ns
t_{CL}	Clk Low Time	24			25			30				ns

ASYNCHRONOUS CLOCK MODE A.C. CHARACTERISTICS

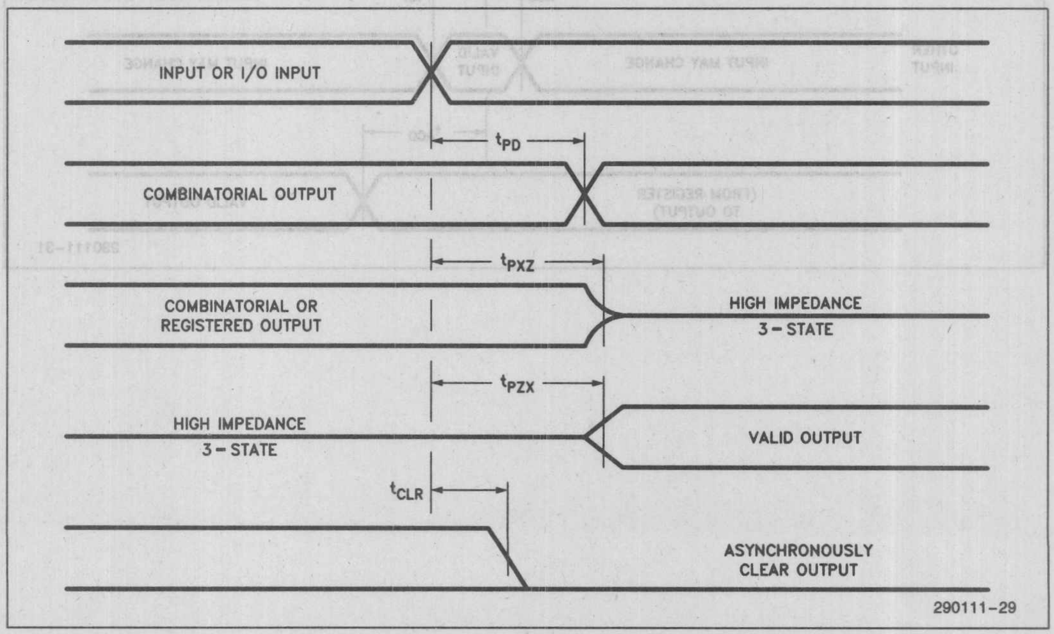
T_A = 0°C to +70°C, V_{CC} = 5V ±5%, Turbo Bit On(9)

Symbol	Parameter	5C180-70 EP1800-2			5C180-75			5C180-90 EP1800			Non-Turbo Mode(11)	Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
f_{AMAX}	Max. Frequency 1/(t_{ACH} + t_{ACL})–No Feedback			20.8			20			16.6		MHz
f_{ACNT}	Max. Frequency 1/t_{ACNT}–With Feedback			16.1			15.1			12.2		MHz
t_{ASU1}	Input Setup Time to Asynch. Clock(12)	17			19			23			+30	ns
t_{ASU2}	I/O Setup Time to Asynch. Clock(12)	22			25			28			+30	ns
t_{AH}	Input or I/O Hold to Asynch. Clock	30			30			30				ns
t_{ACO}	Asynch. Clk to Output Valid			70			75			90		ns
t_{ACNT}	Register Output Feedback to Register Input–Internal Path	62			66			82			+30	ns
t_{ACH}	Asynch. Clk High Time	24			25			30				ns
t_{ACL}	Asynch. Clk Low Time	24			25			30				ns

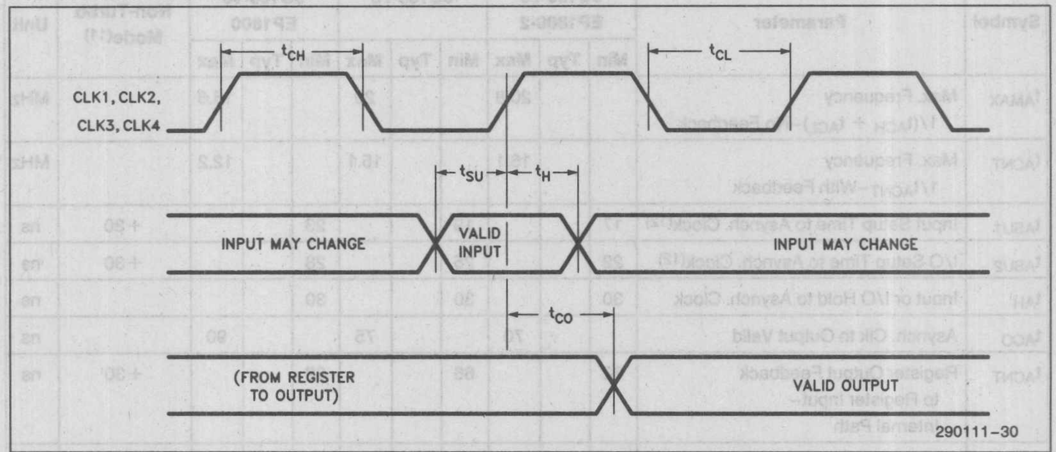
NOTES:
12. For General and Global Macrocells.
13. For Enhanced Macrocells.

SWITCHING WAVEFORMS

COMBINATORIAL MODE



SYNCHRONOUS CLOCK MODE



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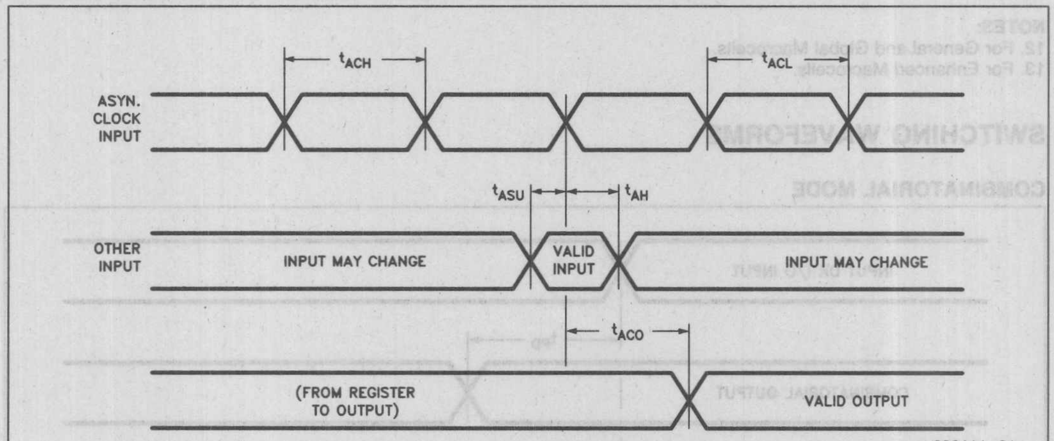
ASYNCHRONOUS CLOCK MODE



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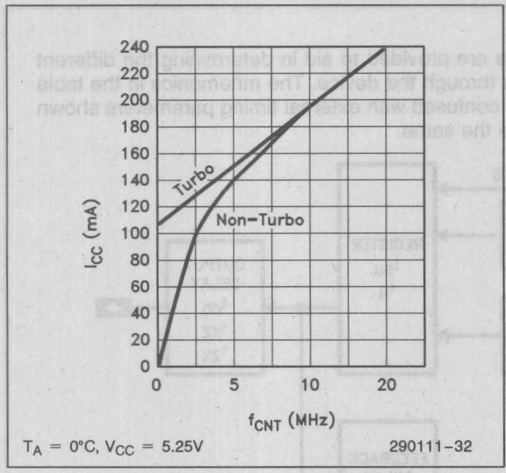
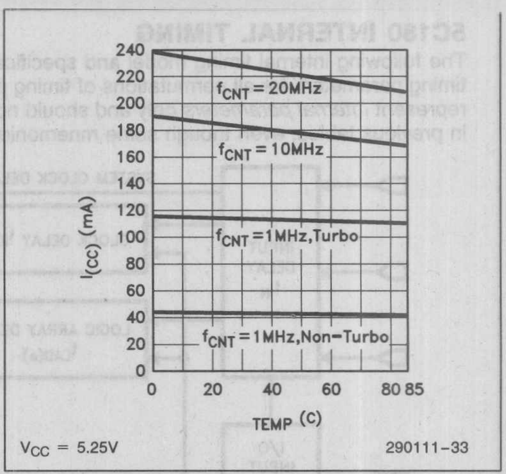
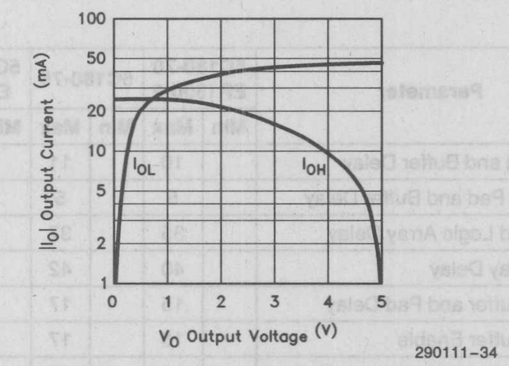


Current in Relation to Frequency



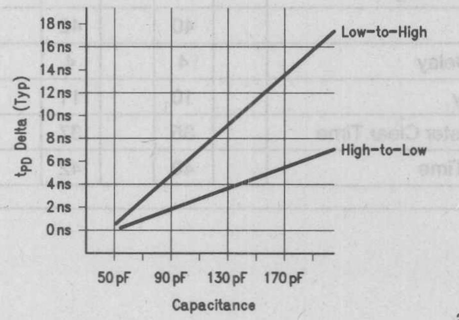
Current in Relation to Temperature



Output Drive Current in Relation to Voltage

5C180

t_{PD} Derating vs Capacitive Loading



Conditions:
T_A = 25°C
V_{CC} = 5.0V

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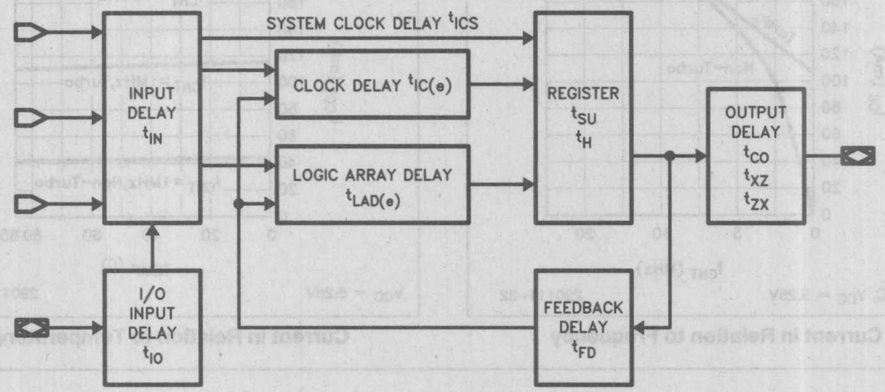
2

5C180 INTERNAL TIMING

The following internal timing model and specifications are provided to aid in determining the different timing parameters for all permutations of timing paths through the device. The mnemonics in the table represent *internal parameters* only and should not be confused with external timing parameters shown in previous tables, even though some mnemonics are the same.



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Symbol	Parameter	5C180-70 EP1800-2		5C180-75		5C180-90 EP1800		Non-Turbo Mode(11)		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{IN}	Input Pad and Buffer Delay		10		11		14		0	ns
t_{IO}	I/O Input Pad and Buffer Delay		5		5		5		0	ns
t_{LADe}	Enhanced Logic Array Delay		35		37		43		30	ns
t_{LAD}	Logic Array Delay		40		42		48		30	ns
t_{OD}	Output Buffer and Pad Delay		15		17		23		0	ns
t_{ZX}	Output Buffer Enable		15		17		23		0	ns
t_{XZ}	Output Buffer Disable		15		17		23		0	ns
t_{SU}	Register Setup Time	12		13		18		0		ns
t_{HS}	Register Hold Time (System Clock)	0		0		0		0		ns
t_H	Register Hold Time	30		30		30		0		ns
t_{ICe}	Enhanced Clock Delay		35		37		43		30	ns
t_{IC}	Clock Delay		40		42		48		30	ns
t_{ICS}	System Clock Delay		4		4		4		0	ns
t_{FD}	Feedback Delay		10		11		16		−30	ns
t_{CLRe}	Enhanced Register Clear Time		35		37		43		30	ns
t_{CLR}	Register Clear Time		40		42		48		30	ns

Applications Information 3

3

Using the iFX780 FLEXlogic FPGA in Hybrid 3.3V/5V Systems

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PROGRAMMABLE LOGIC DEVICES

September 1993

Order Number: 292107-001

Using the iFX780 FLEXlogic FPGA in Hybrid 3.3V/5V Systems

CONTENTS PAGE

1.0 INTRODUCTION

The move from 5V to 3.3V supply voltages in the electronics industry is well under way. The requirements of low-power computers and shrinking process geometries have finally spurred semiconductor manufacturers to qualify many 5V component designs for 3.3V operation, as well as to design components for 3.3V operation from the start. While the laptop/notebook market, as well as other battery-operated markets, will make a complete change to 3.3V-only operation as quickly as component manufacturers will allow, other markets will not move nearly as fast. Many other electronic products will be hybrid 5V/3.3V products for some time.

Hybrid 5V/3.3V systems raise design issues that 5V-only or 3.3V-only systems do not. In addition to routing/switching of two power sources, designers must consider the effects components with different drive levels have on one another when they are connected together. This application brief summarizes the issues with respect to drive levels from 5V and 3.3V components in hybrid systems, and shows how the multi-voltage drive capability of Intel's iFX780 FLEXlogic FPGA device greatly simplifies the design of hybrid systems, while integrating a large number of PLDs or discrete logic devices into a single package.

A brief iFX780 product overview sets the context for the discussion.

2.0 PRODUCT OVERVIEW AND I/O SUMMARY

The iFX780 is the first member of Intel's FLEXlogic family of FPGA-class devices. The iFX780 is an 80 macrocell device that offers a fast, deterministic 10 ns t_{PD} from any input or I/O to any other I/O. It can operate in-system at speeds up to 80 MHz. Figure 1 shows a block diagram of the iFX780 device in the 132-pin package. The device is grouped into eight Configurable Function Blocks (CFBs); each CFB can be independently configured as a 24V10-type PLD or as a 128 deep x 10-bit-wide bank of SRAM. This application brief does not discuss the advanced CFB and macrocell features of the device. For additional information on the architecture and features of the device, refer to the iFX780 FPGA data sheet (literature order no: 290459) and other iFX780 application briefs.

Of special note for hybrid systems is that fact that each CFB has its own output reference pin (V_{CCO}) independent of the V_{CC} pins. This allows the 10 output buffers for each CFB to swing from 0V–3.3V or 0V–5V by tying its respective V_{CCO} pin to a 3.3V or 5V source. Outputs of a CFB can even start out in product life as 5V outputs to drive 5V devices and be shifted to 3.3V outputs when 3.3V devices are available via a manufacturing jumper on the V_{CCO} pin. Dynamic shifting of output levels is also possible via a voltage switch on the V_{CCO} pin. The core of the iFX780 (everything but the output buffers) requires 5V to operate. (Note that the 84-pin package has six V_{CCO} pins rather than eight; two pairs of CFBs share a V_{CCO} pin.)

Design tools allow outputs with like voltages to be assigned to the same CFBs, via a keyword in the source file, such as "5VOLT" or "3VOLT" (the exact keyword and syntax will vary depending on the tool used). Note that while keywords allow design tools to group signals together, the actual voltage level of CFB outputs is dependent on the V_{CCO} pin.

An open-drain option for all outputs is available and is also supported by a source file keyword, such as "OPEN_DRAIN". The open-drain option is supported on an output-by-output basis and is configured during programming, but can be changed via in-circuit reconfiguration.

3

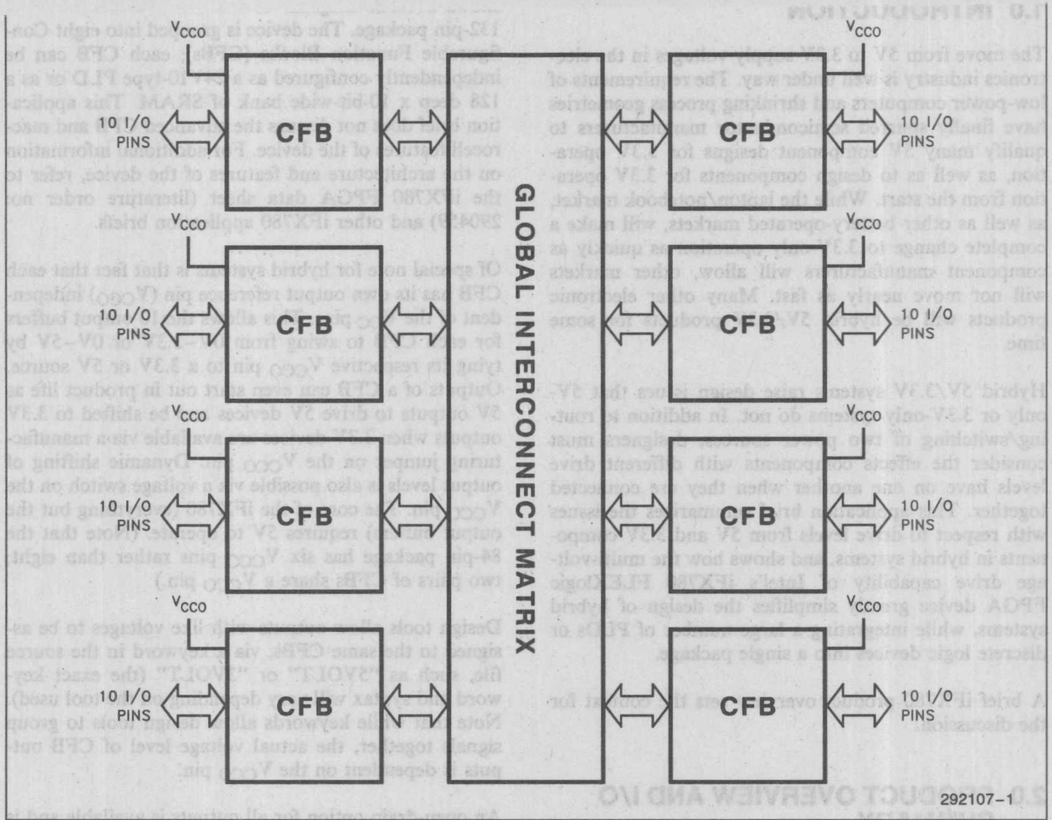


Figure 1. iFX780 Block Diagram Showing V_{CCO} Pins

It also should be noted that inputs and I/O pin feedbacks on the iFX780 recognize 2.0V as a logic high. Input leakage vs. standby current can be matched to CMOS or TTL input levels. This is done on an input-by-input basis via another set of keywords, such as "TTL_LEVEL" or "CMOS_LEVEL". Inputs are configured during programming but can be changed via in-circuit reconfiguration.

The following sections describe iFX780 output buffers and input buffers in more detail, and discuss power sequencing considerations for hybrid systems.

3.0 OUTPUT BUFFER CONSIDERATIONS

Figure 2 shows how the output buffers work. Two N-channel devices on the left side of the diagram pull the output high or low, based on the inputs from the combinatorial or registered macrocell, SRAM, or the JTAG register. The pull-up device pulls outputs to approximately 3.0V. Both devices are switched off for high-impedance mode. For open-drain operation, the upper device is always off while the lower device is switched.

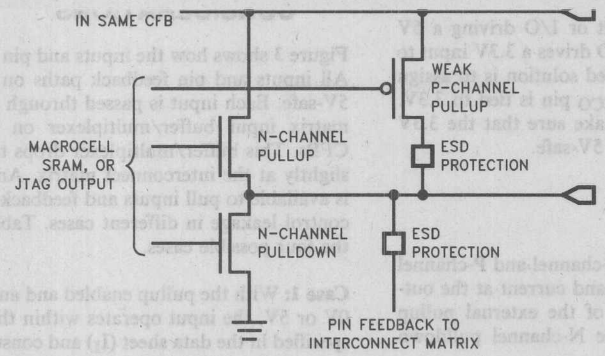


Figure 2. iFX780 Output Buffer Equivalent Circuit

For logic high outputs, the weak P-channel device pulls the outputs past 3.0V to the level determined by the V_{CCO} pin of a CFB. Thus any high level between 3.3V and 5V is supported by the output buffer. This P-channel device is switched off for high-impedance mode and is always off for open-drain operation. Table 1 summarizes operation of the output buffers for different modes.

3.3V Outputs

No issues exist for a 3.3V output or I/O pin driving a 3.3V input or bus. When a 3.3V output or I/O is driving a 5V input, the high level of a 3.3V output is at least 2.4V, which exceeds the 2.0V minimum for a 5V input device. No translator is required; designers should, however, check to see if the receiving device leaks current at TTL levels (system power consideration).

When the 3.3V output or I/O is on a bus that includes both 3.3V and 5V devices, it is possible to drive a 5V high into the 3.3V output or I/O pin. The question naturally arises: "Will driving 5V into a 3.3V I/O pin latch up the output and therefore require that I use a translator/buffer?" For the iFX780, the answer is: "Definitely not." For shared bus applications, the N-channel pullup and the P-channel pullups are normally turned off when other devices are driving the bus (i.e., the iFX780 is in high impedance mode), otherwise bus contention would occur. Outputs, however, may be active for short periods of time during transitions and have 5V sourced even when in a high impedance state. Since all gate inputs to the N- and P-channel devices are referenced to 5V, no leakage occurs. Design techniques have been employed that prevent the P-channel device from latching up. This same protection is present for I/O pins implementing inputs or bi-directional I/O. (The exception occurs during power-up and power-down; see "Power Sequencing" later in this brief.)

5V Outputs

No issues exist for a 5V output or I/O driving a 5V signal. When a 5V output or I/O drives a 3.3V input to another device, the recommended solution is to assign the output to a CFB whose V_{CCO} pin is tied to 3.3V. Otherwise the designer must make sure that the 3.3V input on the receiving device is 5V-safe.

Open-Drain Outputs

For Open-Drain outputs, the N-channel and P-channel pullups are always off. Voltage and current at the output is determined by the size of the external pullup resistor in conjunction with the N-channel pulldown device of the output.

4.0 INPUT BUFFER CONSIDERATIONS

Figure 3 shows how the inputs and pin feedbacks work. All inputs and pin feedback paths on the iFX780 are 5V-safe. Each input is passed through the interconnect matrix input buffer/multiplexer on its way to the CFBs. This buffer/multiplexer drops the input voltage slightly at the interconnect matrix. An internal pullup is available to pull inputs and feedback signals to 5V to control leakage in different cases. Table 2 summarizes the four possible cases.

Case 1: With the pullup enabled and an input voltage of 0V or 5V, the input operates within the leakage rating specified in the data sheet (I_I) and consumes no standby current (I_{SB}). This is the recommended case for 5V CMOS inputs.

Table 1. Output Buffer Mode Summary

Output Mode	N-Channel Pulldown	N-Channel Pullup	P-Channel Pullup
Standard Output—Logic High	Switched Off	Switched On	Switched On
Standard Output—Logic Low	Switched On	Switched Off	Switched Off
Standard Output—High Impedance	Switched Off	Switched Off	Switched Off
Open-Drain Output—Logic High	Switched Off	Always Off (External Pullup)	Always Off (External Pullup)
Open-Drain Output—Logic Low	Switched On (Pulls Against External Pullup)	Always Off	Always Off
Open-Drain Output—High Impedance	N/A (External Pullup)	N/A (External Pullup)	N/A (External Pullup)

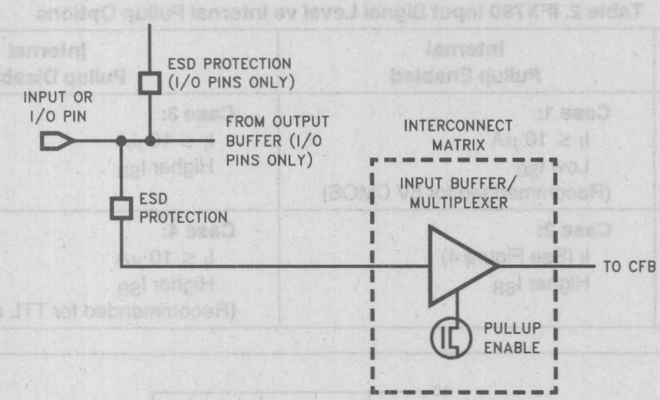


Figure 3. iFX780 Input Buffer Equivalent Circuit

Case 2: With the pullup enabled and an input voltage between 0V and 5V (e.g., being held at 3.0V by a TTL output), I_I will be higher than specification, causing I_{SB} to be higher. Figure 4 shows the leakage current at different voltage levels.

Case 3: With the pullup disabled and an input voltage of 5V, the internal voltage drop holds the input at approximately 3V. I_{SB} will be higher.

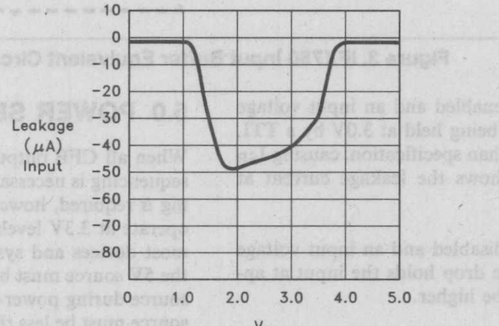
Case 4: For input signals between 0V and 3V, a designer can disable the pullup to bring the leakage current back within specification. This is the recommended case for TTL or 3V CMOS inputs. It should be noted, however, that I_{SB} is 10%–20% higher in this case than with case 2.

5.0 POWER SEQUENCING

When all CFB outputs operate at 5V levels, no power sequencing is necessary for the iFX780. Power sequencing *is* required, however, when any or all CFB outputs operate at 3.3V levels. In this case, as is common with most devices and systems that use both 5V and 3.3V, the 5V source must be equal to or greater than the 3.3V source during power-up. During power-down, the 3.3V source must be less than or equal to the 5V source. This sequencing will prevent I/O latchup during power-up and reverse-bias through the V_{CC} pins during power-down. Figure 5 shows this sequencing.

Table 2. iFX780 Input Signal Level vs Internal Pullup Options

Input Signal Level	Internal Pullup Enabled	Internal Pullup Disabled
$V_{IH} = 5V$	**Case 1:** $I_I \leq 10\ \mu A$ Low I_{SB} (Recommended for 5V CMOS)	**Case 3:** $I_I \leq 10\ \mu A$ Higher I_{SB}
$V_{IH} = 3V$	**Case 2:** I_I (See Figure 4) Higher I_{SB}	**Case 4:** $I_I \leq 10\ \mu A$ Higher I_{SB} (Recommended for TTL and 3V CMOS)



Conditions:
$T_A = 25°C$
$V_{CC} = 5V$

Figure 4. iFX780 Input Leakage vs Voltage—Pullup Enabled

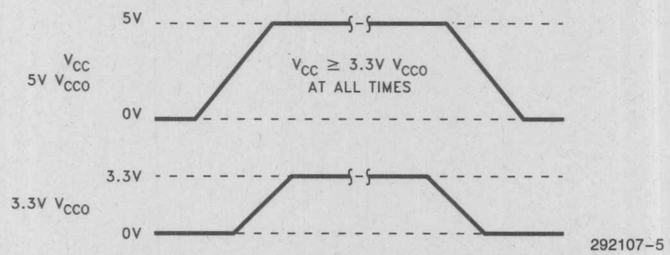


Figure 5. iFX780 5V/3.3V Power Supply Sequencing

APPLICATION
BRIEF

Implementing FIFOs Using the iFX780 FPGA

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APPLICATIONS ENGINEERING
PROGRAMMABLE LOGIC DEVICES

October 1993

Order Number: 292108-001

Implementing FIFOs Using the iFX780 FPGA

CONTENTS

1.0 INTRODUCTION

The ability to receive and store data from one part of a system at one rate and point in time and to send that data to another part of the system at a different rate and point in time has made the FIFO (First In First Out) buffer an important element in system design. Off-the-shelf FIFOs come in many widths and depths and with several styles of interfaces. But additional components, usually PLDs, are still required to make them work in most systems. The iFX780 FPGA architecture allows application-specific FIFOs (memory included!) to be implemented in a single device, a task not possible with most other FPGA architectures.

Application-specific FIFOs can be used in a wide variety of applications, including:

- Peripherals for data acquisition in embedded systems.
- Bridging buffers in systems that implement more than one bus type.
- Accelerators in imaging and instrumentation.

This brief shows how to implement FIFOs in a single iFX780 FLEXlogic FPGA. A general-purpose FIFO is described and guidelines for several modifications to the original design are provided.

2.0 FEATURE/FUNCTION OVERVIEW

The iFX780 is the first member of Intel's FLEXlogic family of FPGA-class devices. The iFX780 is an 80-macrocell device that offers a fast, deterministic 10 ns t_{PD} from any input or I/O to any I/O. It can operate in-system at speeds up to 80 MHz. The device is grouped into eight Configurable Function Blocks (CFBs). Each CFB can be independently configured as a 24V10-type PLD with parallel identity compare or as a 128-deep x 10-bit-wide bank of SRAM.

This ability to use a CFB either as a bank of SRAM or as programmable logic allows FIFOs to be implemented in a single iFX780 device. CFBs configured as SRAM provide data storage while CFBs configured as PLDs provide the control logic and system interface. This application brief discusses only those features of the device that apply directly to FIFO implementation. For additional information on the architecture and features of the device, refer to the iFX780 FPGA data sheet (literature order no: 290459) and other application briefs.

CFBs as SRAM

The interface to a CFB configured as SRAM is the same as for most discrete SRAM devices. Address lines A6–A0 select an individual memory location. BE# (Block Enable#), WE# (Write Enable#), and OE# (Output Enable#) are the control signals. Ten data inputs (DI9–DI0) come from the interconnect matrix, while ten data outputs D9–D0) are available at I/O pins and/or as feedbacks to the interconnect matrix. I/O pins can also use the pin feedback paths to implement bi-directional I/O if common SRAM inputs and outputs are required.

CFBs as 24V10s

When configured as a 24V10 PLD, an identity compare of up to 12 bits can be performed in parallel with standard SOP logic for each CFB. Two asynchronous clocks are available for each CFB and can be used on a macrocell-by-macrocell basis in the CFB. Each macrocell can implement registered or combinatorial logic with a variety of clocking and control options. Dual feedback allows macrocell outputs to be buried while leaving the I/O pin available for use as an input. In the 132-pin package, outputs from all 80 macrocells are available at I/O pins. In the 84-pin package, outputs from 60 macrocells are available at I/O pins; outputs from the remaining 20 macrocells are buried.

3.0 IMPLEMENTING THE FIFO

Figure 1 shows a block diagram of the FIFO circuit implemented here. The design is a 128-deep x 10-bit-wide FIFO with separate read and write ports.

The read pointer is implemented using seven macrocells configured as registers (RP6–RP0); the write pointer also uses seven macrocells configured as registers (WP6–WP0). Both pointers use an asynchronous clock that transitions on the trailing edge of the RD# or WR# command, respectively. Seven additional macrocells configured as combinatorial logic are used to multiplex the read and write pointers to the SRAM address lines (A6–A0).

The identity compare logic compares the read pointer with the write pointer. The compare output (REQW or Read EQuals Write) feeds a Tracking State Machine (TSM) that keeps track of read and write operations. Figure 2 shows the state diagram for the TSM. In response to a RESET# pulse, the TSM transitions to the FIFO_EMPTY state, awaiting the first write. The TSM clocks on the leading edge of the RD# or WR# command and tracks any combination of read and write operations. The current state is combined with REQW to generate the EMPTY# or FULL# signals. These signals inform the system when the FIFO is empty or full to help prevent data overrun or underrun. The system is responsible for holding off on reads if the FIFO is empty and holding off on writes if the FIFO is full. Since the SRAM is not dual-ported, reads and writes are not permitted at the same time.

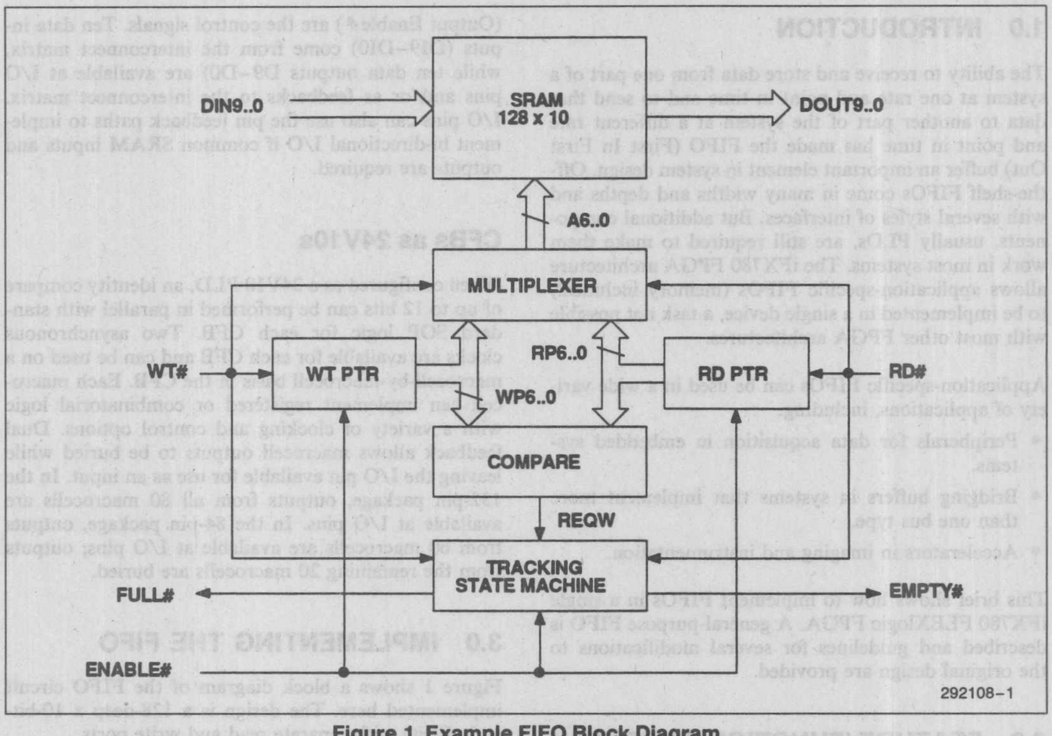

Figure 1. Example FIFO Block Diagram

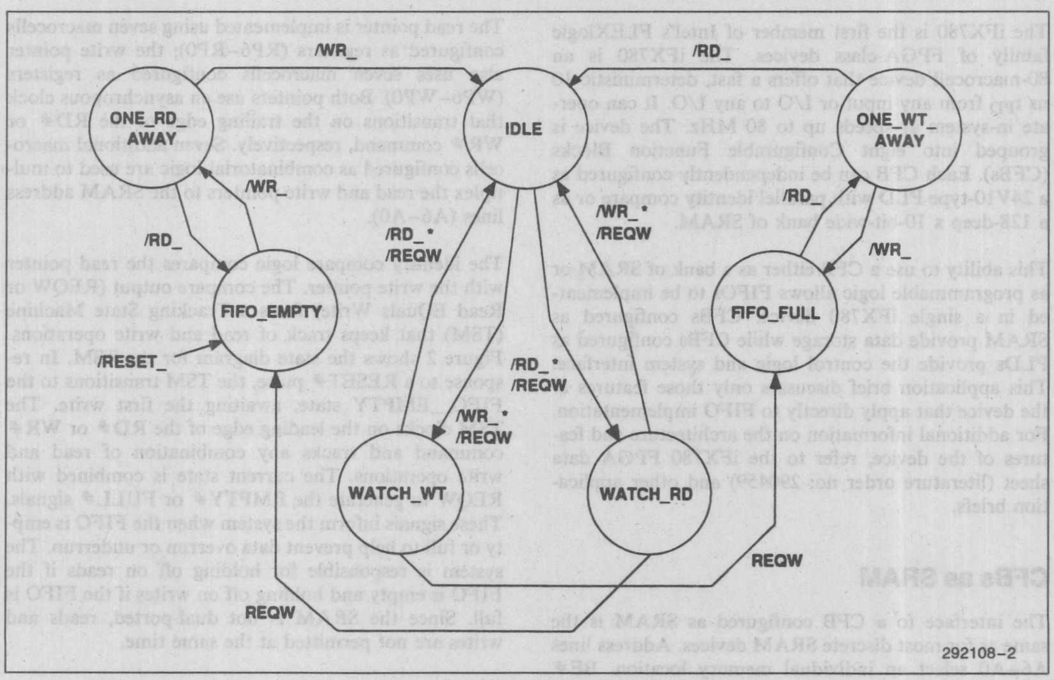

Figure 2. Example FIFO Control State Machine

Device utilization is four CFBs (one used as SRAM and three as 24V10 logic). This is only half the resources of the iFX780 The number of macrocells in the logic portions is broken down as follows:

Read Pointer	=	7 macrocells
Write Pointer	=	7 macrocells
Multiplexer	=	7 macrocells
Compare	=	1 macrocell
State Machine	=	5 macrocells
Total	=	27 macrocells

Read and write access timing for FIFO operations is shown in Figure 3. Read and write access times are both 25 ns. Reads from and writes to the FIFO implemented in the iFX780-10 can operate at up to 27 MHz. This is determined by the maximum delay paths from the read/write pointer, through the address multiplexer, to the SRAM, as follows:

$$t_{ACO} + t_{PD} + (t_{AA} \text{ or } t_{AW}) = \text{total delay}$$

$$1/\text{total delay} = \text{max. frequency}$$

$$12 \text{ ns} + 10 \text{ ns} + 15 \text{ ns} = 37 \text{ ns}$$

$$1/37 \text{ ns} = 27 \text{ MHz}$$

t_{ACO} is the clock-to-output timing from the falling edge of the RD# or WR# command line. t_{PD} is the time the pointers take to propagate through the multiplexer. t_{AA} is the read access time for the SRAM; t_{AW} is the write access time.

The predictable nature of the device architecture makes it easy to determine timing for circuits implemented in the iFX780. For a detailed discussion on iFX780 timing, refer to AB-51, "FLEXlogic iFX780 Logic Configuration Timing", literature order no: 292112.

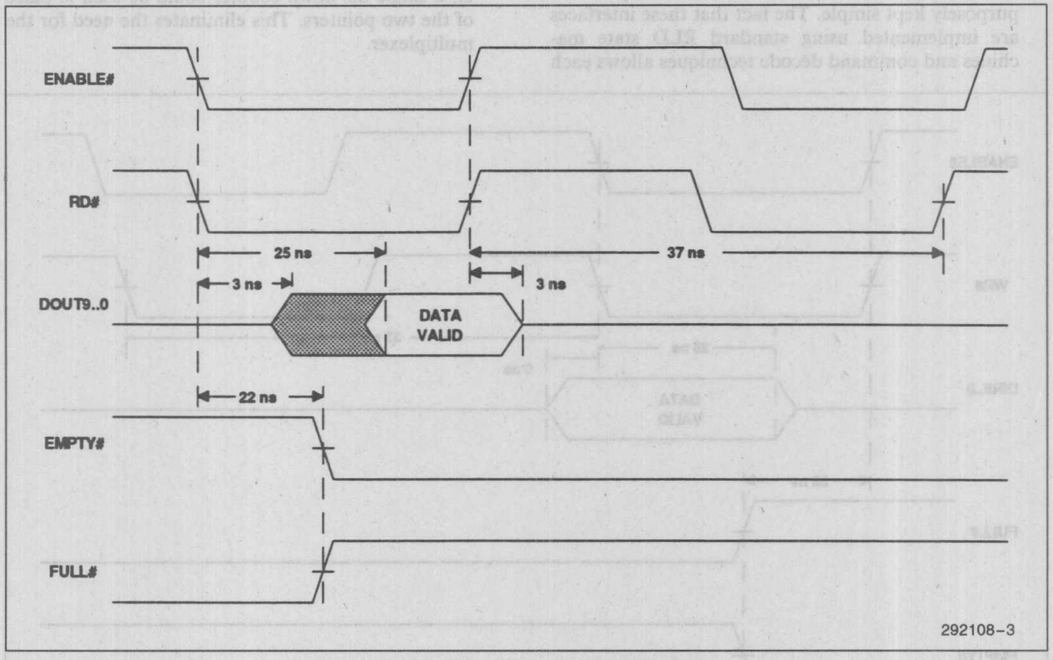

Figure 3. FIFO Read Access Timing

the features of the FIFO described here can be scaled and/or modified for different application needs. Modifications include the following:

- SRAM blocks can be added in parallel to easily increase the width of the FIFO. No changes need to be made to the Tracking State Machine. SRAM blocks can also be added to increase the depth of the FIFO. The read and write pointers and the multiplexer/compare logic would have to be widened slightly to address the additional memory. The outputs from the SRAM blocks would need to be OR-tied, making use of the iFX780 open-drain output option. In this case, output enable equations need to ensure that only one SRAM block is driving the common output bus at any given time. External pullup resistors are required on the common output bus.
- The interfaces to the FIFO for this example were purposely kept simple. The fact that these interfaces are implemented using standard PLD state machines and command decode techniques allows each
- CFB outputs in the iFX780 can swing at 5V levels or 3.3V levels. Inputs respond to 2.0V as a logic high, regardless of the output swing. This allows FIFOs to be designed for use in hybrid 5V/3.3V systems. Refer to AB-27 "Using the iFX780 in Hybrid 3.3V/5V Systems", literature order no: 272107 for detailed information.
- If an application needs more FIFO space than provided by internal SRAM, the outputs from the address multiplexer can drive an external SRAM device. The base design will need some slight modifications (width of counters and multiplexer). This, however, frees up the CFB originally used as SRAM for implementing additional logic.
- A modified form of the FIFO design could be used to implement a processor stack. Since a stack is by nature a single-port LIFO (Last In First Out) buffer, a single up/down counter could be used in place of the two pointers. This eliminates the need for the multiplexer.

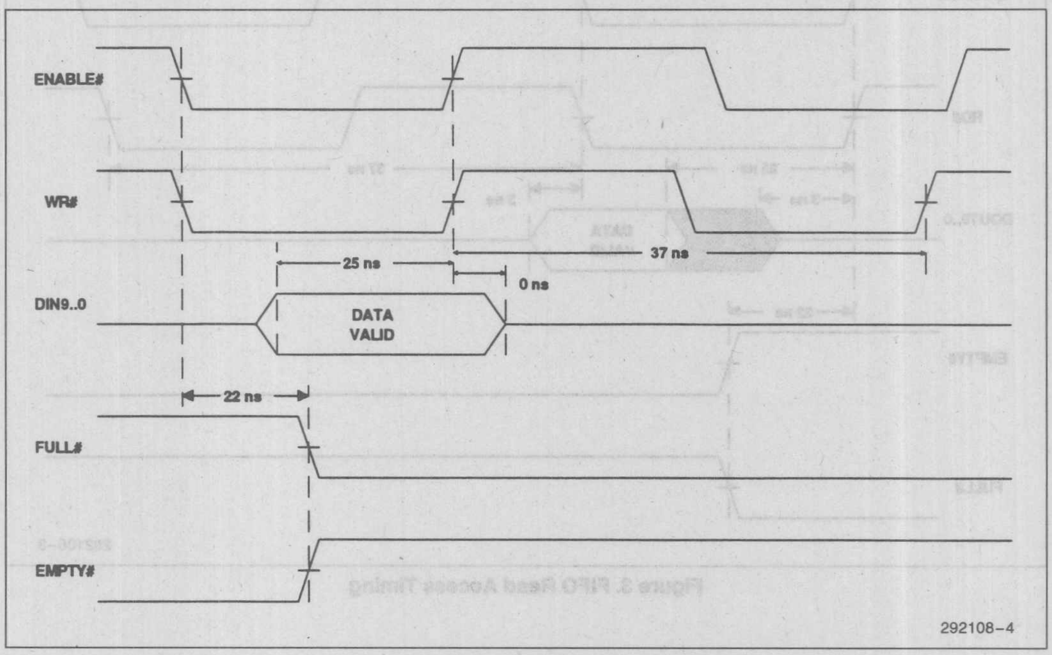

Figure 4. FIFO Write Access Timing

APPLICATION BRIEF

80960CA DRAM Controller in a FLEXlogic iFX780 FPGA

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October 1993

80960CA DRAM Controller in a FLEXlogic iFX780 FPGA

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1.0 INTRODUCTION

The embedded processor market lacks the standard systems architectures that exist in other markets. As a result, standard chipsets are not available to help design products for the embedded market. This situation makes the job of embedded system design more difficult than it might otherwise be. Many of the same subsystems need to be designed for embedded systems as for other markets, but fewer off-the-shelf building blocks are available.

This application brief shows a DRAM controller for an 80960CA-based embedded system, implemented in a single iFX780 FLEXlogic FPGA. Since the iFX780 is a programmable device, this design provides a standard building block for embedded systems that allows customization for different memory subsystems, processor variations, and applications. The DRAM controller requires only 30% of the macrocells in the iFX780, thus allowing additional logic functions to be integrated with no additional board space.

2.0 FEATURE/FUNCTION OVERVIEW

The iFX780 is the first member of Intel's FLEX-logic family of FPGA devices. The iFX780 is an 80-macrocell device that offers a fast, deterministic 10 ns t_{PD} from any input or I/O to any I/O. It can operate in-system at speeds of up to 80 MHz. The device is grouped into eight Configurable Function Blocks (CFBs); each CFB can be independently configured as a 24V10-type PLD or as a 128-deep x 10-bit-wide bank of SRAM.

In the 132-pin package, outputs from all 80 macrocells are available at I/O pins. In the 84-pin package, outputs from 60 macrocells are available at I/O pins; outputs from the remaining 20 macrocells are buried.

The speed and density of the iFX780 allow it to easily implement DRAM controllers. The DRAM controller described here uses CFBs as 24V10-type PLDs and does not require the use of the SRAM capability. This application brief discusses only those features of the device that apply to DRAM controller applications. For additional information on the architecture and features of the device, refer to the iFX780 FPGA data sheet (literature order no: 290459) and other iFX780 application briefs.

When configured as a 24V10 PLD, an identity compare of up to 12 bits can be performed in parallel to the SOP logic for each CFB. Each macrocell can implement registered or combinatorial logic with a variety of clocking and control options. Two asynchronous clocks are available for each CFB and can be used on a macrocell-by-macrocell basis in a CFB. Each register can be configured as D-type or T-type registers. T-type or Toggle registers can greatly reduce the number of p-terms in state machines of D-type registers, thereby increasing the probability of designs fitting into a device. Dual feedback allows macrocell outputs to be buried while leaving the I/O pin available for use as an input.

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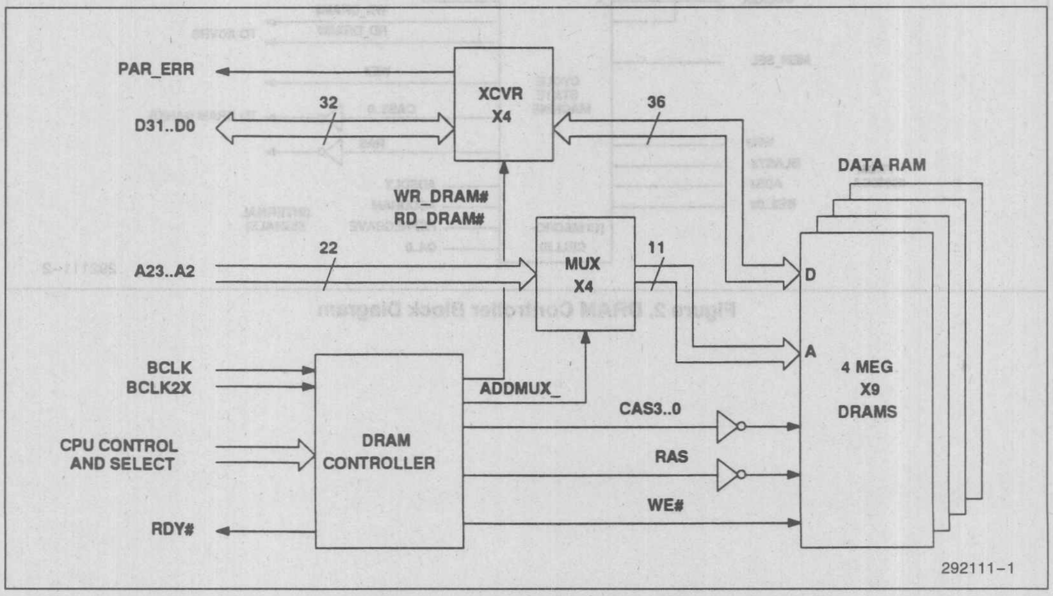

Figure 1. Memory Subsystem Block Diagram

3.0 DRAM SUBSYSTEM

Figure 1 shows a block diagram of the DRAM subsystem. This subsystem provides 16 Mbytes of DRAM for a 16 MHz single-clock mode 80960CA embedded processor system. The memory is segmented into four banks of nine DRAM devices, allowing 32-bit wide memory accesses with a parity bit for each byte. Each bank contains 4-Megabit x 1 nibble-mode DRAMS. Nibble-mode DRAMs are used to support burst cycles of one to four transfers in length with each bit of a nibble providing one bit of a transfer. The banks are not interleaved.

Two clocks are available, BCLK, which runs at the processor rate of 16 MHz, and BCLK2X, which is twice the processor rate at 32 MHz. This allows the DRAM state machine to sequence twice for each processor clock cycle.

Four Bi-CMOS bus transceivers with parity generation and checking interface the DRAM banks to the processor data bus. A parity bit is generated and stored during each DRAM write. During each read, the parity bit is regenerated from the data and compared to the stored parity bit. A parity mismatch is flagged as an error. RD_DRAM# and WT_DRAM# control the direction of data flow through the transceivers.

Three multiplexers translate the 22 address signals into the 11 DRAM address lines. ADDMUX# from the controller feeds the select input to the multiplexers to determine whether the row or column address is being sent.

4.0 IMPLEMENTING THE DRAM CONTROLLER

Figure 2 shows a block diagram of the DRAM controller circuit. The DRAM controller includes two blocks, a Refresh Counter, and a Cycle State Machine (CSM).

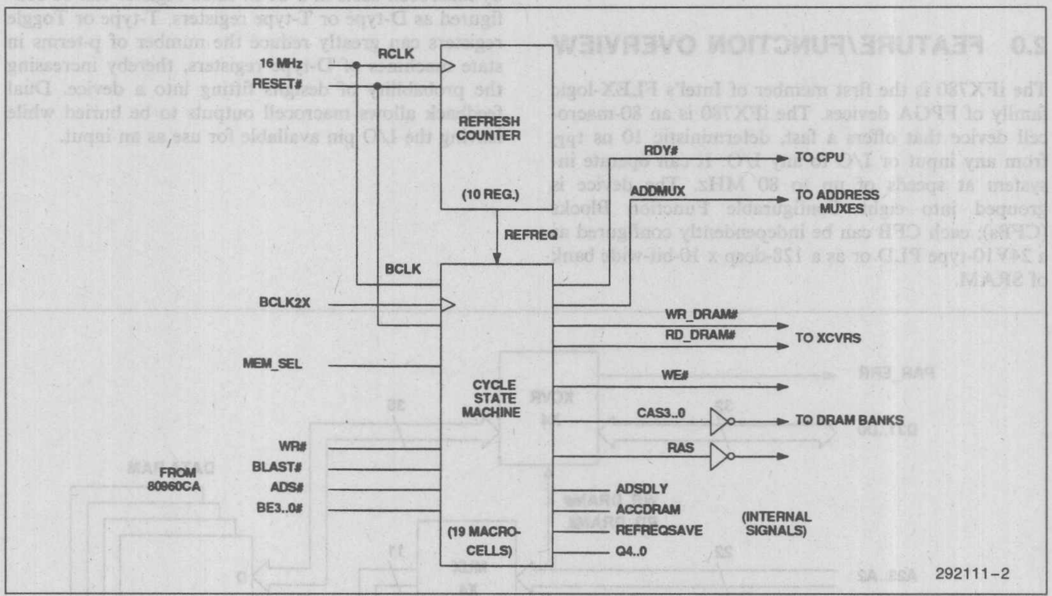

Figure 2. DRAM Controller Block Diagram

Refresh Counter

The Refresh Counter provides a refresh request pulse (REFREQ) to the CSM every 16 μs. This pulse is generated by clocking the counter with the 16 MHz BCLK signal and counting 250 clock cycles. REFREQ is then generated for a single clock cycle. A refresh cycle every 16 μs guarantees that all 1024 rows in the DRAM are refreshed once every 16.38 ms. The CSM arbitrates between refresh requests and read/write commands and executes the DRAM refresh cycle.

Cycle State Machine

The DRAM CSM operates from the faster 32 MHz BCLK2X but uses the slower 16 MHz BCLK to make sure that DRAM cycles are in phase with processor cycles. The CSM uses five registered macrocells (Q4–Q0) to define the eleven states shown in Figure 3. A decode stage in the CSM uses the output states from the registers to generate the appropriate DRAM and buffer/multiplexer control signals. The read and write paths are the same except for the entry points and the

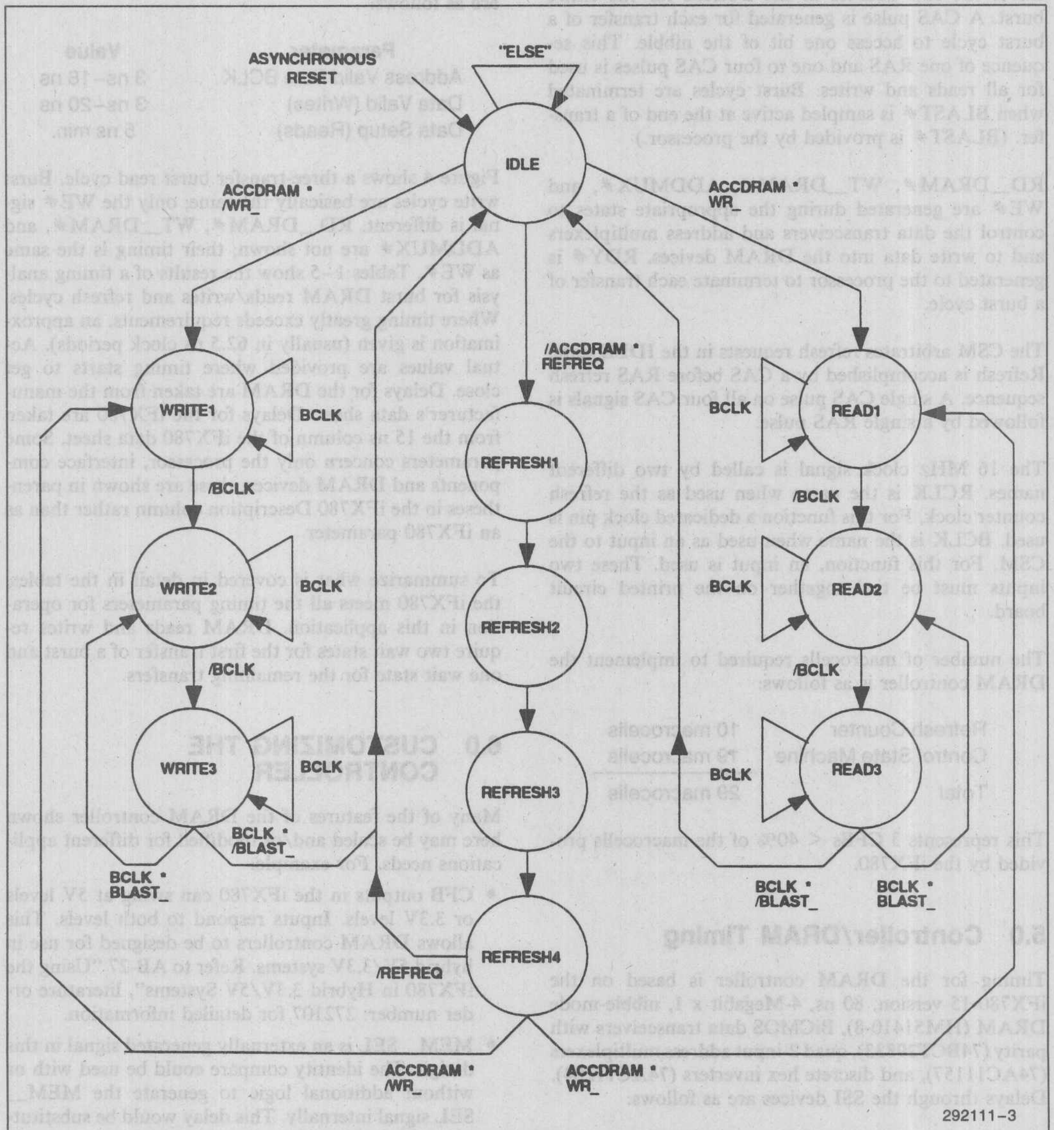

Figure 3. Cycle State Machine Diagram

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control signals generated during the sequence. The refresh path allows a quick exit from REFRESH4 to the read or write path to save the time a transition through an IDLE state would consume.

The active-high CAS3–0 and RAS signals from the CSM drive inverters, which in turn drive the DRAM arrays. The inverters provide the drive capability for the DRAM CAS and RAS signals and the proper polarity. Nibble-mode DRAM accesses require a single RAS for a burst cycle of one to four transfers. RAS stores the row address in the DRAM for the entire burst. A CAS pulse is generated for each transfer of a burst cycle to access one bit of the nibble. This sequence of one RAS and one to four CAS pulses is used for all reads and writes. Burst cycles are terminated when BLAST# is sampled active at the end of a transfer. (BLAST# is provided by the processor.)

RD__DRAM#, WT__DRAM#, ADDMUX#, and WE# are generated during the appropriate states to control the data transceivers and address multiplexers and to write data into the DRAM devices. RDY# is generated to the processor to terminate each transfer of a burst cycle.

The CSM arbitrates refresh requests in the IDLE state. Refresh is accomplished by a CAS before RAS refresh sequence. A single CAS pulse on all four CAS signals is followed by a single RAS pulse.

The 16 MHz clock signal is called by two different names. RCLK is the name when used as the refresh counter clock. For this function a dedicated clock pin is used. BCLK is the name when used as an input to the CSM. For this function, an input is used. These two inputs must be tied together on the printed circuit board.

The number of macrocells required to implement the DRAM controller is as follows:

Refresh Counter	10 macrocells
Control State Machine	19 macrocells
Total	29 macrocells

This represents 3 CFBs < 40% of the macrocells provided by the iFX780.

5.0 Controller/DRAM Timing

Timing for the DRAM controller is based on the iFX780-15 version, 80 ns, 4-Megabit x 1, nibble-mode DRAM (HM51410-8), BiCMOS data transceivers with parity (74BCT29833), quad 2-input address multiplexers (74AC11157), and discrete hex inverters (74AC11204). Delays through the SSI devices are as follows:

Device	Delay
Data Transceiver Delay (Flow Through)	10 ns
Address Multiplexer Delay (Switch from A to B)	9.5 ns
Inverter Delay	7.5 ns

Address valid, data valid, and data setup times for the 80960CA are also crucial for determining memory access timing. These parameters for the 16 MHz version are as follows:

Parameter	Value
Address Valid from BCLK	3 ns–18 ns
Data Valid (Writes)	3 ns–20 ns
Data Setup (Reads)	5 ns min.

Figure 4 shows a three-transfer burst read cycle. Burst write cycles are basically the same; only the WE# signal is different. RD__DRAM#, WT__DRAM#, and ADDMUX# are not shown; their timing is the same as WE#. Tables 1–5 show the results of a timing analysis for burst DRAM reads/writes and refresh cycles. Where timing greatly exceeds requirements, an approximation is given (usually in 62.5 ns clock periods). Actual values are provided where timing starts to get close. Delays for the DRAM are taken from the manufacturer's data sheet. Delays for the iFX780 are taken from the 15 ns column of the iFX780 data sheet. Some parameters concern only the processor, interface components and DRAM devices; these are shown in parentheses in the iFX780 Description column rather than as an iFX780 parameter.

To summarize what is covered in detail in the tables, the iFX780 meets all the timing parameters for operation in this application. DRAM reads and writes require two wait states for the first transfer of a burst and one wait state for the remaining transfers.

6.0 CUSTOMIZING THE CONTROLLER

Many of the features of the DRAM controller shown here may be scaled and/or modified for different applications needs. For example:

- CFB outputs in the iFX780 can swing at 5V levels or 3.3V levels. Inputs respond to both levels. This allows DRAM controllers to be designed for use in hybrid 5V/3.3V systems. Refer to AB-27 "Using the iFX780 in Hybrid 3.3V/5V Systems", literature order number: 272107 for detailed information.
- MEM__SEL is an externally generated signal in this design. The identity compare could be used with or without additional logic to generate the MEM__SEL signal internally. This delay would be substituted for external address decode delay.

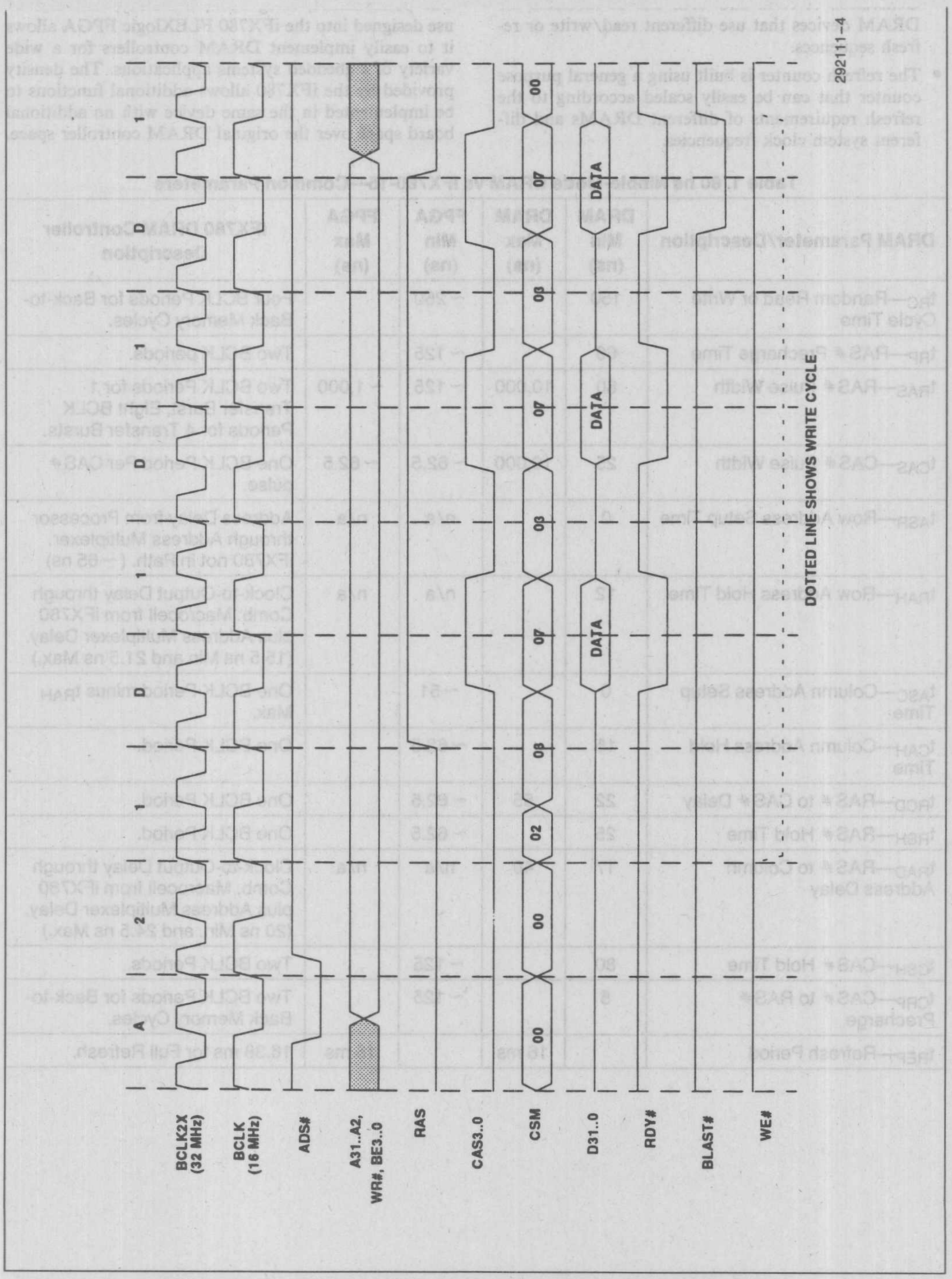

Figure 4. 80960CA DRAM Controller Burst Read—Three Transfers

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- Generation of RAS and CAS can be modified for DRAM devices that use different read/write or refresh sequences.
- The refresh counter is built using a general purpose counter that can be easily scaled according to the refresh requirements of different DRAMs and different system clock frequencies.

The performance, integration, flexibility, and ease-of-use designed into the iFX780 FLEXlogic FPGA allows it to easily implement DRAM controllers for a wide variety of embedded systems applications. The density provided by the iFX780 allows additional functions to be implemented in the same device with no additional board space over the original DRAM controller space.

Table 1. 80 ns Nibble-Mode DRAM vs iFX780-15—Common Parameters

DRAM Parameter/Description	DRAM Min (ns)	DRAM Max (ns)	FPGA Min (ns)	FPGA Max (ns)	iFX780 DRAM Controller Description
t_{RC}—Random Read or Write Cycle Time	150		~250		Four BCLK Periods for Back-to-Back Memory Cycles.
t_{RP}—RAS# Precharge Time	60		~125		Two BCLK periods.
t_{RAS}—RAS# Pulse Width	80	10,000	~125	~1,000	Two BCLK Periods for 1 Transfer Burst; Eight BCLK Periods for 4 Transfer Bursts.
t_{CAS}—CAS# Pulse Width	25	10,000	~62.5	~62.5	One BCLK Period Per CAS# pulse.
t_{ASR}—Row Address Setup Time	0		n/a	n/a	Address Delay from Processor through Address Multiplexer. iFX780 not in Path. (~65 ns)
t_{RAH}—Row Address Hold Time	12		n/a	n/a	Clock-to-Output Delay through Comb. Macrocell from iFX780 plus Address Multiplexer Delay. (15.5 ns Min and 21.5 ns Max.)
t_{ASC}—Column Address Setup Time	0		~51		One BCLK Period minus t_{RAH} Max.
t_{CAH}—Column Address Hold Time	15		~62.5		One BCLK Period.
t_{RCD}—RAS# to CAS# Delay	22	55	~62.5		One BCLK Period.
t_{RSH}—RAS# Hold Time	25		~62.5		One BCLK Period.
t_{RAD}—RAS# to Column Address Delay	17	40	n/a	n/a	Clock-to-Output Delay through Comb. Macrocell from iFX780 plus Address Multiplexer Delay. (20 ns Min. and 24.5 ns Max.)
t_{CSH}—CAS# Hold Time	80		~125		Two BCLK Periods.
t_{CRP}—CAS# to RAS# Precharge	5		~125		Two BCLK Periods for Back-to-Back Memory Cycles.
t_{REF}—Refresh Period		16 ms		16 ms	16.38 ms for Full Refresh.

Table 2. 80 ns Nibble-Mode DRAM vs iFX780-15—Read Cycle

DRAM Parameter/Description	DRAM Min (ns)	DRAM Max (ns)	FPGA Min (ns)	FPGA Max (ns)	iFX780 DRAM Controller Description
t_{RAC}—Access Time from RAS#		80	107.5		Two BCLK Periods minus RAS# Inverter minus Data Transceiver Delay minus Processor Setup Time.
t_{CAC}—Access Time from Falling Edge		25	47.5		One BCLK Period minus Data Transceiver Delay minus Processor Setup Time.
t_{AA}—Access Time from Column Address		40	96		One BCLK Period plus t_{ASC} minus data transceiver delay minus Processor Data Setup Time
t_{RCS}—Read Command Setup Time	0		~62.5		One BCLK Period.
t_{RCH}—Read Command Hold Time Referenced to RAS#	0		~62.5		One BCLK Period.
t_{RRH}—Read Command Hold Time Referenced to RAS#	10		~62.5		One BCLK Period.
t_{OFF}—Output Buffer Turnoff Delay	0	20	n/a	n/a	DRAM Delay through Data Transceiver. iFX780 not in Path. (10 ns. Min and 30 ns Max.)

Table 3. 80 ns Nibble-Mode DRAM vs iFX780-15—Write Cycle

DRAM Parameter/Description	DRAM Min (ns)	DRAM Max (ns)	FPGA Min (ns)	FPGA Max (ns)	iFX780 DRAM Controller Description
t_{WCS}—Write Command Setup Time	0		~62.5		One BCLK Period.
t_{WCH}—Write Command Hold Time	15		~62.5	~62.5	One BCLK Period.
t_{CWL}—Write Command to CAS# Lead Time	25		~62.5		One BCLK Period.
t_{DS}—Data in Setup Time	0		n/a	n/a	Delay from Processor through Data Transceiver. iFX780 not in Path. (40 ns Min.)
t_{DH}—Data in Hold Time	15		n/a	n/a	Delay from Processor through Data Transceiver. iFX780 not in Path. (65.5 ms Min.)

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Table 4. 80 ns Nibble-Mode DRAM vs iFX780-15—Refresh Cycle

DRAM Parameter/Description (CAS# Before RAS#)	DRAM Min (ns)	DRAM Max (ns)	FPGA Min (ns)	FPGA Max (ns)	iFX780 DRAM Controller Description
t_{CSR}—CAS# Setup Time	10		~62.5	~62.5	One BCLK period.
t_{CHR}—CAS# Hold Time	20		~62.5	~62.5	One BCLK period.
t_{RPC}—RAS# Precharge to CAS# Hold Time	10		~62.5	~62.5	One BCLK period.

Table 5. 80 ns Nibble-Mode DRAM vs iFx780-15—Nibble-Mode Cycle

DRAM Parameter/Description	DRAM Min (ns)	DRAM Max (ns)	FPGA Min (ns)	FPGA Max (ns)	iFX780 DRAM Controller Description
t_{NAC}—Nibble-Mode Access Time		25	~40		One BCLK Period minus CAS# Inverter Delay minus Data Transceiver Delay minus Processor Data Setup Time.
t_{NC}—Nibble-Mode Cycle Time	45		~125		Two BCLK periods.
t_{NCP}—Nibble-Mode CAS# Precharge Time	10		~62.5		One BCLK Period.
t_{NCA}—Nibble-Mode CAS# Pulse Width	25	80	~62.5	~62.5	One BCLK Period.
t_{MRSH}—Nibble-Mode RAS# Hold Time	25		~62.5		One BCLK Period.

FLEXlogic iFX780 Logic Configuration Timing

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October 1993

Order Number: 292112-001

FLEXlogic iFX780 Logic Configuration Timing

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1.0 INTRODUCTION

With the advent of Field Programmable Gate Arrays (FPGAs), designers have the ability to quickly integrate large amounts of logic into a single device. A wide variety of CAE tools exist which take designs described in text and/or graphic formats and translate them into a functioning FPGA in a very short period of time.

But function alone is not the entire equation. An FPGA design must also meet timing requirements dictated by system needs. Many FPGA devices fail to operate in even moderate performance designs, running out of steam at 20 MHz or less. Very few FPGAs deliver the predictable high performance required to meet the needs of high speed systems running at 50 MHz–80 MHz.

The Intel FX780 operates easily and predictably in 50 MHz to 80 MHz systems. This application brief discusses all of the timing parameters necessary to perform predictable, high-speed design with this device.

2.0 FPGA ARCHITECTURES

FPGA devices fall into one of two fundamental architectural categories: fine-grained and segmented.

Fine-Grained

Fine-grained FPGAs have device resources grouped into blocks of two registers or less. Although this architecture historically has yielded the highest density devices, it is also characterized by variable routing delays between device resources that are not fully known until the final "place and route" process is done. Maximum device performance is often limited by the longest delay path. Only after analysis of all paths can the true performance be determined and compared to the requirements of the design. If the performance is unacceptable, manual constraints must be added to the "place and route" process and another iteration must be completed. For high performance systems, tedious hand intervention in the "place and route" process is usually a requirement to meet performance goals. Even then, the designer may not be successful.

Segmented

Segmented architecture FPGAs, such as the Intel FLEXlogic family, have device resources grouped into larger "PLD" blocks which contain 10 or more macrocells that can be configured for registered or combinatorial logic functions. Segmented FPGAs are characterized by fixed routing delays between device resources that can be tested, guaranteed and specified in the device's datasheet. This approach yields devices that provide higher performance in most applications.

In the FLEXlogic devices, the delay through the Global Interconnect Matrix is uniform between any two registers. The same holds true for all input and I/O to register paths. Thus, performance is predictable for all possible routing combinations.

To summarize, segmented architecture FPGAs provide higher and more predictable performance than fine-grained FPGAs.

3.0 FLEXlogic iFX780 OVERVIEW

The first member in Intel's FLEXlogic family of FPGAs is the iFX780. The FLEXlogic iFX780 is a very fast, medium-density, low power FPGA. The SRAM-based, segmented architecture iFX780 contains 80 advanced macrocells which are organized into 8 Configurable Function Blocks (CFBs) (Figure 1). Each CFB can be configured as a 24V10-type PLD or as a 128 deep x 10 wide bank of 15 ns SRAM. Each CFB in the 132-pin PQFP and each pair of CFBs in the 84-pin PLCC version have selectable 5V/3.3V output buffers.

Clocking options allow setup and clock-to-output times to be matched to the requirements of system timing. Flexible control signals and a parallel comparator allow complex functions to be implemented in each CFB.

The iFX780 is initialized by on-chip non-volatile memory, but can be reconfigured in-circuit. Reconfiguration as well as boundary scan testing is accomplished via the JTAG 1149.1 test port. For more information, refer to the iFX780 datasheet (Lit. #290459).

Tools support for the iFX780 includes Intel's free PLDshell Plus software as well as most commonly used third-party FPGA/PLD design tools.

Although each CFB can be configured as either general purpose logic (24V10s) or as fast SRAM, this timing discussion will focus on logic configurations. A thorough discussion of SRAM configuration timing is included in the iFX780 datasheet, literature order number 290459.

For designs that use the CFBs as general purpose 24V10 blocks, only a few core timing parameters need to be considered. Combinatorial logic sections of the design involve T_{PD}. Multiple passes through CFBs involve an integer multiple of T_{PD}. Control of the tristate function on every I/O pin is described by T_{ZX} and T_{XZ}. The timing for registered logic sections is completely described by T_{SU}, T_{CO} and T_H.

All of these parameters are tested, guaranteed and specified in the iFX780 datasheet under worst-case conditions. The definition of worst case is V_{CC} = Min, Temp = Max for a given temperature-grade device.

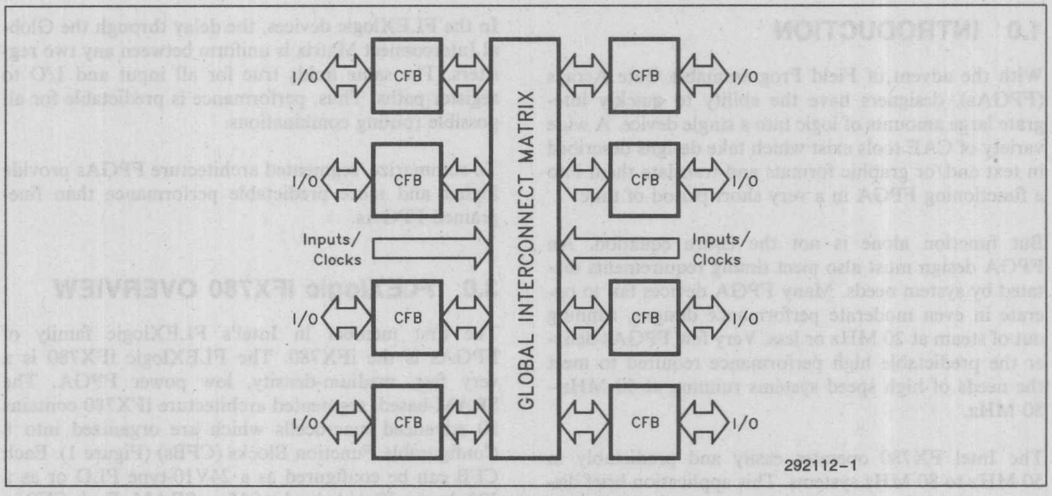

Figure 1. iFX780 Block Diagram

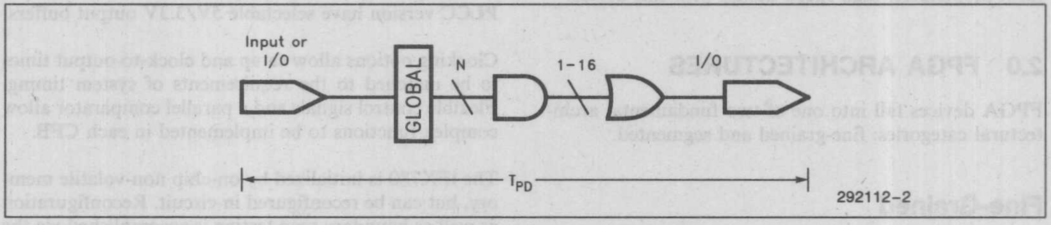

Figure 2. Combinatorial Delay

4.0 COMBINATORIAL LOGIC TIMING

T_{PD}

T_{PD} is the combinatorial signal propagation delay from any device input or I/O pin, through the global interconnect matrix, through the logic array (macrocell), and out the device I/O (Figure 2). Any function that can be implemented in one pass through the logic array is described by the parameter T_{PD}. For two of the ten macrocells in each CFB, a function can be up to 16 product terms wide. For the remaining 8 macrocells in each CFB, the maximum function can be up to 8 product terms wide. A product term is generically defined as an "N-input AND gate". A macrocell that contains 16 product terms is thus capable of logically "OR"ing 16 N-input AND gates. In the iFX780, the maximum value for N is 24, which is the number of terms that fan-into each CFB from the Global Interconnect Matrix.

To implement their maximum width functions, iFX780 macrocells borrow product terms from neighboring macrocells. There is no additional delay incurred by signals that use borrowed product terms. Because of this, no timing consideration needs to be made with respect to product term allocation.

Very complex combinatorial functions, from 17 to 248 product terms, can be implemented by distributing the function over one or more macrocells that serially feed an output macrocell (see Figure 3). In this situation, the pin-to-pin delay would be two times T_{PD}.

Identity Compare Function Timing

In addition to being able to implement logic on product terms, the iFX780 contains dedicated identity compare logic in each CFB. Any or all of the 24 signals that feed into the CFB from the Global Interconnect Matrix may be formed into two data words that feed into the dedicated compare logic. The result of the compare function may then be connected to any single macrocell in the CFB as a product term (see Figure 4). Identity compares of up to 12 bits can be performed with the iFX780 in one T_{PD}.

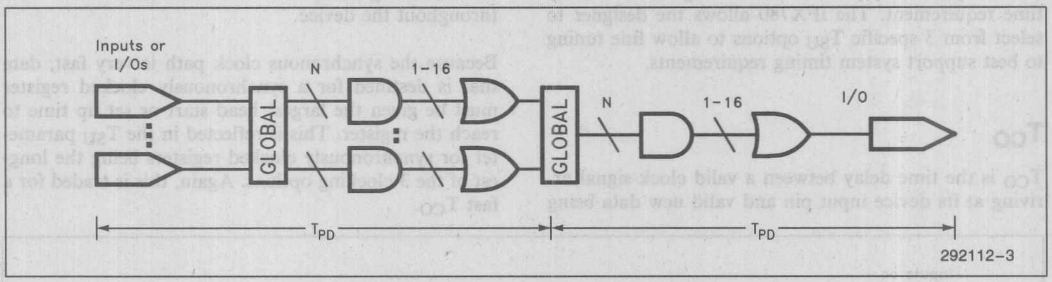

Figure 3. Product Term Cascading

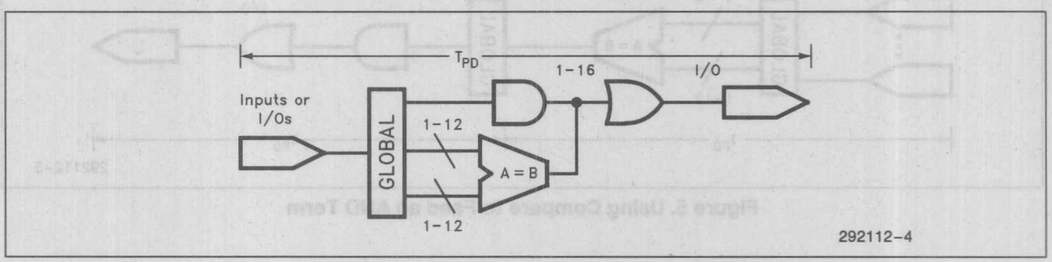

Figure 4. Compare Function Delay

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A design may require the result of the compare to be "AND"ed with other signals to generate the required output. This is most often encountered when using the compare output in the state-transition equations of a state machine. To accomplish this, a macrocell is used to feed the identity compare result onto the Global Interconnect Matrix. It can then be brought back into any CFB and "AND"ed with the required signals (see Figure 5). The pin-to-pin timing for this operation would be two times T_{PD}.

Signals fed into the identity compare logic are still available to all the macrocells in the CFB.

5.0 REGISTERED LOGIC TIMING

T_{SU}

T_{SU} is the time that valid data must be present on a device input pin before a clock signal can be applied to its device pin to latch the data into a device register. T_{SU} is the difference between the clock path delay and the data path delay plus the internal register data setup time requirement. The iFX780 allows the designer to select from 3 specific T_{SU} options to allow fine tuning to best support system timing requirements.

T_{CO}

T_{CO} is the time delay between a valid clock signal arriving at its device input pin and valid new data being available on a register's output pin. Each of the 3 T_{SU} timing options on the iFX780 has a corresponding T_{CO} parameter.

T_H

T_H is the time data must be held valid on a device pin after the rising edge of the clock has occurred on its respective device pin.

Clocking Options

Figure 6 shows the details of the 3 clocking options: Synchronous, Delayed-Synchronous and Asynchronous. With each of the options, signal inversion is selectable on a register basis. This allows for rising or falling edge clocking, resulting in finer timing control granularity.

Registers connected to either of the two device synchronous clock pins are optimized for minimum T_{CO} (Figure 6a). This is because the device synchronous clocks are routed globally via fast dedicated clock lines throughout the device.

Because the synchronous clock path is very fast, data that is destined for a synchronously clocked register must be given the largest head start or set up time to reach the register. This is reflected in the T_{SU} parameter for synchronously clocked registers being the longest of the 3 clocking options. Again, this is traded for a fast T_{CO}.

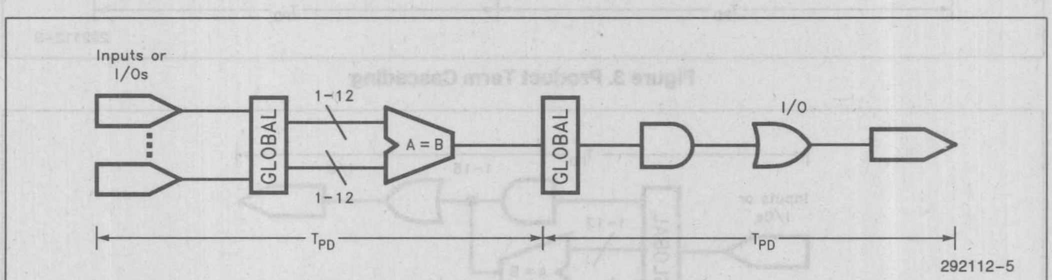
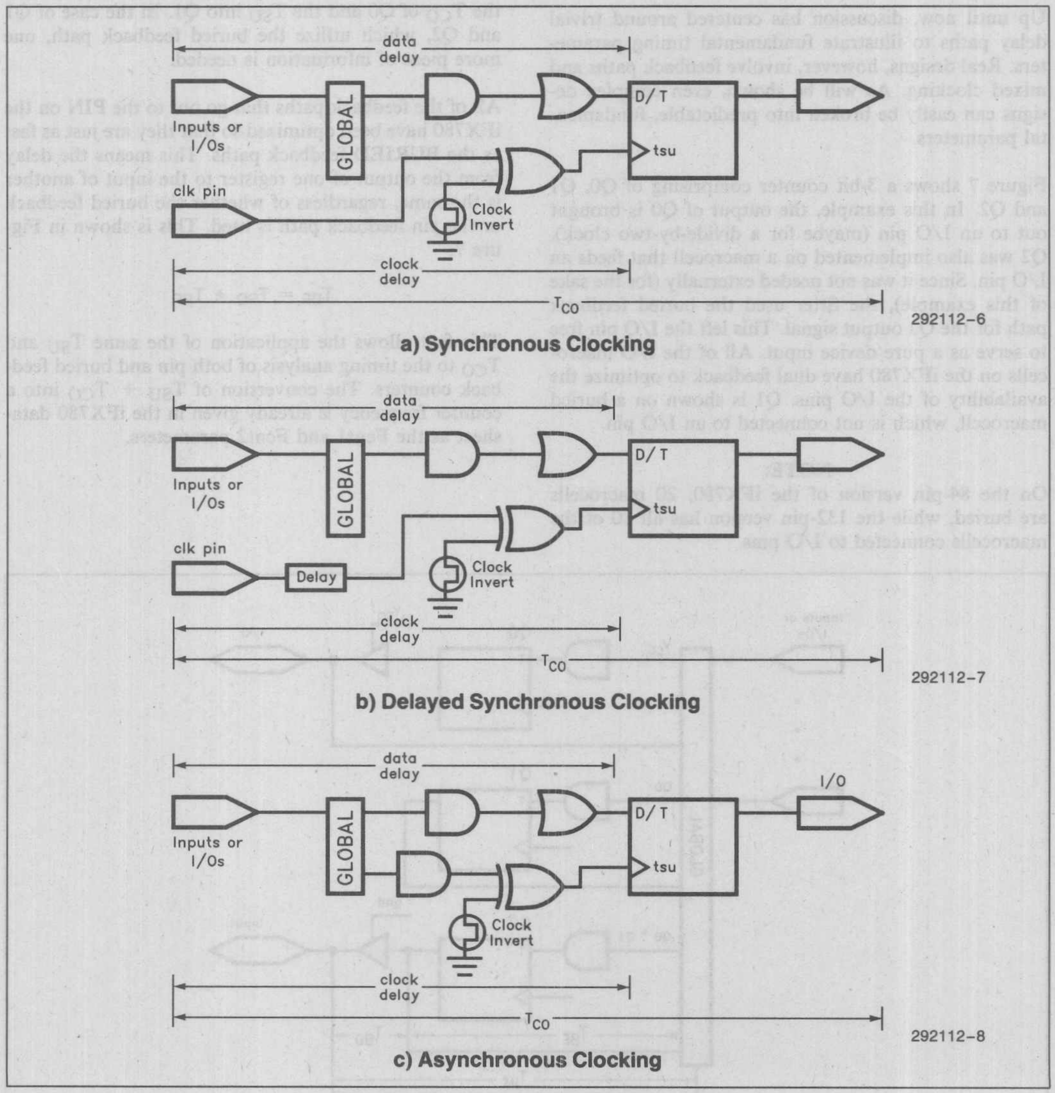


Figure 5. Using Compare to Feed an AND Term

The middle clocking option is the delayed-synchronous clock (Figure 6b). By selecting this option, a register receives a delayed version of one of the two device synchronous clocks. This reduces the head start that data requires to reach the register, which is reflected in a smaller T_{SU} value. This shorter setup time is traded for an increase in T_{CO} and the introduction of a short data hold time.

The fast or delayed version of the two global synchronous clocks is selected on a CFB basis.

For data signals that only allow for very short set up times to their clock signals, any of the locally developed asynchronous clocks may be used which are optimized for minimum T_{SU} (Figure 6c). The product-term-based asynchronous clock provides a clock delay path that matches the data delay path. This results in the minimum T_{SU} traded for an increase in T_{CO} and a data hold time consideration. Table 1 summarizes T_{SU} and T_{CO} for the 10 ns T_{PD} version of the iFX780.



a) Synchronous Clocking

b) Delayed Synchronous Clocking

c) Asynchronous Clocking

Figure 6. iFX780 Clocking Options

Each CFB has two product terms dedicated to develop two asynchronous clocks from any of the 24 signals that fan-in from the Global Interconnect Matrix. "AND" functions as well as pure "OR" functions may be used to develop an asynchronous clock, since the inversion available at the register may be used to implement DeMorgans inversion.

6.0 COUNTERS AND STATEMACHINES

Up until now, discussion has centered around trivial delay paths to illustrate fundamental timing parameters. Real designs, however, involve feedback paths and mixed clocking. As will be shown, even complex designs can easily be broken into predictable, fundamental parameters.

Figure 7 shows a 3-bit counter comprising of Q0, Q1 and Q2. In this example, the output of Q0 is brought out to an I/O pin (maybe for a divide-by-two clock). Q2 was also implemented on a macrocell that feeds an I/O pin. Since it was not needed externally (for the sake of this example), the fitter used the buried feedback path for the Q2 output signal. This left the I/O pin free to serve as a pure device input. All of the I/O macrocells on the iFX780 have dual feedback to optimize the availability of the I/O pins. Q1 is shown on a buried macrocell, which is not connected to an I/O pin.

NOTE:

On the 84-pin version of the iFX780, 20 macrocells are buried, while the 132-pin version has all 80 of the macrocells connected to I/O pins.

	T_{SU}	T_H	T_{CO}
Synchronous	6.5 ns	0 ns	6 ns
Delayed Sync	5 ns	2 ns	8 ns
Asynchronous	2 ns	5 ns	12 ns

In determining the maximum operating frequency of this counter, T_{SU} and T_{CO} must be considered for the specific clock option chosen to run the counter. The timing associated with Q0 feeding back to Q1 is simply the T_{CO} of Q0 and the T_{SU} into Q1. In the case of Q1 and Q2, which utilize the buried feedback path, one more piece of information is needed.

All of the feedback paths that go out to the PIN on the iFX780 have been optimized so that they are just as fast as the BURIED feedback paths. This means the delay from the output of one register to the input of another is the same, regardless of whether the buried feedback or the pin feedback path is used. This is shown in Figure 7:

$$T_{BF} = T_{BD} + T_{PF}$$

This fact allows the application of the same T_{SU} and T_{CO} to the timing analysis of both pin and buried feedback counters. The conversion of T_{SU} + T_{CO} into a counter frequency is already given in the iFX780 datasheet as the Fcnt1 and Fcnt2 parameters.

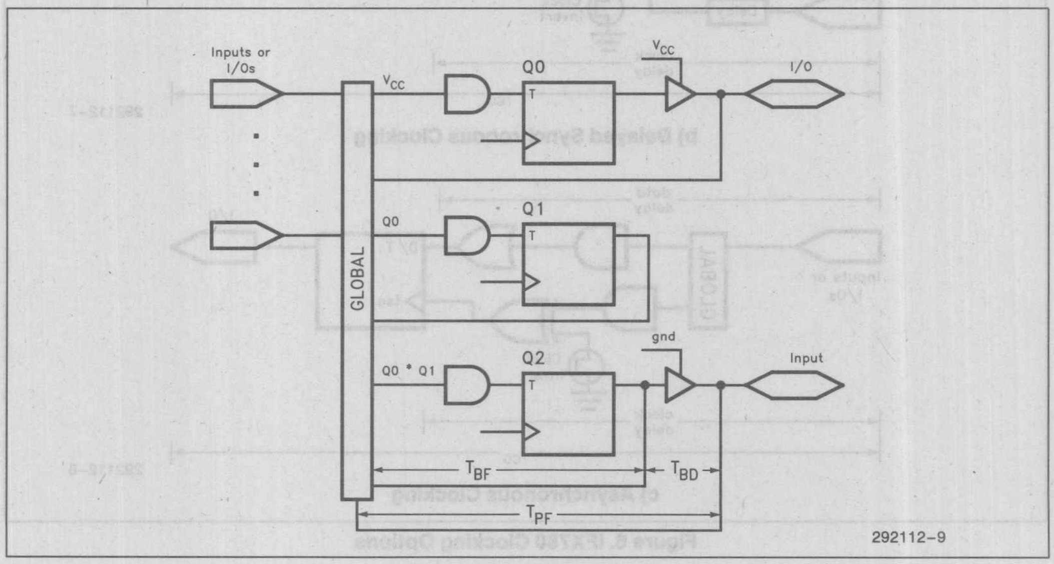


Figure 7. 3-Bit Counter

Fcnt1 and Fcnt2

Traditionally, programmable logic performance is specified both for pin/external feedback counters (which reflects system level performance), as well as buried-feedback counters. The parameter Fcnt1 describes a pin-feedback counter and is defined by the equation:

$$\text{Fcnt1} = 1/(T_{SU} + T_{CO})$$

Fcnt2 is applicable to buried counters and is defined as:

$$\text{Fcnt2} = 1/(T_{BF} + t_{SU})$$

where T_{BF} = buried feedback delay and t_{SU} (small "t") = internal register setup time requirement.

In the iFX780:

$$\text{Fcnt1} = \text{Fcnt2}$$

which reflects the feedback path delay independence.

Each of the three clocking modes: Synchronous, Delayed Synchronous and Asynchronous, have different Fcnt values. This is dictated by their differences in T_{SU} and T_{CO} timing.

Fcnt1 and Fcnt2 also describe the performance of state machines that require 16 or less product terms to implement their next-state decode logic. The majority of state machine designs fall into this category. If a given state machine decode logic is so complex that it requires more than 16 product terms, a technique similar to that shown in Figure 3 can be used to serially distribute the logic over two macrocells. In this case, the timing for this modified Fcnt (called Fcnt') would be described by:

$$\text{Fcnt}' = 1/(T_{SU} + T_{CO} + T_{PD})$$

Mixed Mode Clocking

It is often desirable in datapath, bridging and other applications to clock data in and out of the iFX780 using different clocks or clocking options along the internal device dataflow. An example would be where a short data setup time was given on the input, while a fast clock-to-output was required on the output side. One of the asynchronous clocks on the iFX780 could be used on the input register (optimized for a short T_{SU}), while one of the synchronous clocks could be used for the output register (optimized for a short T_{CO}), as shown in Figure 8.

In determining the timing associated with this design, the feedback symmetry on the iFX780 makes the analysis trivial. The minimum clock window (maximum frequency) a register string requires to pass data through the logic array between them (16 product terms or less), is defined by:

$$T_{MIN} = T_{CO}\ (\text{Source}) + T_{SU}\ (\text{Dest})$$

where the delay of the source register T_{CO} is added to the destination register T_{SU}. For the example in Figure 8:

$$T_{MIN} = T_{CO}\ (\text{Async}) + T_{SU}\ (\text{Sync})$$

For very complex functions requiring two passes through the logic array, the minimum clock window becomes:

$$T_{MIN} = T_{CO}\ (\text{Source}) + T_{PD} + T_{SU}\ (\text{Dest})$$

CFB Placement

Up until now, no mention has been made of the dependence of timing on the distribution of CFBs into which macrocells get placed into. This is because there is none! Counters, statemachines, datapaths and combinatorial circuits may be implemented in macrocells distributed across the iFX780, and the timing is the same as if they resided in a single CFB. So timing is not only predictable, it is symmetrical as well.

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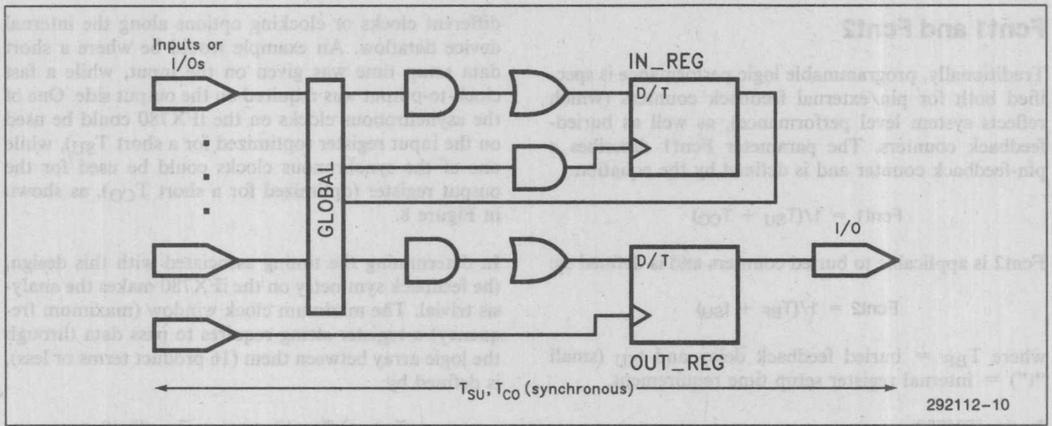

Figure 8. Mixed Clocking Register Pipeline

APPLICATION BRIEF

Overview of In-Circuit Reconfiguration and Programming for the FLEXlogic iFX780 and iFX740

3

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APPLICATIONS ENGINEERING
PROGRAMMABLE LOGIC DEVICES

November 1993

Overview of In-Circuit Reconfiguration and Programming for the FLEXlogic iFX780 and iFX740

CONTENTS PAGE

1.0 INTRODUCTION

This Application Brief describes the In-Circuit Reconfiguration and Programming features of the Intel FLEXlogic iFX780 and iFX740 FPGAs.

The Intel FLEXlogic FPGA family offers all of the advantages of both SRAM and PROM based architectures. Because FLEXlogic FPGAs utilize an SRAM based architecture they provide the flexibility of unlimited reconfiguration for fast prototyping of new designs. This feature also supports applications that require configurations to be dynamically changed after the system is powered up.

Unlike traditional SRAM based FPGAs, Intel's FLEXlogic family also provides built-in nonvolatile cells so that an external PROM device is not required for initialization. The contents of the built-in nonvolatile cells are automatically loaded into the SRAM architecture upon power-up and then disabled in order to reduce power consumption. The availability of both SRAM and nonvolatile cells in one device allows the designer to choose either the ease of use and security of nonvolatile operation or the flexibility of SRAM reconfiguration.

2.0 JTAG INTERFACE

The Intel FLEXlogic FPGA family utilizes an industry standard JTAG/IEEE 1149.1 interface to support in-circuit reconfiguration and programming. The JTAG/IEEE 1149.1 Boundary Scan Standard plays a key role in reducing the total cost of a product, shortening the time to market, and improving product quality.

The most common application for boundary scan is for fast and efficient identification of assembly errors during the manufacturing stage of a product. Connections to all JTAG compliant devices can be checked for opens, shorts, and bridging faults without the use of expensive bed of nails testers. For example, a continuity test may be performed between two JTAG devices on a circuit board by placing a known value on the output pins of one device while observing the input pins of the other device.

In addition to the standard boundary scan operations, the Intel iFX780 and iFX740 also supports optional test capabilities that allow on-chip debug of a design while in-circuit. These capabilities can significantly reduce the time required for prototyping new designs and may decrease the need for extensive design simulations.

Another benefit of utilizing simplified boundary scan methods is that the time required to generate production test software is significantly shortened. This advantage combined with a reduction in prototype debug time can dramatically improve the overall time to market for a new product.

Instead of carrying inventory of preprogrammed FPGAs and incurring the risk that a device with the incorrect pattern will be inserted in a given location, blank FPGAs can be assembled in all locations on the board design. Then the board level tester can program the FPGAs according to their location and the board configuration required.

The iFX780 and iFX740 boundary scan support consists of an Instruction Register, a Data Register, scan cells, and associated logic which are accessed through the Test Access Port (TAP). The TAP interface consists of three inputs (TDI, TCK and TMS) and one output (TDO). All TAP connections must be dedicated to the component. The functions of these pins are described in Table 1.

Table 1. JTAG Pin Descriptions

Pin	Description
TDI	The Testability Data Input is the boundary scan serial data input to the iFX780 and iFX740. JTAG instructions and data are shifted into the iFX780 and iFX740 on the TDI input pin on the rising edge of TCK.
TDO	The Testability Data Output is the boundary scan serial data output from the iFX780 and iFX740. JTAG instructions and data are shifted out of the iFX780 and iFX740 on the TDO output on the falling edge of TCK.
TCK	The Testability Clock Input provides the boundary scan clock for the iFX780 and iFX740. TCK is used to clock state information and data into and out of the iFX780 and iFX740 during boundary scan or programming modes. The maximum operating frequency of the boundary scan test clock is 8 MHz.
TMS	The Testability Control Input is the boundary scan test mode select for the iFX780 and iFX740.

The boundary scan cells of the iFX780 and iFX740 are linked to form a shift register chain for all active pins. This chain provides a path which can be used to shift in test stimulus as well as shift out test response data for inspection.

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Standard boundary scan functions such as EXTEST, SAMPLE/PRELOAD, BYPASS, and IDCODE are supported. With these functions users can capture internal logic values, drive device pins to a preset value, and identify a device electronically within a chain. In addition to the standard boundary scan instructions, custom functions are also provided that support detailed device testing and debug. The public JTAG instructions supported by the iFX780 and iFX740 are listed in Table 2.

Table 2. JTAG Public Instructions

Instruction	Description
EXTEST	Drive the output pins with pre-loaded data
SAMPLE/ PRELOAD	Read current pin state/Pre-load next in state
IDCODE	Read Manufacturers ID code
LDVECT	Load Vector into Program shift register
FREAD	Read the nonvolatile cells
SWRITE	SRAM Write
SREAD	SRAM Read
FPGM	Write (program) the nonvolatile cells
HI-Z	3-State all outputs
UESCODE	Shift out UES bits
ISCAN	Internal Scan of Macrocell registers
BYPASS	Allows data to pass through to the next device in the chain

In order to facilitate the development of boundary scan test programs, the BSDL (Boundary Scan Description Language) files for the iFX780 and iFX740 are supplied by Intel. These BSDL files provide details on the testability features of the iFX780 and iFX740 FPGAs:

I780_132.BSD for the iFX780, 132 pin package

I780_84.BSD for the iFX780, 84 pin package

I780_68.BSD for the iFX740, 68 pin package

I780_44.BSD for the iFX740, 44 pin package

The BSDL files can be obtained either through the Intel Bulletin Board or by calling the Intel Hotline.

3.0 PHYSICAL CONNECTIONS

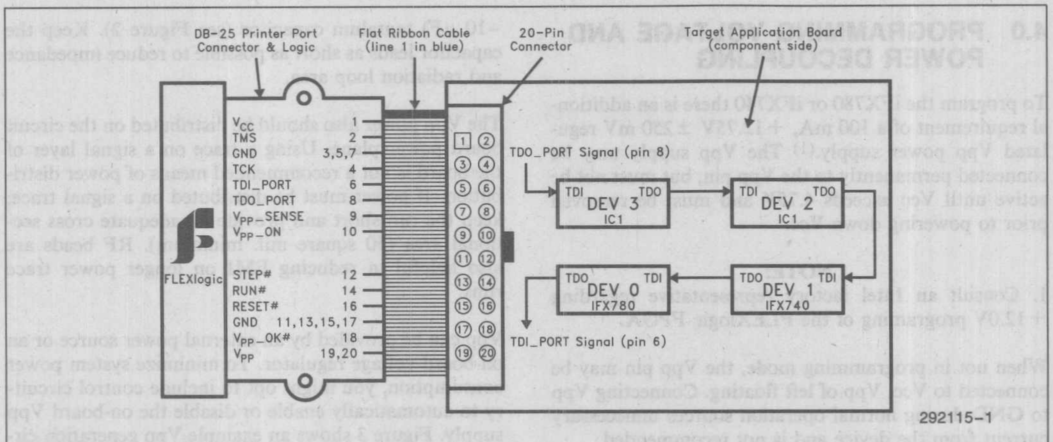
The most convenient method of supporting in-circuit reconfiguration or programming with the iFX780 and iFX740 is to use the FLEXlogic Prototyping Cable Kit which provides a connection between a PC parallel port and the target application board. The cable allows the PC parallel port to act as a TAP controller for all of the devices in the JTAG chain.

The cable supplied in the Intel FLEXlogic Prototyping Cable Kit consists of a male DB-25 connector, circuit board and a flat ribbon cable ending in a female 20-pin connector. The circuit board is housed in the DB-25 connector sheel and contains an integrated line driver. The cable supports the four TAP interface signals (TDI, TDO, TCK and TMS) plus some additional signals useful for debug (STEP, RUN, and RESET).

FLEXlogic Prototyping Cable Installation

The Prototyping Cable connects between a PC parallel port and a male 20-pin connector mounted on the target application board. For a single iFX780 or iFX740, the PC cable TAP interface signals connect directly to the appropriate pins on the FPGA. For multiple FLEXlogic FPGAs, the JTAG TDI and TDO signals are connected in a "daisy chain." In this case, the TDO_PORT from the cable connects to the "last" logical device (first physical device) in the chain. In turn this device's TDO pin connects to the next logic device's TDI pin, and so forth. The chain is completed by connecting to TDO pin of the "first" logical device (DEV 0) to the TDI_PORT on the cable connector (see Figure 1). The TMS and TCK cable signals connect directly to the corresponding TMS and TCK pins on each device in the JTAG chain.

In addition to the TAP interface signals and power connections, the Vcco0 pin must be connected to a +5V or +3.3V source to power the JTAG TDO driver circuitry within the FPGA.



NOTES:
1. VPP_SENSE, STEP# and RUN# are reserved for future use.
2. Pins 19 & 20 are reserved for VPP when used with the FLEXlogic Evaluation Board

Figure 1. Physical Connections for the iFX780

FLEXlogic Prototype Cable Signals

The functions of the FLEXlogic Prototype Cable signals are described in Table 3.

Table 3. FLEXlogic Prototype Cable Signals

Signal	Pin	Description
V_{CC}	1	+5V ± 250 mV must be supplied by the target application circuit. This supplies power to the cable line driver located in the shell of the DB-25 connector.
TMS	2	JTAG Testability Control signal provided by the JTAG software; connect to the TMS pin of each device on the JTAG chain.
GND	3, 5, 7, 11, 13, 15, 17	Connect ALL GND lines to ground to reduce noise.
TCK	4	JTAG Testability Clock signal provided by JTAG software; connect to the TCK pin of each device in the JTAG chain.
TDI_PORT	6	JTAG Testability Data Input; connect to TDO pin of "first" logical device in JTAG chain.
TDO_PORT	8	JTAG Testability Data Output, connect to TDI pin of "last" logical device in JTAG chain.
VPP_SENSE	9	(Optional) Reserved for future use.
VPP_ON	10	(Optional) Active high signal, provided by JTAG software, to activate on-board Vpp power source.
STEP#	12	(Optional) Active low debug signal reserved for future use.
RUN#	14	(Optional) Active low debug signal reserved for future use.
RESET#	16	(Optional) Active low signal provided by the JED2JTAG software. This signal is driven low during device reconfiguration. The PENGN program does not activate this signal.
VPP_OK#	18	An active low signal checked by JTAG software prior to device programming. Tie this signal low if an external Vpp source is used.
VPP	19, 20	A + 12.75V ±250 mV programming voltage supplied by FLEXlogic Evaluation Board or external supply. The FLEXlogic prototyping cable, attached to the PC, DOES NOT supply the programming voltage. *Permanent device damage may occur if Vpp exceeds 13.5V.*

4.0 PROGRAMMING VOLTAGE AND POWER DECOUPLING

To program the iFX780 or iFX740 there is an additional requirement of a 100 mA, +12.75V ±250 mV regulated Vpp power supply.(1) The Vpp supply may be connected permanently to the Vpp pin, but must not be active until Vcc exceeds 4.75V and must be removed prior to powering down Vcc.

NOTE:

1. Consult an Intel factory representative regarding +12.0V programing of the FLEXlogic FPGA.

When not in programming mode, the Vpp pin may be connected to Vcc, Vpp of left floating. Connecting Vpp to GND during normal operation sources unnecessary current from the device and is not recommended.

Good decoupling practices should be followed for all designs using Intel PLDs and FPGAs. This will help reduce susceptibility to noise and voltage overshoot. Vpp must be decoupled with a 0.1 μF ceramic capacitor at the Vpp pin of each FPGA device. In addition, it is recommended to decouple Vpp at the board entry point with **both** a 0.1 μF capacitor and a larger (1 μF −10 μF) tantalum capacitor (see Figure 2). Keep the capacitor leads as short as possible to reduce impedance and radiation loop area.

The Vpp power also should be distributed on the circuit board power plane. Using a trace on a signal layer of the board is not a recommended means of power distribution. If power must be distributed on a signal trace; keep the run short and provide an adequate cross sectional area (50 square mil. minimum). RF beads are also helpful in reducing EMI on longer power trace runs.

Vpp can be provided by an external power source or an on-board voltage regulator. To minimize system power consumption, you might opt to include control circuitry to automatically enable or disable the on-board Vpp supply. Figure 3 shows an example Vpp generation circuit using a linear step down voltage regulator with ON/OFF control capability.

Figure 4 shows an example Vpp generation circuit using a linear step up voltage regulator with ON/OFF control capability. When using a step up regulator, you must accurately set the biasing resistor R1 to maintain the output voltage within the specified range.

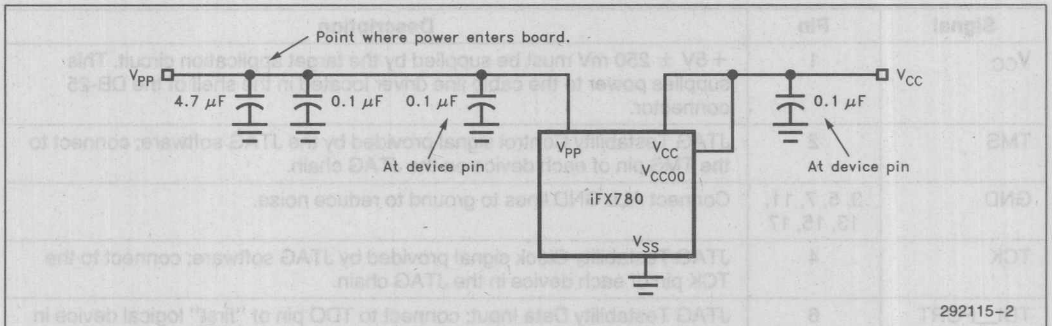
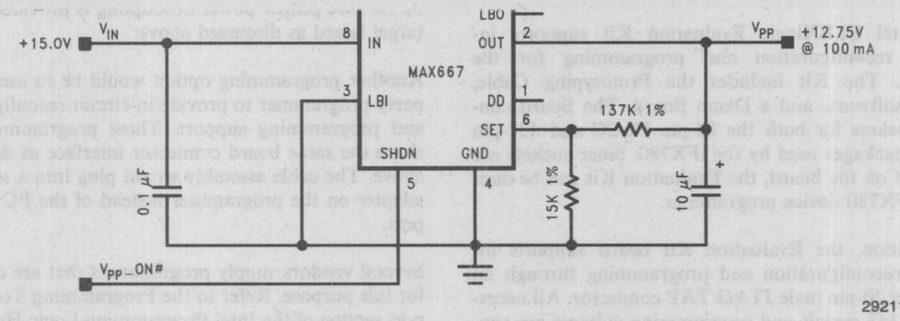
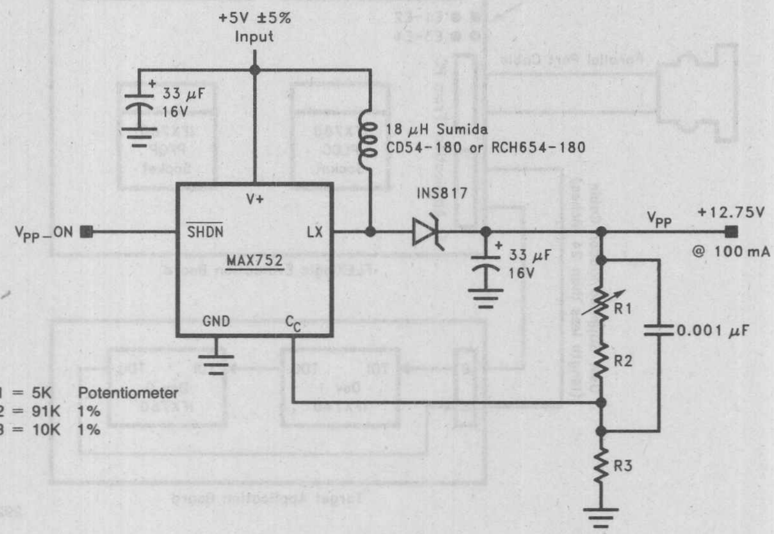


FIGURE 2. Vpp Power Decoupling



NOTE:
When the VPP__ON signal is activated, the Maxim 667 switching regulator produces +12.75V. This circuit is used on the FLEXlogic Evaluation Board and is just one example of a Vpp supply.

FIGURE 3. Basic Step Down Vpp Voltage Supply with ON/OFF control.



NOTE:
When the VPP__ON signal is activated, the Maxim 752 switching regulator produces +12.75V. This is just one example of a Vpp supply.

Figure 4. Basic Step Up Vpp Voltage Supply with ON/OFF Control

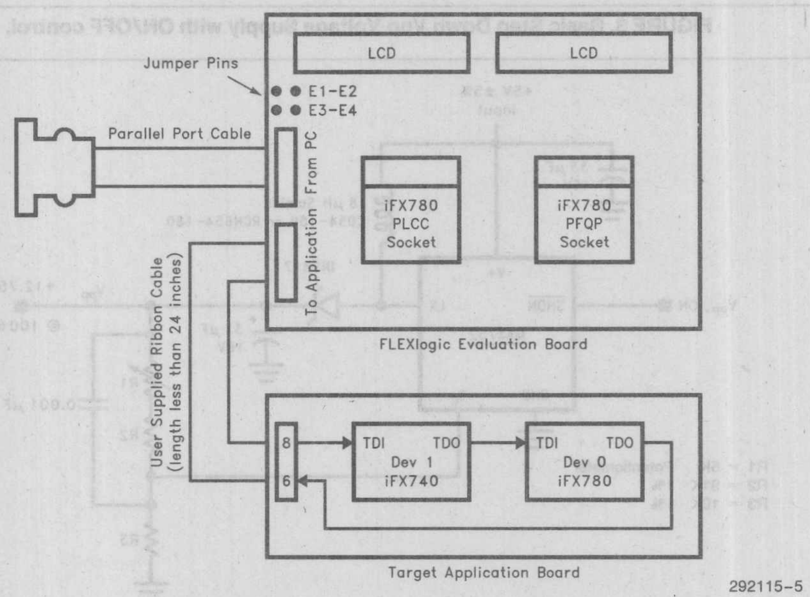
5.0 PROGRAMMER SUPPORT

The Intel FLEXlogic Evaluation Kit supports in-circuit reconfiguration and programming for the iFX780. The Kit includes the Prototyping Cable, JTAG software, and a Demo Board. The Board contains sockets for both the 84-pin PLCC and 132-pin PQFP packages used by the iFX780. Since sockets are supplied on the board, the Evaluation Kit can be used as an iFX780 device programmer.

In addition, the Evaluation Kit board supports in-circuit reconfiguration and programming through an auxiliary 20-pin male JTAG TAP connector. All necessary JTAG signals and programming voltages are supplied through the auxiliary connector. A cable connected from the auxiliary connector can supply these signals to the target application circuit board (see Figure 5). Be sure proper power decoupling is provided on the target board as discussed above.

Another programming option would be to use a third party programmer to provide in-circuit reconfiguration and programming support. These programmers may share the same board connector interface as described above. The cable assembly would plug into a socket or adapter on the programmer instead of the PC parallel port.

Several vendors supply programmers that are designed for this purpose. Refer to the Programming Tools Support section of the Intel Programming Logic Handbook (order number 296083) for a list of supported vendors.



NOTE:
When using this configuration, make sure no FPGA devices are installed in the FLEXlogic Evaluation Board sockets and remove any jumpers on Board pins E1–E2 and E3–E4.

Figure 5. Using the FLEXlogic Evaluation Board for In-Circuit Reconfiguration and Programming.

6.0 JTAG SOFTWARE TOOLS SUPPORT

Intel's PLDshell Plus software includes support for in-circuit reconfiguration and programming of the iFX780 and iFX740 FPGAs. This software is an easy-to-use tool that supports design entry, fitting and functional simulation of Intel PLD and FLEXlogic FPGA applications. Once an FPGA design is completed it may be downloaded to the iFX780 or iFX740 through either a reconfiguration or programming operation.

The JTAG software, PENGN, included in PLDshell Plus, supports either downloading to or reading from the SRAM cells as well as programming or verifying the nonvolatile cells of a single FPGA within a JTAG chain.

Also available from Intel is a dynamic in-circuit reconfiguration tool, JED2JTAG. Automatic support is provided for multiple iFX780s and iFX740s and allows the user to combine the Intel FPGAs with other JTAG devices in a chain.

7.0 RECONFIGURATION EXAMPLE

This section overviews a typical reconfiguration operation using PLDshell and the FLEXlogic Prototyping Cable. Additional details of the reconfiguration processor are available in the PLDshell Plus documentation, FLEXlogic Prototype Cable Interface User's Manual and Application Note AP-390 titled "JTAG 1149.1 Specifications for In-Circuit Reconfiguration and Programming the iFX780 FPGA".

Using the PENGN Program

The program PENGN is used to reconfigure the iFX780 and iFX740 using the Prototyping Cable. The PENGN executable file (PENGN.EXE) is found on the JTAG software diskette included with the FLEXlogic Prototyping Cable Kit or is available on the Intel's application BBS.

The reconfiguration operation using PENGN includes the following steps:

a) Enter the design using either PLDshell Plus or a third party tool and generate a JEDEC file.

b) Connect the download cable between the PC parallel port and the connector on the target application board.

c) Check that the Vcc power supply for the target board is on.

d) At a DOS prompt or PLDshell Run Menu invoke the JTAG software reconfiguration command to down load the bitmap to the FLEXlogic FPGA. Below is the command to configure the SRAM of a 132 pin iFX780 with the JEDEC file (filename.JED).

A full description of the PENGN options are available in the FLEXlogic Prototype Cable User's Manual.

This process may be repeated as many times as desired.

```
C:> pengn -loc 0 -port 1 -part fx780_132 -ps -v filename.jed
```

Using the JED2JTAG Program

The JED2JTAG software also supports in-circuit reconfiguration of a single or multiple iFX780 or iFX740 device in a JTAG chain.

The reconfiguration operation using JED2JTAG includes the following steps:

a) Enter the design using either PLDshell Plus or a third party tool and generate a JEDEC file.

b) Create a .SDL file describing the circuit chain.

```
|FILE: example.sdl -Describes the chain shown in Figure 5
{
|           Port_Num Port_Type
STRING      1        PARALLEL_PORT

|           Loc  Ref Device        JEDEC File
DEVICE      0    U3  FX780_132     780JEDEC.JED
DEVICE      1    U4  FX740_68      740JEDEC.JED
}
```

A "|" indicates a comment line.

c) Connect the download cable between the PC parallel port and the connector on the target application board.

d) Check that the Vcc power supply for the target board is on.

e) At a DOS prompt or PLDshell Run Menu invoke the JED2JTAG software to down load the bitmap to the FLEXlogic FPGA. The following command uses the .SDL file, example.SDL, and reconfigures both FPGAs in the chain.

```
C:> jed2jtag example
```

This process may be repeated as many times as desired.

8.0 PROGRAMMING EXAMPLE

The differences between a reconfiguration operation and a programming operation are:

- The PENGN program command is used instead of the reconfigure command.
- A Vpp supply (+12.75V ± 250 mV) must be provided to the target device and should be switched on after the Vcc supply is stable. The Vpp supply should also be removed before the Vcc supply is powered down. The Prototyping Cable includes the Vpp control signal (VPP_ON) to automatically enable and disable Vpp for the target application.
- If using the Intel FLEXlogic Evaluation Board, Vpp is supplied through pins 19 and 20 of the auxiliary connector.
- For the iFX780 and iFX740 programming may only be performed one time.

The programming operation using the PENGN program includes the following steps:

a) Enter the design using either PLDshell Plus or a third party tool and generate a JEDEC file.

b) Connect the download cable between the PC parallel port and the connector on the target board.

c) Check that the Vcc power supply for the target board is on.

d) Turn on the Vpp power supply. *DO NOT "hot plug" Vpp or permanent ESD damage may occur to the FPGA.* If using a cable from the FLEXlogic Evaluation Board, Vpp is automatically controlled.

e) At a DOS prompt or PLDshell Run Menu invoke the JTAG software program command to down load the bitmap to the nonvolatile cells in the FLEXlogic FPGA. Below is the command to configure the EPROM of a 132 pin iFX780 with the JEDEC file (filename.JED).

```
C:> pengn -loc 0 -port 1 -part fx780_132 -pe -v filename.jed
```

This process may only be performed one time.

9.0 ORDERING INFORMATION

For Intel Literature call (800) 548-4725. Outside of the USA/Canada, please contact your local Intel sales. office.

Application notes are also available through the Intel FAXback system by calling (800) 628-2283. Outside the USA, please call (916)356-3105 or 44 (0) 793-496 646 (Europe).

"JTAG 1149.1 Specifications for In-Circuit Reconfiguration and Programming the iFX780 FPGA," Application Note 390, Order Number 292122-001.

This App-Note contains detailed JTAG timing, and shows how to build JTAG instruction streams from the FLEXlogic bitmaps.

"Designing FLEXlogic Loader Circuits," Application Brief 398, Order Number 292120-001

This App-Brief contains detailed information on the use of JED2JTAG, and shows how to build a JTAG loader circuit.

Intel Programmable Logic Handbook

—Order Number 296083

PLDshell Plus Software, *Free* of Charge

—Order Number 611942

FLEXlogic Prototyping Cable Kit

The JTAG software version 1.1 includes the JED2JTAG and PENGN programs

—Consult your local Intel sales office or authorized distributor

FLEXlogic Evaluation Kit

Includes the FLEXlogic Prototyping Cable Kit and Evaluation Board

—Consult your local Intel sales office or authorized distributor

Intel's Application BBS

(916)356-3600 (USA) or 44 (0) 793-496 340 (Europe)
Settings: 8 bits, No parity, 1 Stop bit, upto 14,400 baud.

The FLEXlogic Prototype Cable Kit software and BSDL files can be downloaded from the BBS. Follow all directions to download from the PLD/FPGA file area.

APPLICATION BRIEF

Using FLEXlogic iFX780 and iFX740 Features with PLDshell Plus

RICHARD VIREDAY
SOFTWARE DEVELOPMENT TOOLS
PROGRAMMABLE LOGIC DEVICES

October 1993

Order Number: 292120-001

Using FLEXlogic iFX780 and iFX740 Features with PLDshell Plus

CONTENTS PAGE

3

1.0 INTRODUCTION

This Application Brief details how to use some of the Intel FLEXlogic iFX780 and iFX740 features, and the PDS language notations necessary to use them.

The information here supplements that in the PLDshell Plus R3.X User's Guide.

2.0 MACROCELL CONTROLS

An FPGA logic macrocell has available to it a variety of controls and configurations. Each macrocell can choose:

1) Any of 4 clock signals. These are the two synchronous clock pins, and the CFB .ACLK pterms.
2) Each macrocell can invert the clock signal it uses, so that it can take the falling edge of a clock pulse, rather than the rising. Either of the two synchronous clock pins can be delayed, but on a CFB basis only. (See the Delay Clock section below.)
3) Any of 4 Output Enable Conditions. These are V_{CC}, GND, or the two CFB OE pterms.
4) Either of the C/P1 or C/P2 pterms can be used by the macrocell as a Clear or Preset.
5) Inversion of OE, and C/P is available on the CFB product terms only. Only the Clock signals are inverted in the macrocell.

To use the product terms, the PLDshell Plus fitter does a pattern match of pterm that use these control signals. Different macrocells, if they have the same OE, Clear, Clock, etc., pterms will share the same pterms in the CFB. The OE and C/P signals must have the same polarity for the PLDshell Plus fitter to match them. The report file shows the final equations placed into each CFB product term.

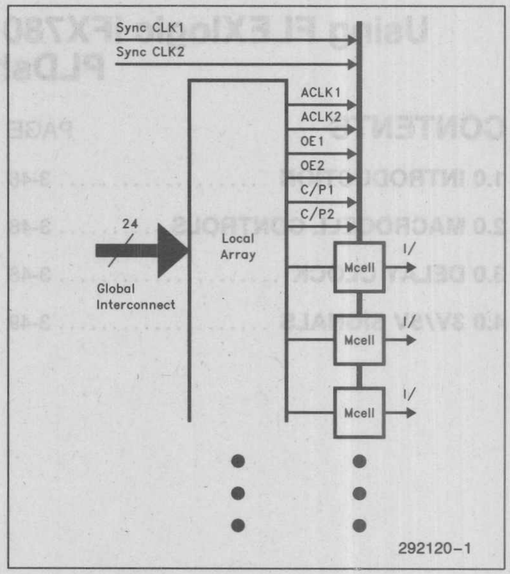


Figure 1. CFB Control Signals

3.0 DELAY CLOCK

Either of the two synchronous clock pins can be delayed, but on a CFB basis only. What the delay clock creates is a change in the T_{SU} and T_H A.C. Timings. The iFX780 and iFX740 Datasheet shows each of the changes.

To specify a delay clock, use the DELAYCLK attribute on the Output pins that require it. The Sync. Clock signal that feeds the CFB will then be Delayed for all the signals in that CFB. The fitter will not allow mixed delay/non-delay modes of a clock signal in the CFB.

DELAYCLK Example

```
PIN CLK
PIN OUTX REG DELAYCLK
PIN OUTY REG

EQUATIONS

OUTX.CLKF = CLK ; delayed
OUTY.CLKF = CLK ; non-delayed
```

4.0 3V/5V SIGNALS

Using the 3VOLT and 5VOLT keywords, the outputs of a design can be partitioned automatically by PLDshell Plus. This can be useful for mixed 3.3V and 5V systems.

Individual pins are denoted with a specific voltage. The PLDshell Plus fitter will then group similar voltage output signals together with the same V_{CC} supply pins.

Voltage Examples

```
PIN CLK 3VOLT
PIN LDLHA 3VOLT ; CPU status
PIN OUTX REG 3VOLT
PIN OUTY REG 5VOLT
PIN OUTZ REG ; default of 5VOLT
```

To specify a system with only 3.3V I/Os use the OPTIONS selection.

```
OPTIONS
  DEFAULT_VCC = 3VOLT
```

All I/Os for this design will now be considered as 3VOLT.

The Sync. Clock pins can also be 3V as well.

5.0 CMOS PULLUPS

The iFX780 and iFX740 have special signal pullups on inputs and I/Os to help with CMOS signals. These are controlled by the CMOS_LEVEL and TTL_LEVEL keywords. The Pullups should only be set as shown

5VOLT CMOS Signals

```
PIN IN1 5VOLT CMOS_LEVEL
```

3.3VOLT CMOS Signals

```
PIN IN2 3VOLT
PIN IN3 3VOLT TTL_LEVEL
PIN IN4 3VOLT ; ICC draw
```

Pin IN1 must have the pullup set. 5V CMOS signals will be pulled up internally.

Pins IN2 and IN3 are equivalent, and the iFX780 and iFX740 will not set the pullup for these.

No pins should be set as IN4 is shown, otherwise the I_{CC} standby power draw will be increased.

6.0 BURIED SIGNALS

Buried signals can be specified by either using the NODE keyword in the pin declarations, or by setting the OE (.TRST) signal of an output to GND.

```
NODE BUF_X
PIN BUR_Y
NODE XBURIED RAM

EQUATIONS
Y.TRST = GND
```

BUR_X and BUR_Y above are both buried signals, and will not use an I/O pin resource.

For SRAM signals, use the NODE keyword, and do not specify the SRAM.TRST equation.

7.0 DEFAULT OPTIONS

The default options for PLDshell Plus R3.X are:

```
OPTIONS
  INPUT_LEVEL = TTL_LEVEL
  DEFAULT_VCC = 5VOLT
  SECURITY = OFF
```

All inputs and I/Os are assumed to be 5V TTL level, unless the defaults are changed accordingly.

8.0 MEMORY AND CONFIGURATION

On some DOS machines, there may be a conflict with the extended memory manager used by PLDshell Plus. Run the "MEMCHK" utility included with PLDshell Plus to verify that at least 2 Mb of extended memory is available.

See the READ.ME file included in the release for further details.

If there are hardware configuration problems that you are unable to resolve, run the "CFGINF.BAT" file in the PLDshell area. This will create a file called "CONFIG.INF" which may then be faxed to the Hotline for further work. Do not forget to fill in your name and other machine information.

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AB-55

APPLICATION BRIEF

How to Use Registered SRAM Macrocells on the FLEXlogic iFX780 and iFX740 via PLDshell Plus Keywords

RICHARD VIREDAY
SOFTWARE DEVELOPMENT TOOLS
PROGRAMMABLE LOGIC DEVICES

October 1993

Order Number: 292121-001

How to Use Registered SRAM Macrocells on the FLEXlogic iFX780 and iFX740 via PLDshell Plus Keywords

CONTENTS PAGE

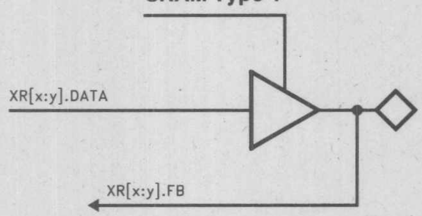
1.0 INTRODUCTION

This Application Brief shows how to use the Macrocells Registers in CFBs configured as SRAMs on the Intel FLEXlogic iFX780 and iFX740 FPGA. The information contained here is in addition to that in the PLDshell Plus 3.X User's Guide.

2.0 REGISTERED SRAM MACROCELL

All configurations shown, are also applicable to standard logic macrocells on the iFX780 and iFX740.

SRAM Type 1



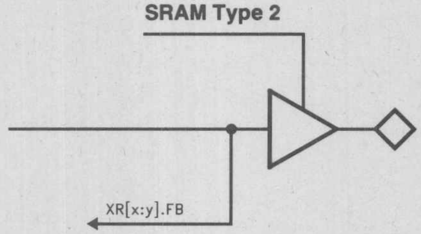
292121-1

```
PIN XR[x:y] RAM
PIN XR[x:y] RAM COMB PINFBK
; COMB and PINFBK are the defaults
; if not specified
```

SRAM Type 1 configurations are the default when the RAM keyword is used. This is currently the only SRAM type supported by Simulation in PLDshell Plus 3.X.

All SRAM control signals work as specified in the iFX780 and iFX740 datasheet.

SRAM Type 2

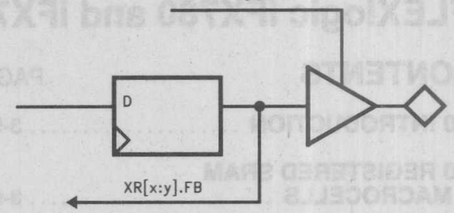


292121-2

```
PIN XR[x:y] RAM COMB CMBFBK
```

SRAM Type 2 uses the internal feedback path instead of the pin I/O path. The SRAM $\overline{BE}$ signal still controls when the .FB is active.

SRAM Type 3



292121-3

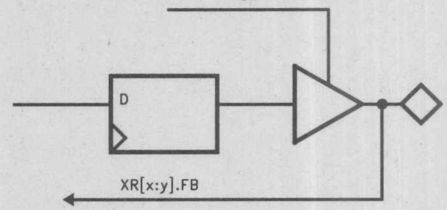
```
PIN XR[x:y] RAM REG REGFBK
```

SRAM Type 3 sets the macrocell to a D flip-flop. The REGFBK(1) keyword is optional.

NOTE:

1. TREGFBK can be used anywhere REGFBK is used to set a T-FF instead.

SRAM Type 4

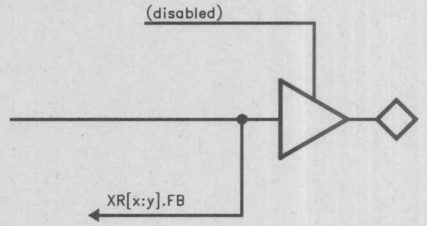


292121-4

```
PIN XR[x:y] RAM REG PINFBK
```

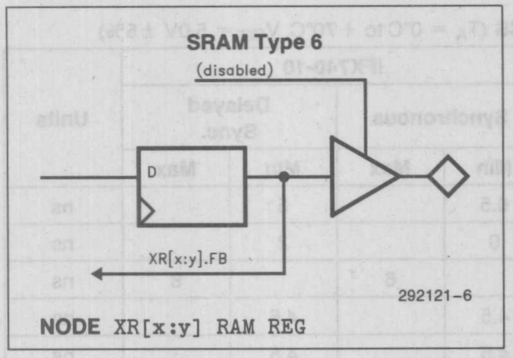
SRAM Type 5

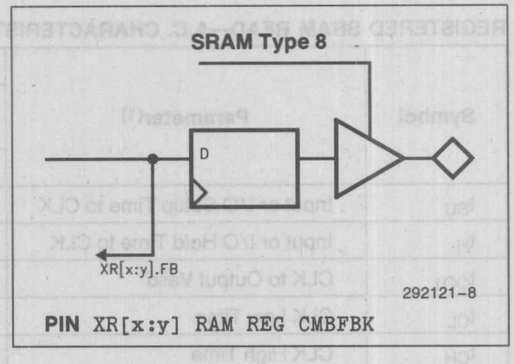
(disabled)



292121-5

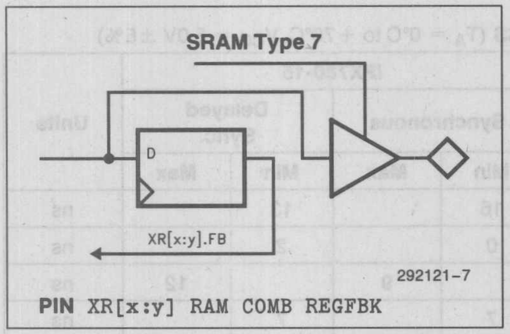
```
NODE XR[x:y] RAM COMB
```





SRAM Types 5 and 6 are buried nodes. They do not use the I/O pin to which they may be attached. That pin is still available as an input, using the dual-feedback paths of the iFX780 and iFX740.

SRAM Types 7 and 8 use some very unique features of the iFX780 and iFX740 architecture. Normal macrocells may also be configured in the same fashion.



SRAM RESTRICTIONS

1) Types 2–8 cannot be simulated in PLDshell Plus 3.X.

2) Only the CLK1 Sync. clock is available for SRAM registers. To invert, specify the CLK1 signal as active low in the pin list. Do not forget to re-invert the clock for those signals that need the normal rising-edge clock.

3) No clears or presets are available for SRAM registers.

4) Device timings for types 2–8 have not been characterized. The following timings are preliminary.

3.0 SRAM REGISTER MODE CHARACTERISTICS

REGISTERED SRAM READ—A.C. CHARACTERISTICS (T_A = 0°C to +70°C, V_{CC} = 5.0V ±5%)

Symbol	Parameter(1)	iFX780-10 Synchronous		iFX780-10 Delayed Sync.		Units
		Min	Max	Min	Max	
t_{SU}	Input or I/O Setup Time to CLK	11.5		10		ns
t_H	Input or I/O Hold Time to CLK	0		2		ns
t_{CO1}	CLK to Output Valid		6		8	ns
t_{CL}	CLK Low Time	4		4		ns
t_{CH}	CLK High Time	4		4		ns
t_{CP}	CLK Period	15		15		ns

NOTE:
1. Device Characterization of Registered SRAM T_{SU}/T_{CO} has not been completed.

REGISTERED SRAM READ—A.C. CHARACTERISTICS ($T_A = 0°C$ to $+70°C$, $V_{CC} = 5.0V \pm 5\%$)

Symbol	Parameter(1)	iFX740-10				Units
		Synchronous		Delayed Sync.		
		Min	Max	Min	Max	
t_{SU}	Input or I/O Setup Time to CLK	6.5		5		ns
t_H	Input or I/O Hold Time to CLK	0		2		ns
t_{CO1}	CLK to Output Valid		6		8	ns
t_{CL}	CLK Low Time	4.5		4.5		ns
t_{CH}	CLK High Time	4.5		4.5		ns
t_{CP}	CLK Period	10		10.5		ns

NOTE:
1. Device Characterization of Registered SRAM T_{SU}/T_{CO} has not been completed.

REGISTERED SRAM READ—A.C. CHARACTERISTICS ($T_A = 0°C$ to $+70°C$, $V_{CC} = 5.0V \pm 5\%$)

Symbol	Parameter(1)	iFX780-15				Units
		Synchronous		Delayed Sync.		
		Min	Max	Min	Max	
t_{SU}	Input or I/O Setup Time to CLK	16		13		ns
t_H	Input or I/O Hold Time to CLK	0		2		ns
t_{CO1}	CLK to Output Valid		9		12	ns
t_{CL}	CLK Low Time	7		7		ns
t_{CH}	CLK High Time	7		7		ns
t_{CP}	CLK Period	20		20		ns

NOTE:
1. Device Characterization of Registered SRAM T_{SU}/T_{CO} has not been completed.

REGISTERED SRAM READ—A.C. CHARACTERISTICS ($T_A = 0°C$ to $+70°C$, $V_{CC} = 5.0V \pm 5\%$)

Symbol	Parameter(1)	iFX740-15				Units
		Synchronous		Delayed Sync.		
		Min	Max	Min	Max	
t_{SU}	Input or I/O Setup Time to CLK	11		8		ns
t_H	Input or I/O Hold Time to CLK	0		2		ns
t_{CO1}	CLK to Output Valid		9		12	ns
t_{CL}	CLK Low Time	7		7		ns
t_{CH}	CLK High Time	7		7		ns
t_{CP}	CLK Period	15		15		ns

NOTE:
1. Device Characterization of Registered SRAM T_{SU}/T_{CO} has not been completed.

APPLICATION NOTE

JTAG 1149.1 Specifications for In-Circuit Reconfiguration and Programming FLEXlogic FPGAs

RICHARD VIREDAY
SOFTWARE DEVELOPMENT TOOLS

October 1993

3

PRELIMINARY
Order Number: 292122-001

JTAG 1149.1 Specifications for In-Circuit Reconfiguration and Programming the iFX780 FPGA

CONTENTS

PAGE

1.0 INTRODUCTION

This Application Note provides a detailed description of the Intel iFX780 FPGA JTAG Specifications and Electrical Characteristics. If you are not using the FLEXlogic Prototyping Cable Kit, then this document will show you how to load configurations into the iFX780.

This document has the following sections.

- Bitmap File Generation
- In-Circuit Reconfiguration and Programming Information
- Detailed JTAG 1149.1 Information

2.0 BITMAP FILE GENERATION

First, a Bitmap file must be generated from a JEDEC file for the iFX780. The JEDEC file can come from any design software.

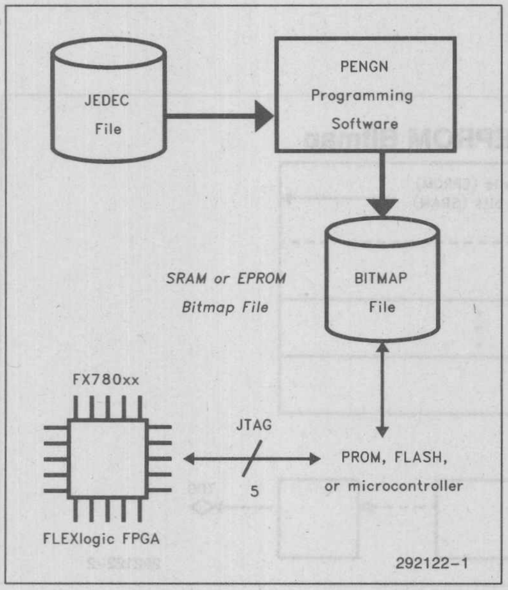


Figure 1. Configuration Process

The "pengn" Bitmap file can come in one of two flavors, either as an SRAM or an EPROM file.

The difference between the two Bitmaps is that an SRAM Bitmap is used to reconfigure the device after it has been powered up.

The EPROM Bitmap is used to program the non-volatile EPROM bits on the device. These are OTP (one-time programmable), and provide a default configuration on power-up.

Commands to generate Bitmaps: *(assuming that buscon is the JEDEC file)*

SRAM Bitmap

```
pengn -part fx780_84 -bs buscon.bit buscon
```

EPROM Bitmap

```
pengn -part fx780_84 -be buscon.bit buscon
```

NOTE:

Use fx780__132 for the 132-pin device.

The "pengn" program is included with the PLDshell R3.0 software. This will translate the JEDEC file to the Bitmap. "pengn" is documented in the PLDshell User Manual, Appendix E.

Translating the Bitmaps to actual test vectors is covered in "Download Algorithms" (Section 6.0).

3.0 SRAM RECONFIGURATION

To do in-circuit reconfiguration of the FPGA, the SRAM Bitmap (generated from the JEDEC file) can be shifted into the device static RAM configuration registers, as shown below. The first bit in each record is shifted in first.

The order of the bits shifted out will match exactly the order of those shifted in, i.e. first-in, first-out.

Hi-Z Outputs

As long as the device is in SWRITE mode, user outputs are in a Hi-Z state. In order to enable the outputs, the instruction register must be modified with a new instruction (i.e. IDCODE, BYPASS, etc.) The easiest method is to go to TEST-LOGIC RESET which will reset the Instruction Registers to IDCODE.

4.0 EPROM PROGRAMMING

The EPROM Bitmap described earlier can be shifted into the device static RAM configuration registers, as shown below. The first bit in each record is shifted in first.

EPROM Programming requires careful control of the power pins. In particular, the V_{PP} programming voltage for the EPROM cells should be raised to its high voltage state after the device has powered up. See "Quick-Pulse Programming Algorithm" (Section 9.1) for further details.

Inputs

Inputs on the device do not have to be static during in-circuit reconfiguration and programming operations (SWRITE and FPGM modes).

Time

SRAM Reconfiguration Time:

JTAG Clock * ~32 Kbit vectors

Example:

8 MHz * ~32K = 4 μs

EPROM Programming Time:

JTAG Clock * ~32 Kbit vectors + 200 μs per pulse * 1080 pulses

Example:

= 8 MHz * ~32K + 200 μs * 1080

= 4 μs + 216 ms

All times are approximate.

5.0 SECURITY BITS

The security bits are programmed normally along with the rest of the device EPROM bits. *Only when the iFX780 is next powered down, then powered back up will the security feature be enabled.* Until that time, the device may be accessed as normal.

Note that even though the security bits prevents the device EPROM from being read, it may still be reconfigured once the device has been powered up. The EPROM fuses will not be affected, but a new configuration can be loaded into the device. This new SRAM configuration cannot be read out, and will be lost when power is removed.

Thus once the security bit is set, the device configuration is writable, but never readable.

This is only true for SRAM reconfiguration. Once the security bits are set, the EPROM bits cannot be overprogrammed with a new pattern.

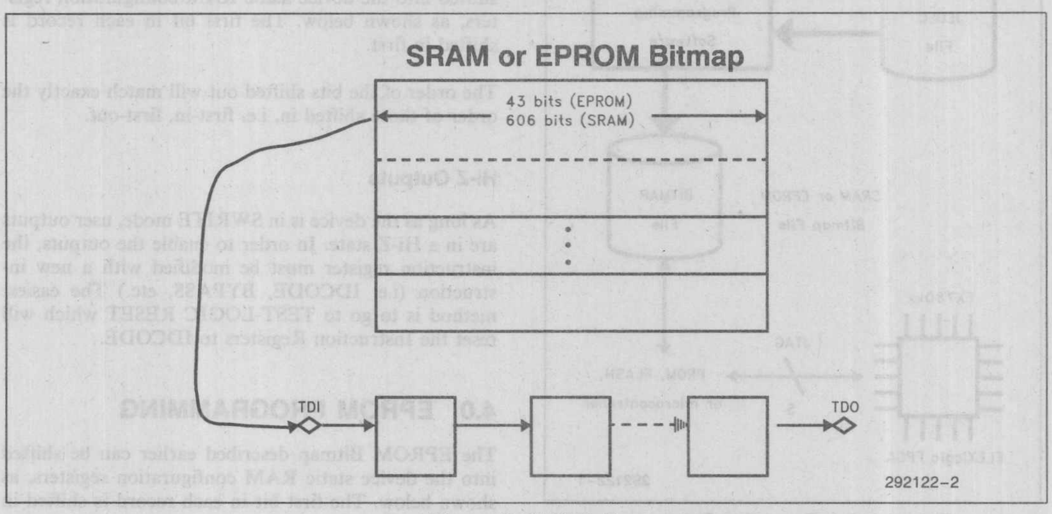


Figure 2. Shift Path

6.0 DOWNLOAD ALGORITHMS

The basic algorithm necessary to configure or program the device is shown in pseudo-code below.

```
Device Power on
Send Header State Vectors
WHILE (not end of vectors)
BEGIN
  Send SRAM/EPROM Bitmap file
    vector information
  Send Middle State Vectors
END
Send Footer State Vectors
```

The Header, Middle and Footer information are predefined operations that control the device JTAG state controller operations. These whill shift in instructions to get the JTAG TAP Controller to the proper state. See the next page for the TAP state machine.

There is an example "C" program, "fx ims.c", distributed with the PLDshell R3.0 software. This program will read either the SRAM or EPROM bitmaps, and translate the output into IMS(1) style test vectors with the necessary Header/Middle/Footer information. This includes deciding whether to use the FPGM or SWRITE instruction.

NOTE:

1. IMS is a trademark of Integrated Measurement Systems.

The rest of this document contains further details on using the iFX780 SRAM and EPROM reconfiguration via the JTAG port. Some knowledge of JTAG is required in order to understand the Instructions and Opcodes.

7.0 BSDL FILES

To facilitate the development of boundary scan test programs, use the BSDL (Boundary Scan Description Language) files for the iFX780. The files are,

I780_132.BSD-for the 132-pin package.
I780_84.BSD-for the 84-pin package

These files can be found in the PLDshell installation directory. You can also use the Intel PLD Bulletin Board by dialing: (916) 356-5702 or Applications Support Hotline 1-800-628-8686.

8.0 JTAG 1149.1 FOR THE iFX780

Further information on JTAG can be found in the "IEEE Standard Access Port and Boundary-Scan Architecture", IEEE Standard 1149.1-1990. For the rest of this document, it is useful, but not necessary, to have some knowledge of JTAG and using the TAP (Test Access Port).

The state machine for the TAP is controlled by the TMS pin. Entering the *SHIFT-R* state, a device instruction is then loaded into the device and executed. See "JTAG Public Instructions and OPCODES" (Table 2) for the iFX780 JTAG instructions.

Table 1. Pin Connections for iFX780 JTAG Operations

Pin Name	iFX780_132 PQFP Pin Numbers	iFX780_84 PLCC Pin Numbers
V_{CC} (5V)	21, 87	26, 68
V_{SS}	11, 17, 18, 27, 44, 53, 59, 77, 83, 84, 93, 110, 125	17, 23, 29, 38, 46, 59, 65, 71, 80
V_{PP}	119	4
T_{DI}	132	11
T_{DO}	131	10
T_{CK}	66	53
T_{MS}	65	52
I/Oxxx, INxx, V_{CCOx}, CLKx	All other pins may be connected as required by the application. Refer to the device datasheet for further pinout information.	

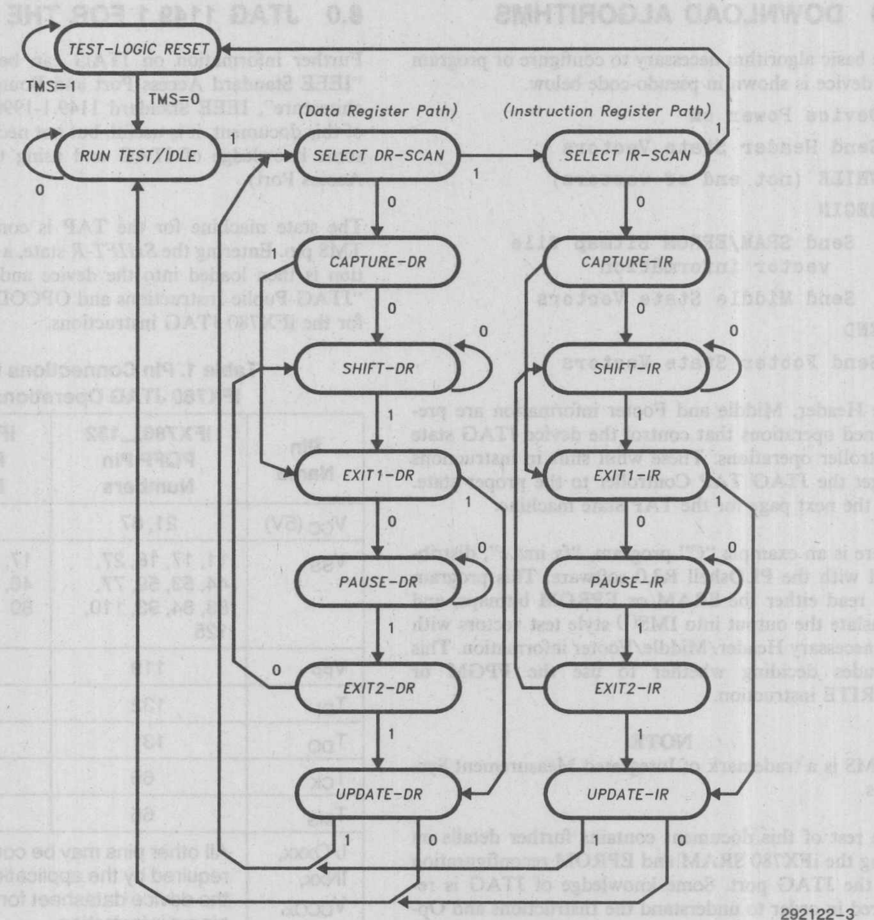
EXTRA PIN NOTES:

V_{PP}—Do not set to GND. Set to either V_{CC}, V_{PP} or leave floating. Ensure that V_{PP} becomes active after V_{CC} has been established.

V_{CCO0}—Must be +5V during programming. Other V_{CCO} pins may be either 3V or 5V, as required by your application.

For SRAM reconfiguration, no special voltages are required.

3



NOTES:
All state transitions occur on the rising edge of TCK, and are dependent on the state of TMS.
To reset the TAP Controller to the *TEST-LOGIC-RESET* state, set TMS = 1 and clock TCK for at least 5 cycles.

Figure 3. IEEE 1149.1 TAP Controller State Machine

Opcode	Instruction	Brief Description
00000	EXTEST	Drive Outputs with Pre-Loaded Data
00001	SAMPLE/ PRELOAD	Read Current Pin State/Pre-Load Next Pin State
00010	IDCODE	Read Manufacturer's ID Code
00101	LDVECT	Load Vector into Program Shift Register
00110	FREAD	EPROM Read
01111	SWRITE	SRAM Write
10000	SREAD	SRAM Read
10100	PORST	Power-on Reset. Restarts Device Architecture.
10101	FPGM	EPROM Program
11101	HI-Z	3-state All The Outputs
10110	UESCODE	Shift Out UES Bits
11000	RADLOAD	Row Address Load
11111	BYPASS	Bypass
MSB..LSB(1)		

NOTE:
1. This is also the shift order of the Opcode bits into the device. LSB first, then MSB.

The TDI/TDO pins are only active in the *SHIFT-DR* and *SHIFT-IR* states.

By convention, DR stands for Data Register, IR stands for Instruction Register.

Opcodes not specified are reserved by Intel as private instructions, and must not be used otherwise damage to the device may result.

The details for each instruction are described in the next sections.

8.1 LDVECT—Opcode 00101

This instruction is used to load row/column address and Programming data. The Data shift register chain in this mode contains forty-three (43) bits of data. The gramming (Section 4.0). The instruction register is updated in *UPDATE-IR* state of the TAP controller state machine. Data is shifted out or in from the SHIFTDR state.

To load the data for the programming, load the instruction register with LDVECT instruction. This occurs via entering the *SHIFT-IR* state, and shifting the OPCODE in, while TMS = 0. The OPCODE LSB is loaded on the rising edge of TCK during the second SHIFT-IR state; the MSB is loaded on the rising edge of TCK during EXIT-IR (see timing diagrams in Figure 4). Then enter the *SHIFT-DR* state and shift in the data packet.

8.2 IDCODE—Opcode 00010

This instruction is used to read out the ID code register for the device, which is fixed by Intel and is described in Table 4. iFX780 Manufacturer Codes and User ID Bytes. During this mode, a dedicated 32-bit device identification register (DIR) chain is connected between TDI and TDO. During *CAPTURE-DR* state the IDCODE is loaded into the Instruction Register, and can be shifted out in the *SHIFT-DR* state

8.3 FPGM—Opcode 10101

This instruction is used to program EPROM cells. Row/column addresses and Program Data were shifted in using LDVECT instruction. The instruction will not be enabled unless V_{PP} pin is at high voltage. V_{PP} pin must be at high voltage at least 2 μs before the FPGM instruction is updated. If the security bit is set the mode will not be enabled.

Programming is initiated in the *Run-Test/Idle* state at the first falling edge of the TCK. The device must stay in this state at least 200 μs. If the amount of time spent in *Run-Test/Idle* state is longer than 200 μs, internal timer will terminate the programming pulse internally. If the time is shorter, TAP controller will terminate the programming pulse at the falling edge of TCK after exiting *Run-Test/Idle* state.

Program data and the verify data are internally verified by XORing both. XOR data is latched into Program/Verify status register in the *CAPTURE-DR* state. This one bit of data can be shifted out in *SHIFT-DR* state through the TDO pin. Address or Program data information is not altered during this operation. Therefore, if a fail data is detected, the programmer could go back to *Run Test/Idle* state and provide another programming pulse as shown.

3

Only the Program/Verify status bit register is in the TDI/TDO chain. TDI pin is not connected to the serial in path of this register. When the status bit is shifted out a FAIL data (0) is shifted into the status bit register.

While shifting in the next data to be programmed, the verified data can be shifted out using the LDVECT command at the same time.

WARNING:
The device will not enter/execute FPGM unless the V_{PP} pin is at V_{PP} high voltage. The device will verify back that programming has occurred. In order to absolutely verify that the EPROMs have actually been programmed, an FREAD operation must be performed.

In order to make the programming operation JTAG compliant with the BSDL files, a RADLOAD instruction may be inserted *before* the FREAD instruction. RADLOAD only loads the 6 bits of the row address register. This register will be overwritten by the FREAD instruction later. The RADLOAD functions as a NOP (No OPeration) instruction in order to satisfy the EPROM element timings.

8.4 FREAD—Opcode 00110

This instruction is used to read out an entire row of EPROM data. Only the row address needs to be shifted in. After shifting in the row addresses, the device must stay in the *Run Test/Idle* state for at least 250 ns before capturing the read data in the *CAPTURE-DR* state. There is NO internal verify built in for this mode.

A typical operation would be to load in FREAD instruction and then enter the *SHIFT-DR* state, shift in the Row address and then enter the *Run Test/Idle* state and remain there for at least 250 ns. Then enter the *CAPTURE-DR* state where the data is captured into the shift registers. Captured data can be shifted out through TDO pin in *SHIFT-DR* state.

8.5 SWRITE—Opcode 01111

This instruction is used to alter the contents of the SRAM bits of the device, not the EPROM bits. This can be used to reconfigure the device. Data to be written to the SRAM cells and the row address are shifted in the *SHIFT-DR* state. The SRAM write operation is actually performed in *Run Test/Idle* state of the TAP controller.

SRAM write is initiated on the first falling edge of TCK in *Run Test/Idle* state and is terminated on the first falling edge of TCK after exiting *Run Test/Idle* state. It should be ensured that the user remains in *Run Test/Idle* state for at least for 100 ns.

There is no verify or read in this mode. To read out the contents of the SRAM cells, the SREAD command may be used.

A typical operation would be to load in SWRITE instruction, move to *SHIFT-DR* state, shift in the data and then move to the *Run Test/Idle* state to execute the write.

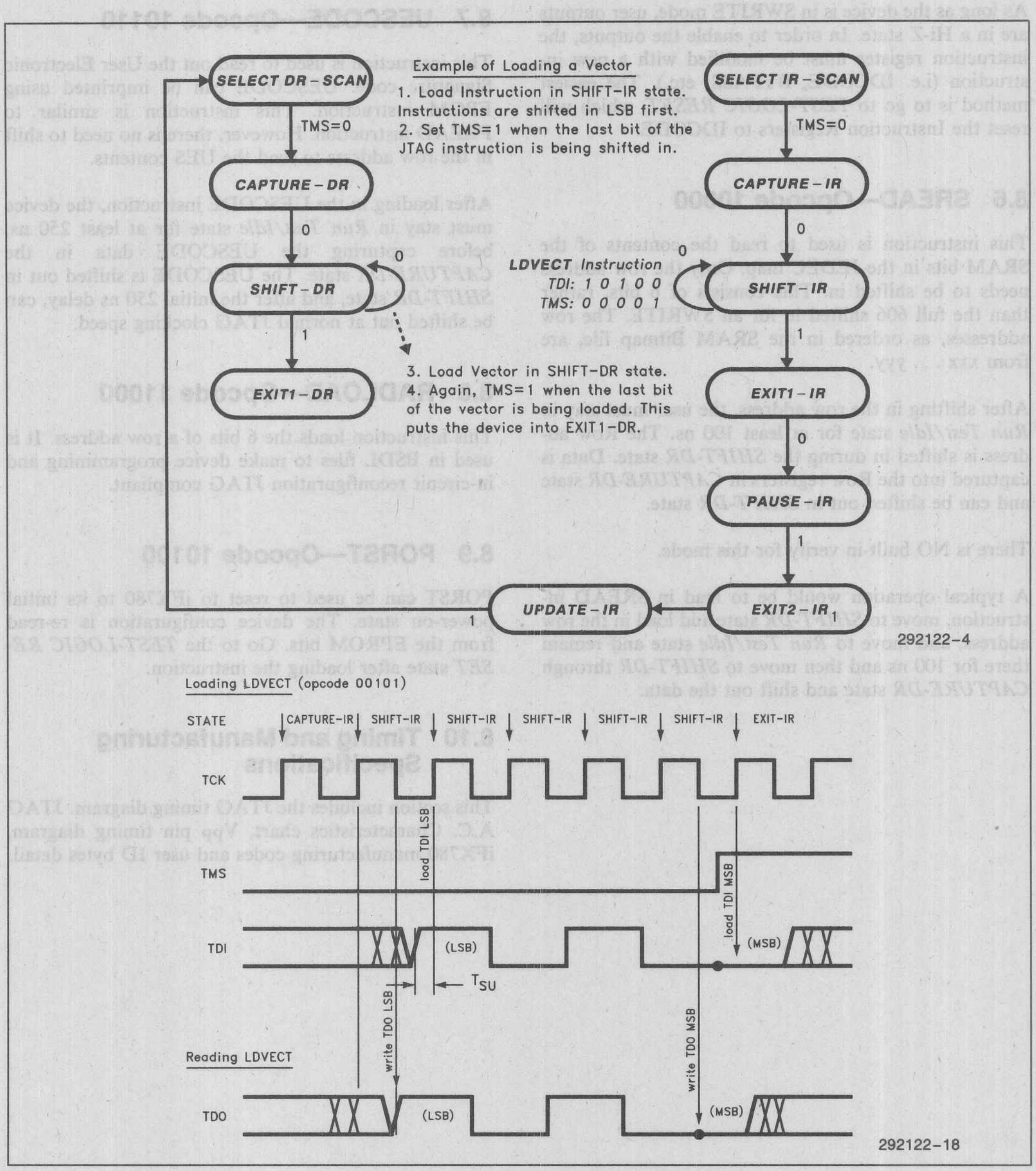


Figure 4. Timing Diagram

As long as the device is in SWRITE mode, user outputs are in a Hi-Z state. In order to enable the outputs, the instruction register must be modified with a new instruction (i.e. IDCODE, BYPASS, etc.). The easiest method is to go to *TEST-LOGIC RESET*, which will reset the Instruction Registers to IDCODE.

8.6 SREAD—Opcode 10000

This instruction is used to read the contents of the SRAM bits in the JEDEC map. Only the row address needs to be shifted in. This consists of 6 bits, rather than the full 606 shifted in for an SWRITE. The row addresses, as ordered in the SRAM Bitmap file, are from xxx . . . yyy.

After shifting in the row address, the user must stay in *Run Test/Idle* state for at least 100 ns. The Row address is shifted in during the *SHIFT-DR* state. Data is captured into the Row registers in *CAPTURE-DR* state and can be shifted out in *SHIFT-DR* state.

There is NO built-in verify for this mode.

A typical operation would be to load in SREAD instruction, move to *SHIFT-DR* state and load in the row address, and move to *Run Test/Idle* state and remain there for 100 ns and then move to *SHIFT-DR* through *CAPTURE-DR* state and shift out the data.

8.7 UESCODE—Opcode 10110

This instruction is used to read out the User Electronic Signature code. UESCODE can be imprinted using FPGM instruction. This instruction is similar to FREAD instruction. However, there is no need to shift in the row address to read the UES contents.

After loading in the UESCODE instruction, the device must stay in *Run Test/Idle* state for at least 250 ns, before capturing the UESCODE data in the *CAPTURE-DR* state. The UESCODE is shifted out in *SHIFT-DR* state, and after the initial 250 ns delay, can be shifted out at normal JTAG clocking speed.

8.8 RADLOAD—Opcode 11000

This instruction loads the 6 bits of a row address. It is used in BSDL files to make device programming and in-circuit reconfiguration JTAG compliant.

8.9 PORST—Opcode 10100

PORST can be used to reset to iFX780 to its initial power-on state. The device configuration is re-read from the EPROM bits. Go to the *TEST-LOGIC RESET* state after loading the instruction.

8.10 Timing and Manufacturing Specifications

This section includes the JTAG timing diagram. JTAG A.C. Characteristics chart, V_{PP} pin timing diagram, iFX780 manufacturing codes and user ID bytes detail.

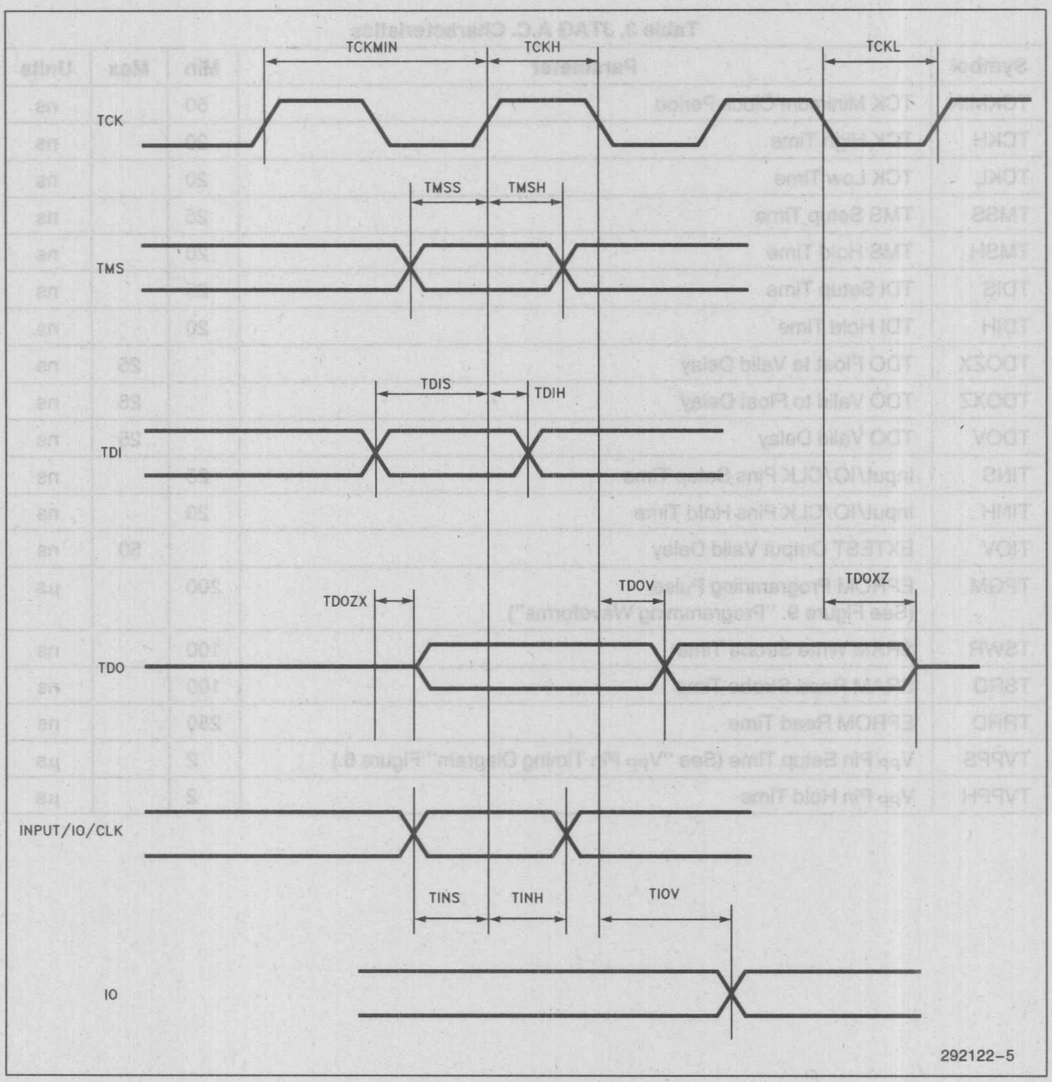


Figure 5. JTAG Timings

Table 3. JTAG A.C. Characteristics

Symbol	Parameter	Min	Max	Units
TCKMIN	TCK Minimum Clock Period	50		ns
TCKH	TCK High Time	20		ns
TCKL	TCK Low Time	20		ns
TMSS	TMS Setup Time	25		ns
TMSH	TMS Hold Time	20		ns
TDIS	TDI Setup Time	25		ns
TDIH	TDI Hold Time	20		ns
TDOZX	TDO Float to Valid Delay		25	ns
TDOXZ	TDO Valid to Float Delay		25	ns
TDOV	TDO Valid Delay		25	ns
TINS	Input/IO/CLK Pins Setup Time	25		ns
TINH	Input/IO/CLK Pins Hold Time	20		ns
TIOV	EXTEST Output Valid Delay		50	ns
TPGM	EPROM Programming Pulse (See Figure 9. "Programming Waveforms")	200		μs
TSWR	SRAM Write Strobe Time	100		ns
TSRD	SRAM Read Strobe Time	100		ns
TRRD	EPROM Read Time	250		ns
TVPPS	V_{PP} Pin Setup Time (See "V_{PP} Pin Timing Diagram" Figure 6.)	2		μs
TVPPH	V_{PP} Pin Hold Time	2		μs

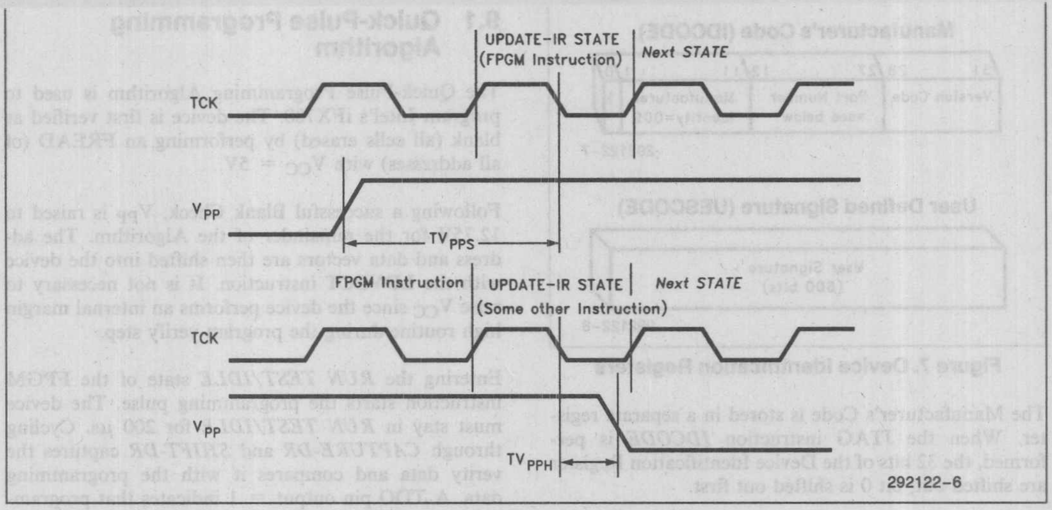


Figure 6. V_{PP} Pin Timing Diagram

Table 4. iFX780 Manufacturer Codes and User ID Bytes

Device	Hex Value	Ver.	Part Number	Manufacturer's Identity	0
132-Pin	00621013h	0 0 0 0	0 0 0 0 0 1 1 0 0 0 1 0 0 0 0 1	0 0 0 0 0 0 0 1 0 0 1	1
84-Pin	10621013h	0 0 0 1	0 0 0 0 0 1 1 0 0 0 1 0 0 0 0 1	0 0 0 0 0 0 0 1 0 0 1	1

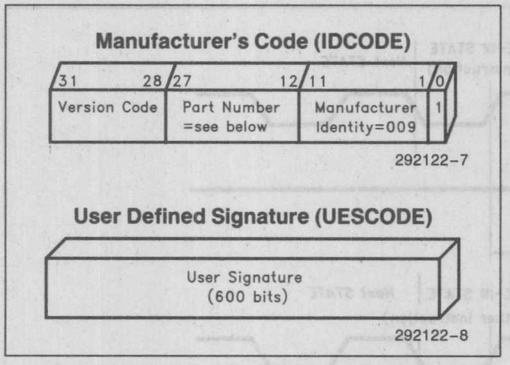


Figure 7. Device Identification Registers

The Manufacturer's Code is stored in a separate register. When the JTAG instruction *IDCODE* is performed, the 32 bits of the Device Identification Register are shifted out; bit 0 is shifted out first.

A user code can be stored in the User Electronic Signature (UES) field of the JEDEC file. When the UESCODE instruction of the JTAG port is accessed, the 600 bits are shifted out.

NOTE:

There is an *optional* JTAG instruction called *USERCODE.* This is **not** the same as *UESCODE,* and the two should not be confused. The iFX780 FPGA does not implement the JTAG *USERCODE* instruction.

9.0 EPROM PROGRAMMING

The next sections contain the electrical programming information for the Intel iFX780. Included are the electrical addresses to be programmed, and the programming process algorithm, the programming waveforms, and the physical address to programming packet mapping.

9.1 Quick-Pulse Programming Algorithm

The Quick-Pulse Programming Algorithm is used to program Intel's iFX780. The device is first verified as blank (all cells erased) by performing an FREAD (of all addresses) with $V_{CC} = 5V$.

Following a successful Blank Check, V_{PP} is raised to 12.75V for the remainder of the Algorithm. The address and data vectors are then shifted into the device with the LDVECT instruction. It is not necessary to raise V_{CC} since the device performs an internal margin high routine during the program verify step.

Entering the *RUN TEST/IDLE* state of the FPGM instruction starts the programming pulse. The device must stay in *RUN TEST/IDLE* for 200 μs. Cycling through *CAPTURE-DR* and *SHIFT-DR* captures the verity data and compares it with the programming data. A TDO pin output = 1 indicates that programming passed while a TDO pin output = 0 indicates that programming failed. A fail on verify requires up to 24 additional pulses before the algorithm terminates.

This program/verify sequence is repeated until the last address is programmed. When programming is complete, a final verify of the EPROM may be accomplished with the FREAD instruction.

WARNING:

The device will not enter/execute FPGM unless the V_{PP} pin is at V_{PP} high voltage. The device will verify back that programming has occurred. In order to absolutely verify that the EPROMs have actually been programmed, an FREAD operation must be performed.

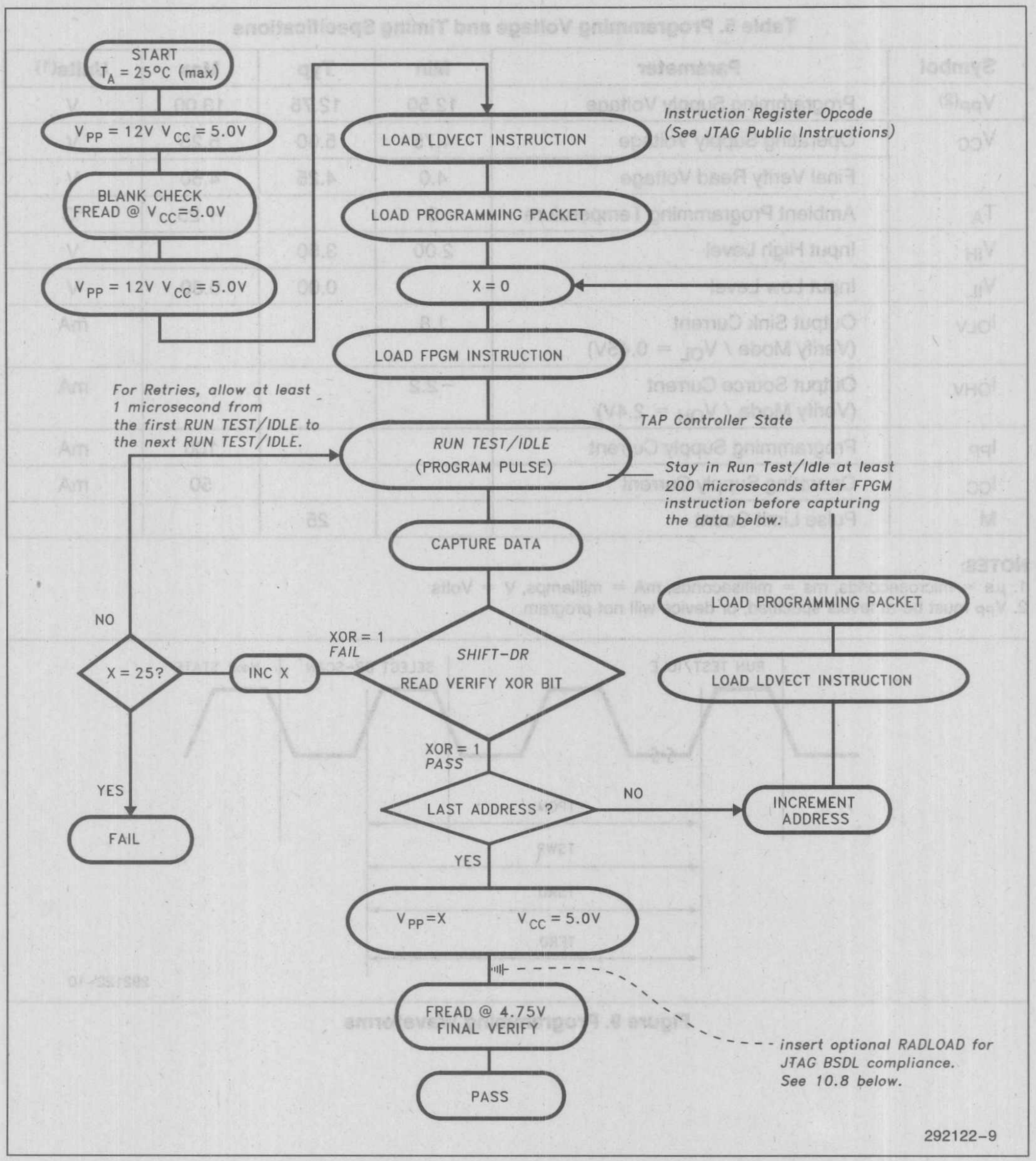


Figure 8. Quick-Pulse Algorithm Flow Chart

Table 5. Programming Voltage and Timing Specifications

Symbol	Parameter	Min	Typ	Max	Units[1]
V_{PP}[2]	Programming Supply Voltage	12.50	12.75	13.00	V
V_{CC}	Operating Supply Voltage	4.75	5.00	5.25	V
	Final Verify Read Voltage	4.0	4.25	4.50	V
T_A	Ambient Programming Temperature	0		+25	°C
V_{IH}	Input High Level	2.00	3.50		V
V_{IL}	Input Low Level		0.00	0.80	V
I_{OLV}	Output Sink Current (Verify Mode / V_{OL} = 0.45V)	1.8			mA
I_{OHV}	Output Source Current (Verify Mode / V_{OH} = 2.4V)	−2.2			mA
I_{PP}	Programming Supply Current			100	mA
I_{CC}	Operating Supply Current			50	mA
M	Pulse Limit Count		25		

NOTES:
1. μs = microseconds, ms = milliseconds, mA = milliamps, V = Volts
2. V_{PP} must be at levels specified, or device will not program.

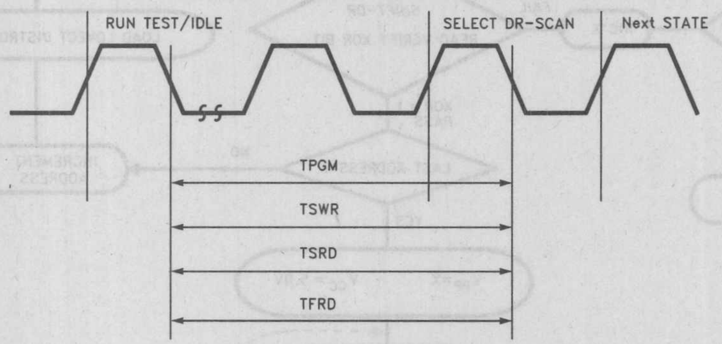


Figure 9. Programming Waveforms

PRELIMINARY

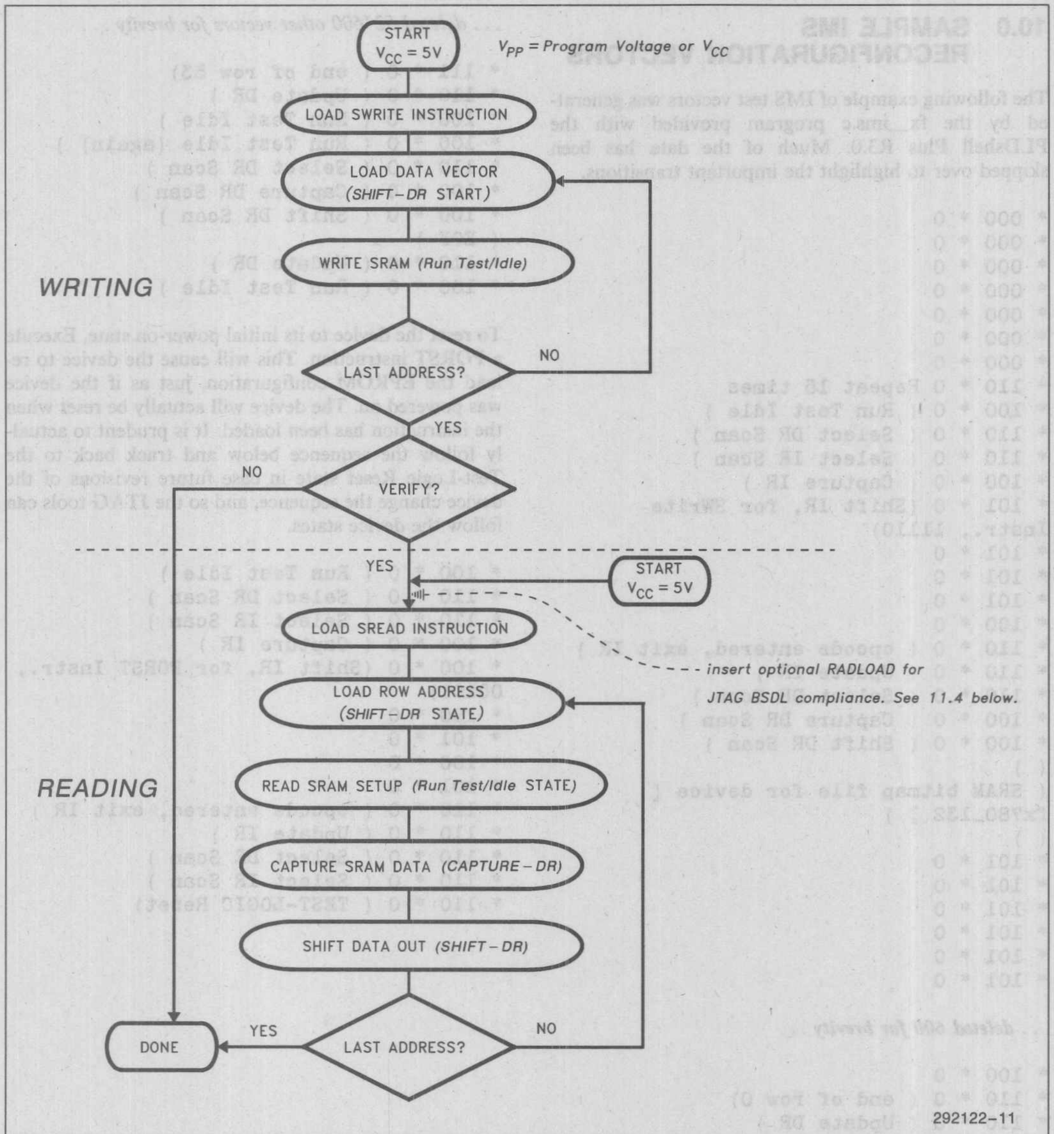


Figure 10. Reconfiguration Flowchart

3

10.0 SAMPLE IMS RECONFIGURATION VECTORS

The following example of IMS test vectors was generated by the fx_ims.c program provided with the PLDshell Plus R3.0. Much of the data has been skipped over to highlight the important transitions.

```
* 000 * 0
* 000 * 0
* 000 * 0
* 000 * 0
* 000 * 0
* 000 * 0
* 000 * 0
* 110 * 0 Repeat 15 times
* 100 * 0 ( Run Test Idle )
* 110 * 0 ( Select DR Scan )
* 110 * 0 ( Select IR Scan )
* 100 * 0 ( Capture IR )
* 101 * 0 (Shift IR, for SWrite
Instr., 11110)
* 101 * 0
* 101 * 0
* 101 * 0
* 100 * 0
* 110 * 0 ( opcode entered, exit IR )
* 110 * 0 ( Update IR )
* 110 * 0 ( Select DR Scan )
* 100 * 0 ( Capture DR Scan )
* 100 * 0 ( Shift DR Scan )
( )
( SRAM bitmap file for device [
fx780_132 ] )
( )
* 101 * 0
* 101 * 0
* 101 * 0
* 101 * 0
* 101 * 0
* 101 * 0
```

. . . deleted 600 for brevity . . .

```
* 100 * 0
* 110 * 0 ( end of row 0)
* 110 * 0 ( Update DR )
* 100 * 0 ( Run Test Idle )
* 100 * 0 ( Run Test Idle (again) )
* 110 * 0 ( Select DR Scan )
* 100 * 0 ( Capture DR Scan )
* 100 * 0 ( Shift DR Scan )
* 100 * 0
* 101 * 0
* 101 * 0
* 101 * 0
```

*. . . deleted 52*600 other vectors for brevity . . .*

```
* 111 * 0 ( end of row 53)
* 110 * 0 ( Update DR )
* 100 * 0 ( Run Test Idle )
* 100 * 0 ( Run Test Idle (again) )
* 110 * 0 ( Select DR Scan )
* 100 * 0 ( Capture DR Scan )
* 100 * 0 ( Shift DR Scan )
( EOF )
* 110 * 0 ( Update DR )
* 100 * 0 ( Run Test Idle )
```

To reset the device to its initial power-on state, Execute a PORST instruction. This will cause the device to reload the EPROM configuration, just as if the device was powered on. The device will actually be reset when the instruction has been loaded. It is prudent to actually follow the sequence below and track back to the Test-Logic Reset state in case future revisions of the device change the sequence, and so the JTAG tools can follow the device states.

```
* 100 * 0 ( Run Test Idle )
* 110 * 0 ( Select DR Scan )
* 110 * 0 ( Select IR Scan )
* 100 * 0 ( Capture IR )
* 100 * 0 (Shift IR, for PORST Instr.,
00101)
* 100 * 0
* 101 * 0
* 100 * 0
* 101 * 0
* 110 * 0 ( opcode entered, exit IR )
* 110 * 0 ( Update IR )
* 110 * 0 ( Select DR Scan )
* 110 * 0 ( Select IR Scan )
* 110 * 0 ( TEST-LOGIC Reset)
```

```
/****************************************************************************/
/* Program name: fx_ims.c                                                   */
/* Version Number: 0                                                        */
/* Author: Richard Vireday                                                  */
/* Date: March 1993                                                         */
/* $Revision: 0.0 $                                                         */
/****************************************************************************/

/****************************************************************************/
/* Description: This program will translate the 'pengn' Bitmap */
/* file format into EPROM and SRAM test vectors for the IMS. */
/****************************************************************************/

/**************************** INTEL CORPORATION ************************
 * Copyright (C) 1993 by Intel Corporation.
 * Intel Corporation, 3065 Bowers Avenue, Santa Clara, California 95051.
 *
 * This program is made available for public release as part of the
 * iFX780 FPGA device support.
 *
 * Intel Corporation assumes no responsibility for the reliability,
 * support, use, or modifications to this program.!
 *
 ***********************************************************************
 */

/* standard includes */
#include <stdio.h>

#define MAXLINE 1000 /* maximum input line length */
#define MAXNAME 100 /* maximum filename length */

#define EOS '\0'
#define EOL '\n'

/* equates for packet information and file types */
#define SRAM_TYPE 0
#define EPROM_TYPE 1

#define SRAM_LEN 606
#define EPROM_LEN 43

/* function to write a JTAG vector, such as an instruction */
wr_vector(format, comment, vector, outfile)
char *format;
char *comment;
char *vector;
FILE *outfile;
{
 char *v = vector;

 fprintf(outfile, format, *v++);
 fprintf(outfile, " {%s, %s}\n",comment, vector);
 while (*v != EOS)
```

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```
{
        fprintf(outfile, format, *v++);
        fputc(EOL, outfile);
}
}

main(argc, argv)
int argc; /* number of command line args */
char **argv; /* command line ptr string */
{
        FILE *infile; /* input file */
        FILE *outfile; /* output file */
        FILE *fopen();

        char *inname; /* input filename */
        char *outname; /* output filename */

        char c; /* process variables */

        int type_of_file; /* to indicate type */

        int i; /* index variable */
        int no_rows; /* the number of rows processed */

        int data_len; /* the length of data in a packet */

        /* Standard IMS Vector Format. '*' starts a new vector */
        char *vecfmt = " * 10%c * 0";
        /* ::: :...TCK signal (in next vector)
         * :::...TDI
         * ::...TMS
         * :...TCK signal
         */

/****************************************************************************/
/* Parse command line arguments */
/****************************************************************************/

 inname = NULL; /* initialize filename strings */
 outname = NULL;

 i=1;
 while (i < argc)
 {
        if (inname == NULL)
         inname = argv[i]; /* get file names */
        else if (outname == NULL)
         outname = argv[i];

        /* else all other arguments ignored */
        i++;
 }

/****************************************************************************/
```

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```
/* Check command line arguments */
/***************************************************************************/

if (inname == NULL)
{
        printf("%s: Error, source bit filename not specified.\n",argv[0]);
        exit(1);
}
if (outname == NULL)
{
        printf("%s: Error, output pattern filename not specified.\n",argv[0]);
        exit(1);
}

/***************************************************************************/
/* Open files for processing */
/***************************************************************************/

if ((infile = fopen(inname,"r")) == NULL)
{
        printf("%s: Error opening source bit pattern filename %s\n",
                                                        argv[0],inname);
        exit(1);
}
if ((outfile = fopen(outname,"w")) == NULL)
{
        printf("%s: Error opening output pattern filename %s\n",
                                                        argv[0],outname);
        exit(1);
}

/***************************************************************************/
/* Preliminary processing of source bit pattern file */
/***************************************************************************/
/* First we determine the length of the vectors, and what type of file */
/* is being used. Then we know what instruction to use. SWRITE or FPGM */

data_len = 0;
while ((c = getc(infile)) != EOF)
{
        if (c == ':') /* enter comment state */
        {
         while ((c = getc(infile)) != EOL)
         {
                if (c == EOF)
                 break;
         }
        }

        if (c != EOL)
        {
         while ((c = getc(infile)) != '*')
         {
                if (c == EOF) break;
```

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```
                if (c == ';') break;

                if (c != EOL)
                 data_len++;
          }
          break;
          }
}

rewind(infile); /* reset to re-read again */

switch (data_len)
{
        case SRAM_LEN:
         printf("SRAM vectors in %s, vector length %d\n", inname, data_len);
         type_of_file = SRAM_TYPE;
         break;
        case EPROM_LEN:
         printf("EPROM vectors in %s, vector length %d\n", inname, data_len);
         type_of_file = EPROM_TYPE;
         break;
        default:
         printf("WARNING: Unknown vectors in %s, vector length %d\n",
                                                 inname, data_len);
         printf("Assuming SRAM type.\n");
         type_of_file = SRAM_TYPE;
         break;
}

/**************************************************************************/
/* Add Initial Information to output pattern */
/**************************************************************************/
/* Comments are in { }, and show the JTAG TAP Controller state the*/
/* vector will put the device into.                   */

for (i = 0 ; i < 8; i++)
        fprintf(outfile, "* 000 * 0\n");
fprintf(outfile, "* 110 * 0 Repeat 15 times\n"); /* to initialize */
fprintf(outfile, "* 100 * 0 { Run Test Idle }\n");
fprintf(outfile, "* 110 * 0 { Select DR Scan }\n");
fprintf(outfile, "* 110 * 0 { Select IR Scan }\n");
fprintf(outfile, "* 100 * 0 { Capture IR }\n");

if (type_of_file == EPROM_TYPE)
        wr_vector(vecfmt, "Shift IR, for FPGM Instr. LSB..MSB", "10101", outfile);
else
        wr_vector(vecfmt, "Shift IR, for SWrite Instr. LSB..MSB", "11110", outfile);

fprintf(outfile, "* 110 * 0 { opcode entered, exit IR }\n");
fprintf(outfile, "* 110 * 0 { Update IR }\n");
fprintf(outfile, "* 110 * 0 { Select DR Scan }\n");
fprintf(outfile, "* 100 * 0 { Capture DR Scan }\n");
fprintf(outfile, "* 100 * 0 { Shift DR Scan }\n");
```

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```
/***************************************************************************/
/* Begin processing of source bit pattern file */
/***************************************************************************/
/* JTAG TAP Controller is now in Shift-DR state. Next vectors will */
/* begin pumping the Bitmap data in. */

 i = 0; /* number of bits read */
 no_rows = 0;
 data_len = data_len - 1;

 while ((c = getc(infile)) != EOF)
 {
         if (c == ':') /* process comment */
         {
                 fprintf(outfile, "{ ");

                 while ((c = getc(infile)) != EOL)
                 {
                  if (c == EOF) break;

                  fputc(c,outfile);
                 }

                 fprintf(outfile, " }\n");
         }
         else if (c == '*')
         {
                 while ((c = getc(infile)) != ';')
                 {
                  if (c == EOF) break;
                  if (c == EOL) continue;

                  /* if not on final bit, print it */
                  if (i < data_len)
                         fprintf(outfile, " * 10%c * 0\n",c);
                  else
                         /* put in pattern transition for final address */
                         fprintf(outfile, " * 11%c * 0 { end of row %d}\n",
                                                         c,no_rows);

                  i++; /* increment bit count */
                 }
         }

         if (c == ';')
         {
                 i=0;
                 no_rows++;

                 /* write the transition pattern for the next vector */
                 fprintf(outfile, "* 110 * 0 { Update DR }\n");
                 fprintf(outfile, "* 100 * 0 { Run Test Idle }\n");
                 fprintf(outfile, "* 100 * 0 { Run Test Idle (again) }\n");
```

292122–15

```
        fprintf(outfile, "* 110 * 0 { Select DR Scan }\n");
        fprintf(outfile, "* 100 * 0 { Capture DR Scan }\n");
        fprintf(outfile, "* 100 * 0 { Shift DR Scan }\n");
        /* note: both Run-Test-Idle states are necessary for
         SRAM and EPROM configurations. */
    }
}

printf("The number of converted rows: %d\n",no_rows);

/*************************************************************************/
/* Write the final closing vector patterns */
/*************************************************************************/

fprintf(outfile, "* 110 * 0 { Update DR }\n");
fprintf(outfile, "* 100 * 0 { Run Test Idle }\n");

/* if necessary, uncomment these vectors go to Test-Logic-Reset */
/* for (i = 0; i < 5; i++) */
        /* fprintf(outfile, "* 110 * 0 { Test-Logic-Reset }\n"); */

/*************************************************************************/
/* Close all files */
/*************************************************************************/

fclose(infile);
fclose(outfile);
}
```

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APPLICATION NOTE

Designing FLEXlogic Loader Circuits

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October 1993

Order Number: 292139-001

Designing FLEXlogic Loader Circuits

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CONTENTS

INTRODUCTION

This Application Note shows how to create Reconfiguration Loader circuits for the Intel FLEXlogic FPGAs. There are several possible circuits that can be used or created. All can use the JED2JTAG software to control the process.

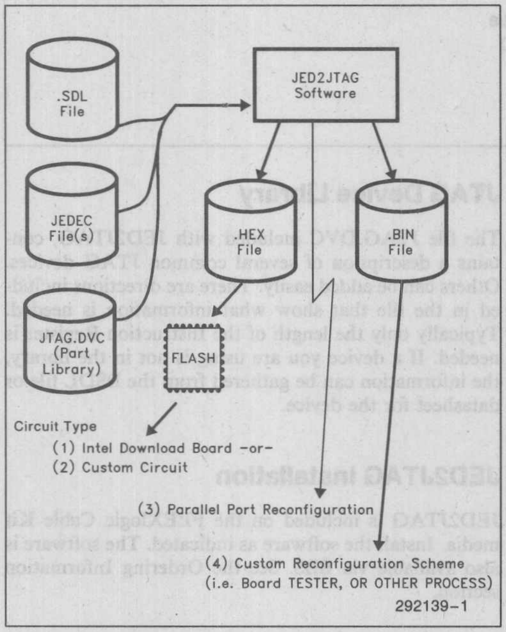

Figure 1. Different Reconfiguration Circuits

JED2JTAG

The JED2JTAG program is a front-end coordinator to several other programs. It handles all of the protocols and coordinates generation of the intermediate and download files.

```
C:> jed2jtag <project.sdl>
```

INPUT FILES

project.SDL	File describing JTAG chain.
*.JED	Device configuration file(s)
JTAG.DVC	Library of JTAG devices
project.DVC	Local project library of JTAG devices If present in the local directory, it is used instead of JTAG.DVC.

CREATED FILES

project.HEX	Hex file for FLASH memory
project.BIN	JED2JTAG Stream of JTAG signals that is used to create a HEX file or is sent to the Parallel Port. Created from .BIT files
*.BIT	JED2JTAG Intermediate file. One for every .JED file. JED2JTAG checks the time of each .BIT file to each .JED. If the .JED is newer, it will recreate the .BIT.

Creating JTAG Chain Description Files (.SDL)

It is assumed that JEDEC file(s) for devices in the JTAG chain have been generated from some design software. The string description file (.SDL) describes the JTAG chain on your circuit board.

The file ***example.sdl*** contains an example of the chain on a prototype board, shown in Figure 2.

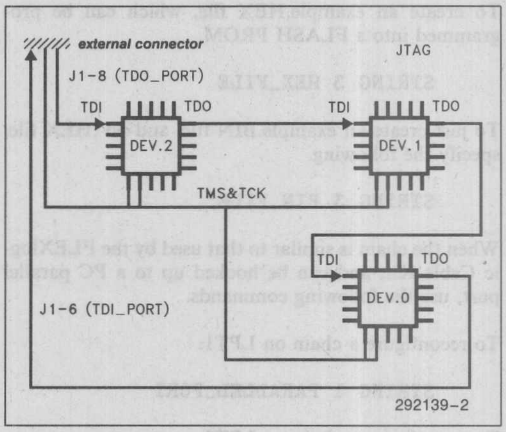

Figure 2. example.sdl JTAG chain

```
|FILE: example.sdl -Simple Prototype Board
{
|          Port_Num   Port_Type
String     3          BIN_FILE
| Port_Num 1 - for LPT1:
| Port_Type must be PARALLEL_PORT or BIN_FILE

|          Loc.  Ref   Device       JEDEC File
DEVICE     0     U3    FX780_132    RIGHT.JED
DEVICE     1     U4    FX780_84     LEFT.JED
DEVICE     2     U1    TI_74BCT8373
}
```

A "|" indicates a comment line.

This prototype board could connect to the Intel Download Board. Figure 2 also shows the connections for the Download Board, and the FLEXlogic Cable kit.

Note that DEVICE 2 does not have a JEDEC file associated with it. Non-FLEXlogic Devices and those without JEDEC files, JED2JTAG will not reconfigure.

STRING Instruction

The STRING instruction in SDL files controls what operations JED2JTAG will take for the JTAG chain.

To create an example.HEX file, which can be programmed into a FLASH PROM.

```
STRING 3 HEX_FILE
```

To just create an example.BIN file, and no .HEX file, specify the following.

```
STRING 3 BIN_FILE
```

When the chain is similar to that used by the FLEXlogic Cable Kit, and can be hooked up to a PC parallel port, use the following commands.

To reconfigure a chain on LPT1:

```
STRING 1 PARALLEL_PORT
```

To reconfigure a chain on LPT2:

```
STRING 2 PARALLEL_PORT
```

JTAG Device Library

The file JTAG.DVC included with JED2JTAG, contains a description of several common JTAG devices. Others can be added easily. There are directions included in the file that show what information is needed. Typically only the length of the Instruction Register is needed. If a device you are using is not in the library, the information can be gathered from the BSDL file or datasheet for the device.

JED2JTAG Installation

JED2JTAG is included on the FLEXlogic Cable Kit media. Install the software as indicated. The software is also available via BBS. See the Ordering Information section.

EXAMPLE: THE INTEL DOWNLOAD BOARD

An example Download Board using an 87C51 is shown to illustrate how to build your own custom Download circuit. The Download Board provides for prototyping hardware systems with FLEXlogic FPGAs already soldered in, but the system hardware logic is not completely debugged.

The Download Board, shown in Figure 3, reloads configurations for Intel FLEXlogic devices in prototype circuit boards. Power for the Loader board is provided by the host environment.

The JTAG chain is described in the .SDL file for the board. This tells the JED2JTAG software what devices are in the chain. JED2JTAG then uses this information to create a .HEX file, which is programmed into a FLASH memory chip.

Upon power-up, or when a reset button on the FPGA Loader Board is pressed, the configuration(s) stored in the FLASH memory on the Loader Board is shifted down the JTAG chain into the FPGAs on the circuit board. After the configuration has been sent, then the RESET signal on the Parallel Port Cable is enabled.

A Custom Download circuit, such as that shown in Figure 4, could be built similarly using other CPUs, such as an i960, other Intel Architectures, or even PLD logic. The pseudo-code for the download algorithm is shown in the HEX FILE DOWNLOAD ALGORITHM Section described later.

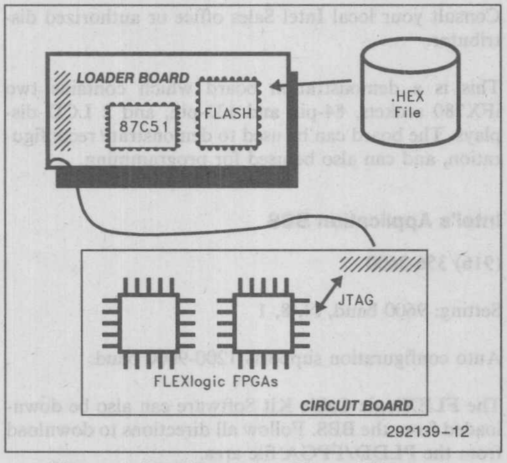

Figure 3. Intel Download Board Example

Steps to use the Intel Download Board

1. Create JEDEC files.
2. Create the .SDL file describing the circuit chain. i.e., *project1.sdl*
3. Run *jed2jtag* and create the .HEX file.(1)

```
c:> jed2jtag project1
```

4. Program the Loader Board FLASH EPROM with the .HEX file, and insert it into the Loader Board socket.
5. Connect the Loader Board to your Circuit Board, and power-up!

NOTE:
1. The examples assume the software runs on PC-DOS.

How to Build the Intel Download Board

The PCB drawings for the Intel Download board are provided on the North American Marketing BBS. They are Gerber files, and have been provided with no guarantees of support or accuracy.

The Bill-of-Materials shown below is also included with the Gerber files.

Schematics for the Download board are included at the end of this document.

With a 256K EPROM, the Download Board has enough capacity to handle approximately 30 FLEXlogic devices in a JTAG chain. For instance, each iFX780 device configuration takes roughly 8K of the FLASH EPROM memory.

Intel Download Board Bill-of-Materials

Item	Qty	Part/Doc Number	Part Name	Value
1	4	C7, C6, C5, C4	CAP	0.1 μF
2	5	R4–R8	CAP	30.1Ω
3	1	R2	CAP	215Ω
4	1	R3	CAP	237Ω
5	1	C3	CAP	4.7 μF
6	2	R1 ,R9	RESISTOR	21.5K
7	2	C1, C2	CAP	33 pF
8	1	S1	SWITCH	
9	1	U3	256X8 FLASH	
10	1	U2	74ALS573B	or equivalent
11	1	U1	87C51FA	
12	1	U1	LED	
13	1	J1	CON20PIN(1)	
14	1	Y1	XTAL	12 MHz

NOTE:
1. AMP part number 1-535542-2, or equivalent.

USING THE PARALLEL PORT FLEXlogic CABLE KIT

The Intel Download board is designed in such a way that it can be directly connected to the host system, or to a flat ribbon cable similar to that used in the FLEXlogic Cable Kit. This makes it interchangable with the Cable Kit, and both methods can be used interchangably for prototyping.

ed directly to your circuit board with a cable from the Parallel Printer Port.

Instead of creating a .HEX file, the .SDL file must be changed so that it will send the configuration via the Parallel Printer Port instead.

Example: **STRING 1 PARALLEL_PORT**

See the STRING commands in the JED2JTAG secton for further information.

CUSTOMIZED LOADER CIRCUITS

As mentioned previously, custom load circuits can be built, similar to the Intel Download Board. There are two choices: 1) a customer circuit with a FLASH memory, or 2) a software download-able circuit

1. A custom FLASH loader can be built similarly to the Loader board using a different CPU, or different memory. For this, you may use the HEX FILE DOWNLOAD ALGORITHM.
2. An example of a software download-able circuit would be an add-in card, where the configuration is downloaded from the disk of a host CPU. In this case, the BIN FILE DOWNLOAD ALGORITHM should be used.

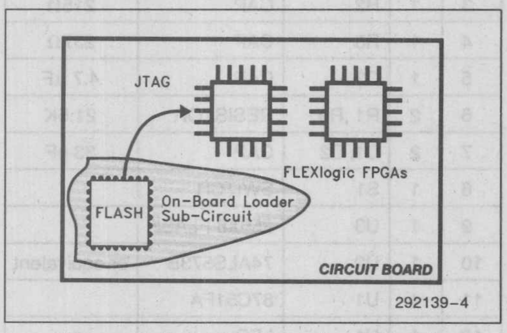

Figure 4. A Custom Download Circuit

The .BIN file contains TMS/TDI pairs for each JTAG clock (TCK). All that is required is a host CPU that drives these signals accordingly.

The BIN file download algorithm describes the contents of these files.

ORDERING INFORMATION

For Intel Literature call (800) 548-4725. Outside of the USA/Canada, please call your local Intel sales office.

JTAG 1149.1 Specifications for In-Circuit Reconfiguration and Programming the iFX780 FPGA", Application Note 390, Order Number 292122-001.

The App-Note contains detailed JTAG timings, and shows how to build JTAG instruction streams from FLEXlogic bitmaps.

FLEXlogic Prototyping Cable Kit

Consult your local Intel Sales office or authorized distributor.

Be sure to get the FLEXlogic Cable Kit Software V1.1 or later to get the JED2JTAG software.

FLEXlogic Demo Board Kit

Consult your local Intel Sales office or authorized distributor.

This is a demonstration board which contains two iFX780 sockets, 84-pin and 132-pin, and 2 LCD displays. The board can be used to demonstrate reconfiguration, and can also be used for programming.

Intel's Application BBS

(916) 356-3600

Setting: 9600 baud, N, 8, 1

Auto configuration supports 1200-9600 baud.

The FLEXlogic Cable Kit Software can also be downloaded from the BBS. Follow all directions to download from the PLDD/FPGA file area.

The DOS Cable Kit Software is delivered in a compressed format. The regular install program should be run in order to uncompress the files.

READEVAL.ME
JED2JTAG.EXE
BIN2HEX.EXE
BIN2PP.EXE
PENGN.EXE
EXAMPLE.SDL
JTAG.DVC

Other files may be included in later versions of the software.

The Intel Download Board Gerber files are available on the BBS as a compressed file.

The 87C51 Assembler Code (with .OBJ and .HEX files) for the example Intel Download Board is also provided in a separate compressed file.

HEX FILE DOWNLOAD ALGORITHM

This pseudo-code shows the algorithm used in the Intel Download Board to read the contents of the FLASH memory, and control the JTAG pin signals.

```
;********************************************************************
;* JTAG STAND-ALONE LOADER PSEUDO CODE
;* *
;* Author: John Logue
;* Revision Record: 06/17/93 JDL Initial Release - Version 1.0
;* *
;* This program typically executes in an embedded controller from an executable memory bank.
;* It transmits data from a local nonvolatile data memory bank to a JTAG (IEEE 1149.1) chain,
;* typically to load the SRAM control memory in the FLEXlogic FPGAs in the chain.
;* *
;* Data is stored in the nonvolatile memory off-line, e.g., with a PROM programmer. It is
;* formatted as a JTAG data stream. Each byte contains TDO/TMS data for 4 TCKs. Bit 0 of
;* each byte is the first TDO, bit 1 is the first TMS, bit 2 is the second TDO,
;* etc. No inversion occurs between memory and TMS/TDO.
;* *
;* The first four bytes in the nonvolatile memory specify the Ending Address + 1. The least
;* significant byte is at data address 0. The JTAG data stream starts at data address 4.
;* *
;* The down-load operation takes place automatically each time the embedded controller is
; *reset, including power-on.
;********************************************************************
; Initialization
 SET LED# port bit ; turn off LED

 DELAY (500) ; delay 500 ms.
; Give time for host JTAG string to completely power-up before beginning.

 CLR TCK port bit ; init TCK to LOW
 CLR RESET# port bit ; init RESET# to LOW (activate host RESET)
 CLR CE# port bit ; enable Flash memory
 CLR LED# port bit ; turn on LED

; Transmit data

 adrs = 0; ; initialize data address and
 last_adrs = (adrs) ; last address + 1 (these are 32 bit values)
 adrs = adrs + 4;

 WHILE (adrs < last_adrs)
 { ; loop until all data is moved from memory to JTAG chain

 ; output 1st TMS/TDO
 MOVE bit 0 of (adrs) to TDO port bit
 MOVE bit 1 of (adrs) to TMS port bit
 SET TCK port bit ; pulse TCK
 CLR TCK port bit

 ; output 2nd TMS/TDO
 MOVE bit 2 of (adrs) to TDO port bit
 MOVE bit 3 of (adrs) to TMS port bit
 SET TCK port bit ; pulse TCK
 CLR TCK port bit

 ; output 3rd TMS/TDO
 MOVE bit 4 of (adrs) to TDO port bit
 MOVE bit 5 of (adrs) to TMS port bit
 SET TCK port bit ; pulse TCK
 CLR TCK port bit

 ; output 4th TMS/TDO
 MOVE bit 6 of (adrs) to TDO port bit
 MOVE bit 7 of (adrs) to TMS port bit
 SET TCK port bit ; pulse TCK
 CLR TCK port bit

 adrs = adrs + 1
 }

; Completion
 SET RESET# port bit ; release host
 SET LED# port bit ; turn off LED
 SET CE# port bit ; disable memory to save power
 SLEEP ; disable embedded controller to save power
```

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BIN FILE DOWNLOAD ALGORITHM

This pseudo-code shows the algorithm translate a .BIN file into JTAG pin signals.

```
;*****************************************************************
;* *
;* JTAG BINARY FILE DOWNLOAD PSEUDO CODE
;* *
;* Author: John Logue
;* Revision Record
;* 06/21/93 JDL Initial Release - Version 1.0
;* *
;*****************************************************************
;* *
;* This program typically executes in a computer, such as a PC,
;* that is capable of reading disk files. It transmits data from
;* a binary file to a JTAG (IEEE 1149.1) chain. Typically, this
;* is to load the SRAM control memory in the FLEXlogic FPGAs in
;* the chain. Normally, the binary file was generated by JED2JTAG.
;* *
;* Data in the binary file is formatted as a JTAG data stream.
;* Each byte contains TDO/TMS data for 4 TCKs. Bit 0 of each
;* byte is the first TDO, bit 1 is the first TMS, bit 2 is the
;* second TDO, etc. No inversion occurs between the file data
;* and TMS/TDO.
;* *
;* Note that the hardware interface to the JTAG chain is not
;* defined. Examples are: Processor port pins, ISA or
;* Microchannel ports, etc. Refer to Standard IEEE 1149.1 for
;* more information on signals TCK, TMS, and TDO.
;* *
;*****************************************************************

; Initialization

 CLR TCK hw bit ; init TCK to LOW
 SET RESET hw bit ; activate RESET to FLEXlogic circuitry
 OPEN bin_file ; open binary file

; Transmit data

 DO
 { ; loop until all data is read from the binary file

        READ byte of bin_file into data_byte

        IF(END_OF_FILE bin_file) break; exit DO loop if end of file

        ; output 1st TMS/TDO
        MOVE bit 0 of data_byte to TDO hw bit
        MOVE bit 1 of data_byte to TMS hw bit
        SET TCK hw bit ; pulse TCK
        CLR TCK hw bit

        ; output 2nd TMS/TDO
        MOVE bit 2 of data_byte to TDO hw bit
        MOVE bit 3 of data_byte to TMS hw bit
        SET TCK hw bit ; pulse TCK
        CLR TCK hw bit

        ; output 3rd TMS/TDO
        MOVE bit 4 of data_byte to TDO hw bit
        MOVE bit 5 of data_byte to TMS hw bit
        SET TCK hw bit ; pulse TCK
        CLR TCK hw bit

        ; output 4th TMS/TDO
        MOVE bit 6 of data_byte to TDO hw bit
        MOVE bit 7 of data_byte to TMS hw bit
        SET TCK hw bit ; pulse TCK
        CLR TCK hw bit
 }

; Completion

 CLR RESET hw bit ; release RESET to FLEXlogic circuitry
 CLOSE bin_file ; close binary file
 MOV TMS,C
 SETB TCK
```

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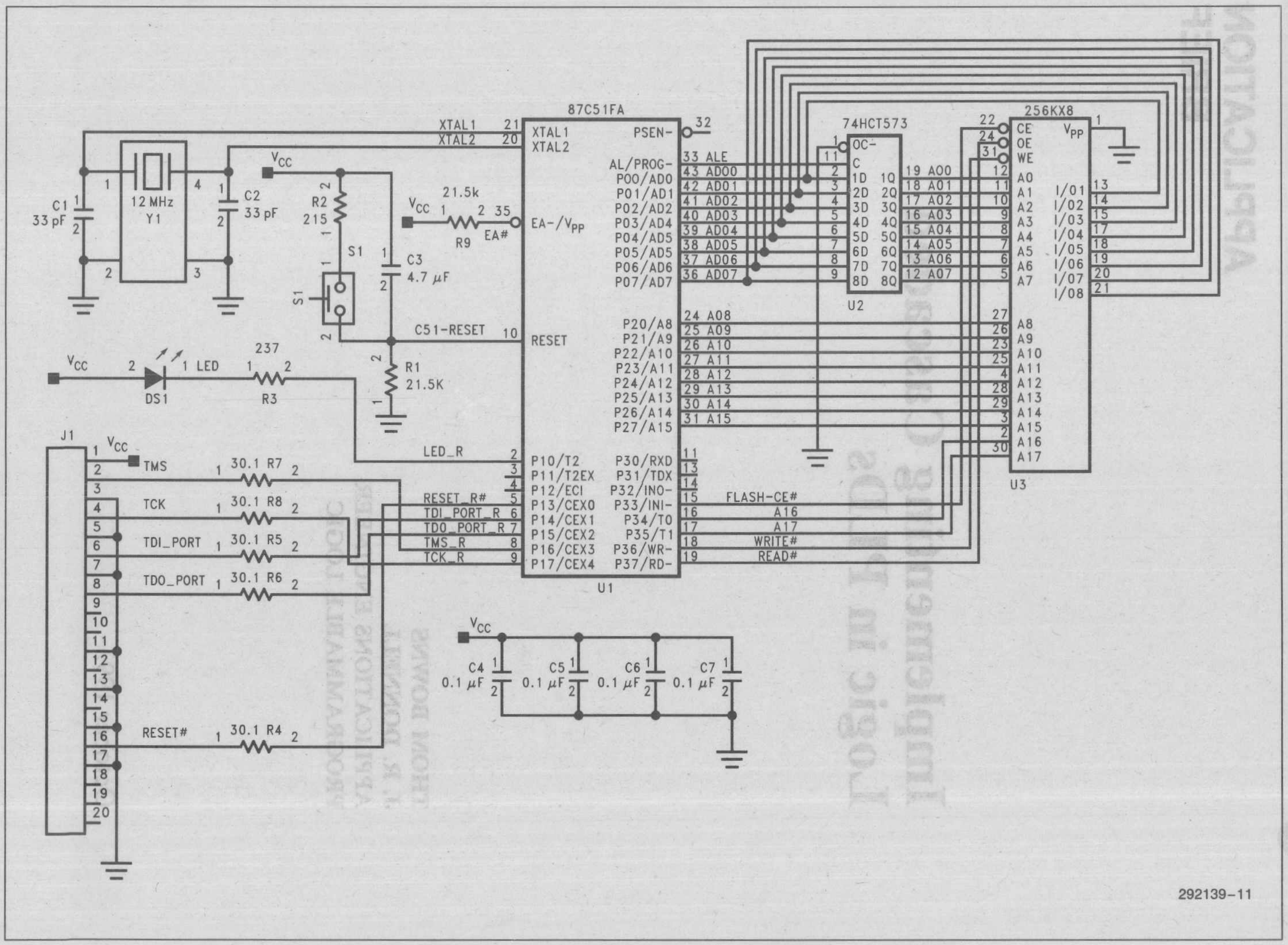

Figure 7. Download Board Schematics

APPLICATION
BRIEF

Implementing Cascaded Logic in PLDs

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October 1993

Order Number: 292003-002

IMPLEMENTING CASCADED LOGIC IN THE PLDs

CONTENTS

3

PROBLEM

Designs that utilize numerous levels of cascaded logic often result in excessive product terms when expressed in the sum-of-products form. Although this poses no problem when designing with discrete logic, PLDs are generally optimized for the sum-of-product form. This stems from the architecture of the basic Macrocell.

Macrocells typically consist of a programmable AND array feeding a fixed width OR gate. Most Intel PLDs (with a few exceptions) have a fixed OR gate width of eight product terms. For most applications, eight available product terms are sufficient. However certain designs require logic to be cascaded, which usually causes product term requirements to expand geometrically. One example where product terms become an issue is cascaded exclusive-OR (XOR) circuits. Here the number of product terms increase by 2 to the nth power, where n equals the number of XOR gates. If the number of product terms exceeds eight, the equation may not fit in the PLD macrocell.

SOLUTION

There is a simple solution to reduce the product term requirements when using cascading XOR (or other) logic. Figure 1 shows a circuit cascading five XOR gates. As designed, this circuit expands to 32 product terms (p-terms) when expressed in the minimized sum-of-products form. Figure 3 shows the minimized equations expressed in PLDasm language, which is the logic description language used with Intel's PLDshell Plus development tool.

An easy solution to fitting this logic into an PLD is to cascade three exclusive XORs together and then send the result through a combinatorial NODE. This has the effect of gathering the 8 p-terms required to implement a three XOR cascade into a single term. Figure 4 shows the PLDasm file for this implementation, where the gathering term is called MCELL. Note the reduction in the p-terms required by the signal OUT, as compared to Figure 3.

The penalty in this method is the added delay needed for the feedback path, and the use of an additional macrocell resource. The worst case t_{pd} (circuit input to output delay) for the circuit in Figure 2 would be twice the specified t_{pd} for the target PLD. For the 7.5 ns 85C220, the t_{pd} would be 15 ns worst case.

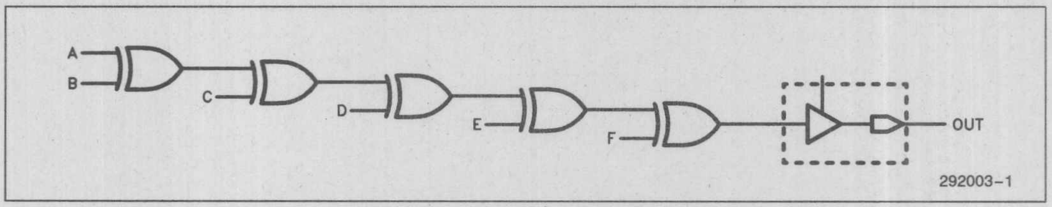

Figure 1. Cascaded Exclusive-ORs

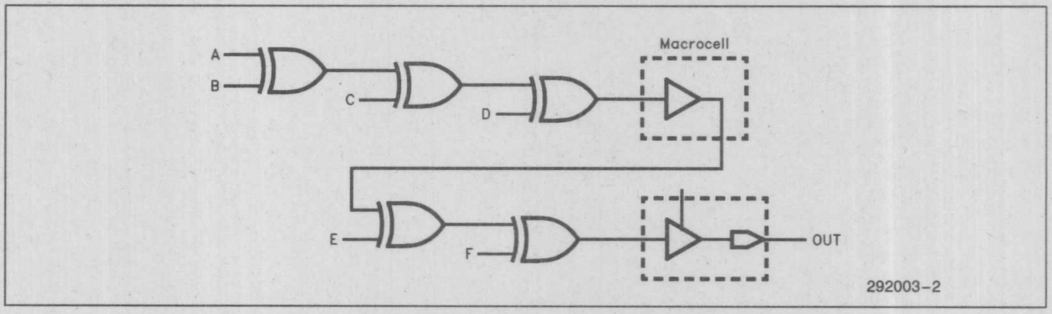

Figure 2. Cascaded Exclusive-ORs using Combinatorial Feedback

```
TITLE CASCADING XOR GATES -- NO FEEDBACK

CHIP  XOR1 85C220

;inputs
PIN        A
PIN        B
PIN        C
PIN        D
PIN        E
PIN        F

;outputs
PIN        OUT

EQUATIONS

OUT = F * /E * /D * /C * /A * /B
    + F * /E * /D * /C * A * B
    + F * /E * /D * C * A * /B
    + F * /E * /D * C * /A * B
    + F * /E * D * C * /A * /B
    + F * /E * D * C * A * B
    + F * /E * D * /C * A * /B
    + F * /E * D * /C * /A * B
    + F * E * D * /C * /A * /B
    + F * E * D * /C * A * B
    + F * E * D * C * A * /B
    + F * E * D * C * /A * B
    + F * E * /D * C * /A * /B
    + F * E * /D * C * A * B
    + F * E * /D * /C * A * /B
    + F * E * /D * /C * /A * B
    + /F * E * /D * /C * /A * /B
    + /F * E * /D * /C * A * B
    + /F * E * /D * C * A * /B
    + /F * E * /D * C * /A * B
    + /F * E * D * C * /A * /B
    + /F * E * D * C * A * B
    + /F * E * D * /C * A * /B
    + /F * E * D * /C * /A * B
    + /F * /E * D * /C * /A * /B
    + /F * /E * D * /C * A * B
    + /F * /E * D * C * A * /B
    + /F * /E * D * C * /A * B
    + /F * /E * /D * C * /A * /B
    + /F * /E * /D * C * A * B
    + /F * /E * /D * /C * A * /B
    + /F * /E * /D * /C * /A * B
```

292003-5

Figure 3. PLDasm Equations for Figure 1

```
TITLE CASCADING XOR GATES -- MACROCELL FEEDBACK USED

CHIP  XOR2 85C220

;inputs
PIN        A
PIN        B
PIN        C
PIN        D
PIN        E
PIN        F

;buried
NODE       MCELL

;output
PIN        OUT

EQUATIONS

MCELL = D * /C * /A * /B
      + D * /C * A * B
      + D * C * A * /B
      + D * C * /A * B
      + /D * C * /A * /B
      + /D * C * A * B
      + /D * /C * A * /B
      + /D * /C * /A * B

OUT = F * /MCELL * /E
    + F * MCELL * E
    + /F * MCELL * /E
    + /F * /MCELL * E
```

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Figure 4. PLDasm Equations for Figure 2

APPLICATION BRIEF

The 85C224 Clock Driver Low Output Skew PLD

3

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October 1993

Order Number: 292117-001

The 85C224 Clock Driver Low Output Skew PLD

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CONTENTS PAGE

1.0 INTRODUCTION

With the continuing demand for performance driving the need for high frequency microprocessors and information systems (i.e., the Pentium™ processor, i486 microprocessors, and PCI Bus), designers of these complex systems are faced with the task of completing numerous system instructions within a shrinking window of time; from a 30 ns clock period @33 MHz to 15 ns @66 MHz. Many recent logic devices feature faster propagation delays, but this is not always enough. Designers are now seeking relief from these timing constraints by using higher quality clock driver devices, as well. At the current stage of advanced processor system development, clock signal timing accuracy is more important than ever. Designers must be able to drive clocks to various regions of the board using special clock driver chips featuring extremely low output pin-to-output pin skew (T_{OS}).

Intel programmable logic devices are a highly effective, low cost solution to the output skew minimization problem associated with high frequency clock distribution. The 85C224 Programmable Logic Device is designed with extremely low output pin skew. In addition, it offers superior output signal quality including fast rise and fall times. Combined with the flexibility of programmable logic the 85C224 can be programmed in a variety of clock driver configurations with maximum output pin skew of less than 400 ps.

Unlike dedicated clock drivers that have limited flexibility, Intel's 85C224 can be configured into different types of clock drivers. This flexibility allows the designer to satisfy several clock driver needs with one device. In addition, while dedicated clock drivers can perform only one function (typically distribution or division), the flexible 85C224 satisfies programmable logic needs such as control signals and widespread glue logic needs. Only with a minimized output skew PLD like the 85C224 can a designer implement clock distribution, division, and programmable logic with a single device.

Not only is the 85C224 flexible, but it is also cost effective. In comparison, dedicated clock driver devices with equivalent output skew range in cost of up to 10 times more than the 85C224! If the extrinsic value of the flexible programmable logic features were included in this cost comparison, the cost savings multiple would be even greater!

For power intensive systems, like notebook PCs, low power consumption clearly becomes important. Fortunately, the 85C224 has always incorporated low power CMOS technology (typical I_{CC} = 60 mA). The 85C224 is an ideal clock driver for low power notebook PC's and portable systems.

This Application Brief describes how the flexibility and extremely low output skews of the 85C224 meet the clock driver needs of high clock speed systems. Two types of clock drivers are discussed, the simple gate driver or distributor and the frequency divider.

2.0 CLOCK DISTRIBUTOR

The 85C224 PLD performs as a simple gate driver or clock signal distributor when its outputs are programmed to replicate an input clock. In this configuration, the input clock signal is replicated and driven from between 1 to 8 output pins (see Figure 1).

From the outputs, the clock lines are then distributed to numerous regions of the system layout which require a synchronous version of the system clock as an input. Each of the output clocks has the same frequency and duty cycle as the original input clock. Output pin skew in this mode will typically be less than 250 ps for the low to high transition and 130 ps for the high to low transition (see Table 1). This configuration will drive/distribute clocks up to a maximum clock frequency of 133 MHz. A simple PLDasm program is shown below where the outputs (IO's) follow the clock input (inp1):

```
EQUATIONS
    io1 = inp1
    io1.TRST = VCC
    io2 = inp1
    io2.TRST = VCC
```

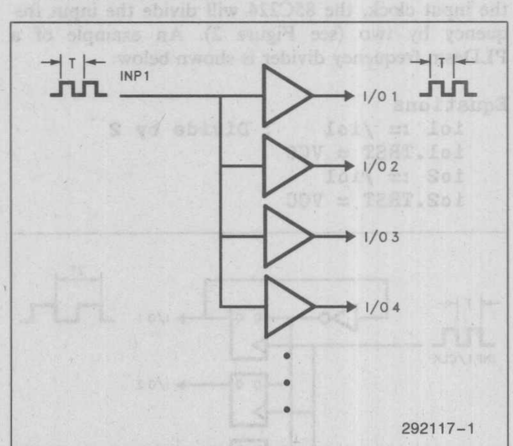

Figure 1. Gate Driver

Design Recommendations: The lowest output skew can be obtained by defining Input 6 (pin 6) as the clock input of choice. This path has been determined by engineering to provide the lowest output pin skew.

The best way to ensure a clean output clock with limited ground bounce is to connect all unused input pins and optional ground pins to a clean ground plane. In addition, connect all optional power pins to a clean power supply.

The output skew that is noted in Table 1 was determined with a configuration driving all 8 outputs and measuring worst case skew between all combinations of outputs. If less than eight output clocks are needed then the designer can attain even better output skew by selecting the optimal output pins which maintain progressively better output skew characterizations. For the low to high transition, the output pin skew decreases as used clock outputs are closer to V_{CC}, pin 28. In addition, unused output pins should be tied to ground. For example, a 1 to 4 clock distribution using the first four I/Os (and grounding I/Os 5–8) provides output pin skew as low as 200 ps across all four outputs.

Conversely, for the high to low transition the skew increases as you move away from the ground pin. By grounding I/O1 and I/O8 the skew for the remaining pins are reduced to 100 ps. For systems requiring the least skew possible ($\leq$100 ps), triggering from the falling clock edge will provide the smallest clock skew achievable by the 85C224 (or any device on the market).

3.0 FREQUENCY DIVIDER

For systems that require multiple clock frequencies (i.e., 66 MHz and 33 MHz) or a clock signal with 50% duty cycle, a clock frequency divider can be used. By programming the outputs to toggle on the rising edge of the input clock, the 85C224 will divide the input frequency by two (see Figure 2). An example of a PLDasm frequency divider is shown below:

```
Equations
    iol := /iol     ; Divide by 2
    iol.TRST = VCC
    io2 := /iol
    io2.TRST = VCC
```

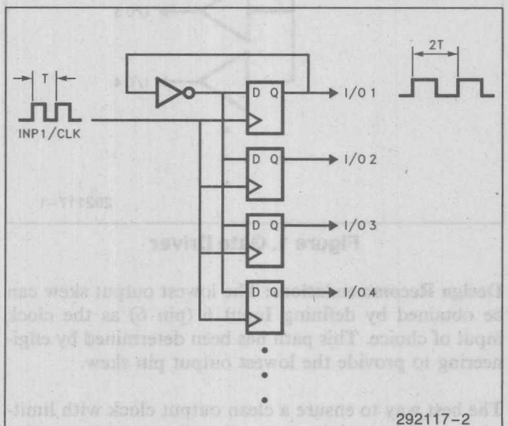

Figure 2. Frequency Divider

In this mode the 85C224 can achieve typical output skews of 130 ps for the high to low transition and 200 ps for the low to high transition (see Table 1). These superior output skews are achieved as a result of the close proximity of the toggling registers to the output pin. The reduced signal path in the divider configuration translates into a narrowing of the potential variation in the output pin skew; hence, even less output pin skew.

The maximum frequency of the 85C224-100 clock divider is 100 MHz input with a 50 MHz output. The 85C224-10 will divide clock inputs up to 58 MHz and is offered at an even lower price.

As with the clock distributor, the best way to insure a clean output clock signal and limited ground bounce is to connect all unused input pins, other than the clock input pin, (INPUT 1) to a clean ground plane. Also, connect the pins labeled "no connection" to ground and Pin 1 to V_{CC}. The skew increases for I/Os as they move farther from the V_{CC} pin. Conversely, for the high to low transition the skew increases for outputs farthest from the ground pin. This information is often useful when routing low skew priority signals.

4.0 INVERTED OUTPUTS

In addition to low output pin skews and a variety of clock driver configurations the 85C224 can be programmed to invert any of the eight outputs. This feature reduces skew and saves parts as it eliminates the need to route a clock through an inverter chip to provide the capability of triggering on the falling edge of the clock. The inversion is done with a negligible increase in output skew. From a software standpoint, the inversion can be accomplished by programming the "invert" bit in the PLD source code. In PLDasm, inverting the signal is accomplished by using the active-low declaration "/" in front of the output signal that is to be inverted.

5.0 RISE AND FALL TIMES

The rise and fall times of the 85C224 meet the needs of high-speed system applications such as the Pentium™ microprocessor, while controlling ground bounce. Typical rise times are under 1.4 ns and typical fall times are under 1000 ps. Rise and fall times were measured from 0.8V to 2.0V with a 50 pF load.

6.0 TEMPERATURE DEPENDENCE

As the temperature approaches 85°C, the output skew of the 85C224 remains under 500 ps. In combinatorial logic, the output skew will increase to typical values of 350 ps for the low to high transition and 230 ps for the high to low transition. In registered mode the skew at 85°C is typically 200 ps for the low to high transition and 250 ps for the high to low transition.

7.0 POWER SAVINGS

The 85C224 is perfect for laptop system as the 1-micron CHMOS IIIE EPROM process allows it to consume less power than bipolar PALs and even CMOS GALS. Since there is an output enable P-term for every macro cell, a power management scheme can be programmed into the array that will disable macrocells according to the power requirements of the system. In this case, the 85C224 can perform three functions: power management, clock distribution and division, further demonstrating the high utility and flexibility of this device.

8.0 TOOLS AND SUPPORT

Complete design files and JEDEC files associated with this brief can be downloaded via the PLDshell Plus BBS. The number is (916) 985-2308. You must be a registered PLDshell Plus user to log in.

PLDshell Plus software is available from Intel Literature 1-800-548-4725 or your local Intel sales office.

9.0 CONCLUSION

The 85C224 is an excellent choice for low skew clock driver applications. The PLD offers flexibility which allows the designer to configure the device into an assortment of clock driving implementations: distribution, division, and inversion. The device fundamentally provides low power and programmable logic functionality to meet the needs of control logic, state machines, and power management—all with a single device, the 85C224. The extremely low skews offered by the 85C224 are as good and better than comparable single function clock drivers; for a fraction of the cost!

High performance, low power, minimal output skew, programmable capabilities, low cost and overall flexibility make the 85C224 an intelligent solution for your design needs.

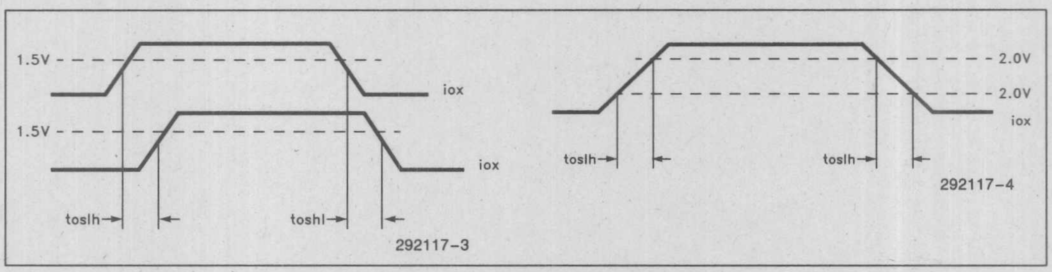

Figure 3. Measurements

Table 1. 85C224-10 Characteristic Data

Symbol	Parameter	V_{CC}	$T_A = 25°C$ $C_L = 50$ pF Typ	$T_A = 25°C$ $C_L = 50$ pF Max	$T_A = 75°C$ $C_L = 50$ pF Typ	$T_A = 75°C$ $C_L = 50$ pF Max	Units
Comb t_{OSHL}	Combinatorial I/O to I/O Skew High to Low Transition	5.0V	130	250	175	250	ps
Comb t_{OSLH}	Combinatorial I/O to I/O Skew Low to High Transition	5.0V	250	400	200	300	ps
Reg t_{OSHL}	Registered I/O to I/O Skew High to Low Transition	5.0V	150	225	150	225	ps
Reg t_{OSLH}	Registered I/O to I/O Skew Low to High Transition	5.0V	200	300	200	250	ps
t_r	Rise Time (0.8V–2.0V)	5.0V	1.3	1.5	1.2	1.4	ns
t_f	Fall Time (0.8V–2.0V)	5.0V	1.0	1.2	1.1	1.1	ns
f_{MAX}	Max. Counter Freq. $1/t_{CNT}$ Internal Feedback	5.0V	80	62.5	80	62.5	MHz
f_{MAX}	85C224-100 Internal Feedback $1/t_{CNT}$	5.0V		115		115	MHz

APPLICATION NOTE

85C220/85C224 Design Guide

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INTEL CORPORATION
PROGRAMMABLE LOGIC APPLICATIONS

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INTRODUCTION

In the past decade and half, system designers have come to depend on PLDs (Programmable Logic Devices) to implement random logic and interface circuits because of the low cost and high performance these devices offer. Bipolar PLDs (commonly called PALs*) were the first class of devices to become a common part of the designer's repertoire. As power requirements and heat dissipation of bipolar PLDs became a design and/or reliability limiter in the mid-1980's, designers began using CMOS PLDs (GALs** and PLDs).

In 1989 and 1990 Intel began shipping its fast 85C220 and 85C224 PLDs. These PLDs are supersets of common 20-pin and 24-pin PALs/GALs. Both the 85C220 and 85C224 exhibit extremely fast speeds, low power consumption, and high integration, which make them ideally suited for high-speed microcomputer system applications. This application note covers the architectural features that distinguish these Intel PLDs (also called μPLDs for Microcomputer Programmable Logic Devices) from their competition. It also covers performance, power requirements, and heat dissipation. Finally, it describes electrical characteristics of the devices, along with guidelines for taking best advantage of device behavior while mitigating tradeoffs that may be encountered.

PERFORMANCE

PLDs can be measured in terms of propagation delay (t_{PD}) or state machine frequency ($1/t_{SU} + t_{CO}$). In terms of propagation delay, performance of the first CMOS PLDs lagged behind bipolar PLDs by 15 ns–20 ns. This gap has been closed to 2.5 ns or less. In terms of state machine frequency, CMOS PLDs also historically lagged bipolar PLDs significantly. State-machine performance of Intel PLDs equals or surpasses bipolar PLDs. Table 1 lists the key speed parameters of 16-series and 20-series PALs and GALs, and the 85C220/85C224. The additional performance provided by the 85C220/85C224-80 can allow faster state machine designs or provide additional margin for existing designs. The 85C220/85C224-7 provide fast combinatorial logic at significantly reduced power consumption over bipolar devices.

Table 1. PAL/GAL/85C220/85C224 Performance Comparison

Parameter	16R8-D 20R8-D	16R8-E 20R8-E	16V8-10 20V8-10	85C220-7 85C224-7	85C220-80 85C224-80	85C220-100 85C224-100	Units
t_{PD}	10	*7.5*	10	*7.5*	10	7.5	ns
t_{SU}	10	*7*	10	*7*	*7*	4.5	ns
t_{CO}	7	6.5	8	*6.5*	*5.5*	5.5	ns
f_{CNT1}	58.8	74	55.5	74	*80*	100	MHz
t_{CNT}	16.5	10	Not Avail.	*10*	*10*	10	ns
f_{CNT2}	60	*100*	Not Avail.	*100*	*100*	115	MHz
f_{MAX}	62.5	100	62.5	100	*111*	115	MHz

Italics indicate fastest specification for that category.

Parameter Definitions:

t_{PD} — Propagation Delay, Input or I/O to Output Valid Delay
t_{SU} — Input or I/O Setup Time to Clock
t_{CO} — Clock to Output Valid Delay
f_{CNT1} — Max. External Counter Frequency ($1/t_{SU} + t_{CO}$)
t_{CNT} — Clock to Feedback Setup for Next Clock—Internal Path
f_{CNT2} — Max. Internal Counter Frequency ($1/t_{CNT}$)
f_{MAX} — Max. Pipelined Frequency

*PAL is a registered trademark of Advanced Micro Devices.
**GAL is a registered trademark of Lattice Semiconductor, Inc.

ARCHITECTURAL SUPERSET FEATURES

This section summarizes the architectural limitations of PALs and GALs and describes the superset features of the 85C220/85C224 devices.

Standard PALs and Their Limitations

Designers are familiar with common 16-series and 20-series PAL and GAL devices. The layout is standard with clock, output enable, inputs and outputs in the same pin locations across families of devices (all signals on R4, R6, and R8 devices; inputs and outputs on L8 devices). Seven or eight p-terms (product-terms) are available for logic implementation. The major task with PALs is to pick the device with the desired range of inputs and registers. The designer then fits the design into the device, modifying the design to fit the architecture of the device.

Architectural limitations that experienced PAL users have all encountered include:

1. One active output polarity per device (usually active low)
2. Only 7 SOP (Sum-of-Products) p-terms on combinatorial outputs
3. Unusable pin on R4, R6 and R8 devices if the dedicated OE is not used
4. No feedback on the outside macrocells (#0 and #7) of L8 devices
5. Wasted resources in cases where the number and type of outputs does not match device resources. (For example, a 16R-series or 20R-series PAL cannot implement a design requiring 5-registered and 3-combinatorial outputs. An R6 would be needed to implement the 5 registers and 2 of the 3 combinatorial outputs. One register in the R6 would not be used and the 3rd combinatorial output would have to be implemented in discrete logic or in an additional PAL.)

GALs Provide a Partial Improvement

The GAL architecture overcomes some of these limitations. GALs offer programmable output polarity so that any output can be active high or active low. Any combination of registered/combinatorial outputs can be implemented in a single device. But several architectural limitations are still present in GALs:

1. Only 7 SOP p-terms are available for combinatorial outputs if a p-term is used for an OE signal
2. The dedicated OE pin is unusable if registers are used but the OE control is not needed
3. No feedback on the outside macrocells (#0 and #7) when the device is configured for all combinatorial outputs.

Thus while GALs provide greater flexibility than PALs, GAL users still find themselves designing around the architectural limitations.

85C220/85C224—The Total Solution

With the Intel 85C220/85C224 PLDs, the architectural limitations of PALs and GALs have been overcome. The 85C220 is an architectural superset of 16-series (20-pin) PALs and GALs, while the 85C224 is an architectural superset of 20-series (24-pin) devices. Let's look at the superset features.

SOP Invert

Figure 1 compares the macrocells (output structures) of PALs, GALs, and the 85C220/85C224. Note that the 85C220/85C224 and the GAL contain a programmable invert option to allow each output to be individually configured as active low or active high. This feature allows logic compilers to use DeMorgan's inversion techniques to fit equations into an 85C220/85C224 that would not fit into a standard PAL. Larger equations will fit into the 85C220/85C224 that will not fit in 16-series and 20-series PALs.

Independently Configurable Outputs

The 85C220/85C224 and the GAL allow any combination of registered and combinatorial outputs in a single device. This feature means that designers will not have to leave outputs unused as with PALs.

Output Enable P-Term

Figure 1 also shows that the 85C220/85C224 contains an output enable p-term in addition to the 8 SOP p-terms (9 p-terms total). L8 PALs and GALs borrow one of the SOP p-terms to implement an OE equation, leaving only 7 p-terms to implement the SOP. In cases where an SOP equation requires all 8 p-terms, the PAL/GAL designer must route part of the equation through another macrocell first (and accept the additional delay), or choose a different device. Since the 85C220/85C224 does not have this limitation, larger designs will fit more often in Intel PLDs.

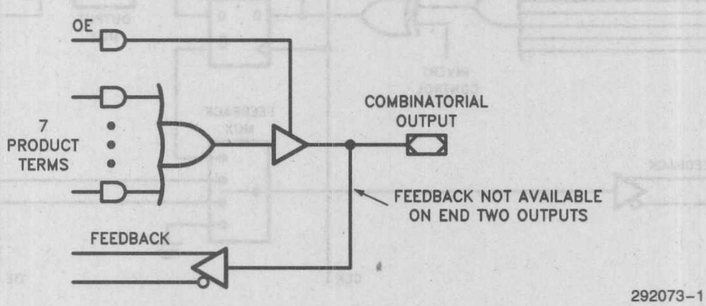
Output Feedback

Note that the two outside macrocells (#0 and #7) on L8 PALs and GALs configured for combinatorial operation do not allow feedback to the logic array. If this feedback is needed, a different device must be chosen.

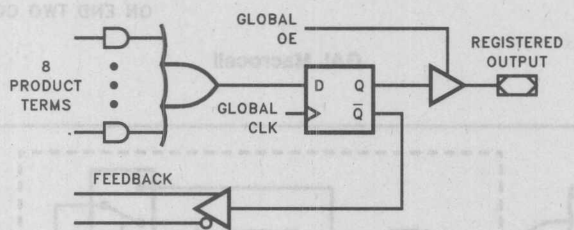
This may mean switching to an 18P8, 18CV8, etc., or moving up to a larger device with more inputs. All 8 outputs on the 85C220/85C224 can feed back a combinatorial signal from the I/O pin to the logic array. The need to change devices or move up to a larger device is diminished for 85C220/85C224 users.

No Dedicated Output Enable Pin

When using PALs and GALs configured for registered operation, the OE pin can only be used as an OE signal. If no OE function is needed, the pin must be tied high; it cannot be used as a standard input to the logic array. The 85C220/85C224, however, does not contain a dedicated output enable pin, making these devices more flexible than PALs and GALs. With the 85C220/85C224, if the registers do not require an output enable, the internal p-term can hold the output buffers in the enabled state. The corresponding pin can then be used as a dedicated input. If a global OE is needed, then the OE p-terms for all eight macrocells can be programmed identically.

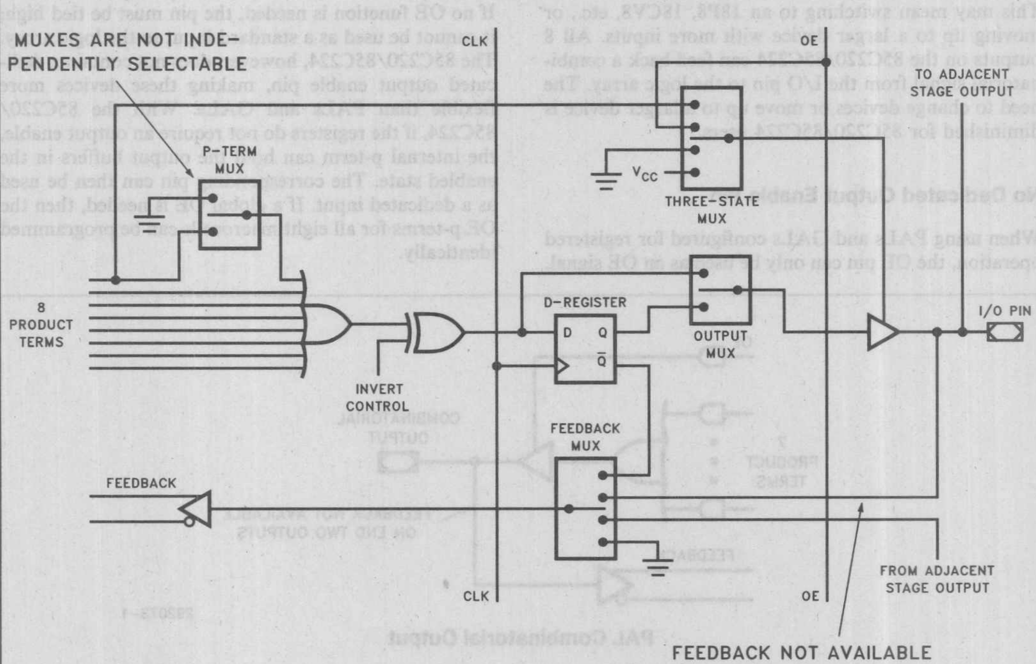


PAL Combinatorial Output



PAL Registered Output

Figure 1. Output/Macrocell Architecture Comparison



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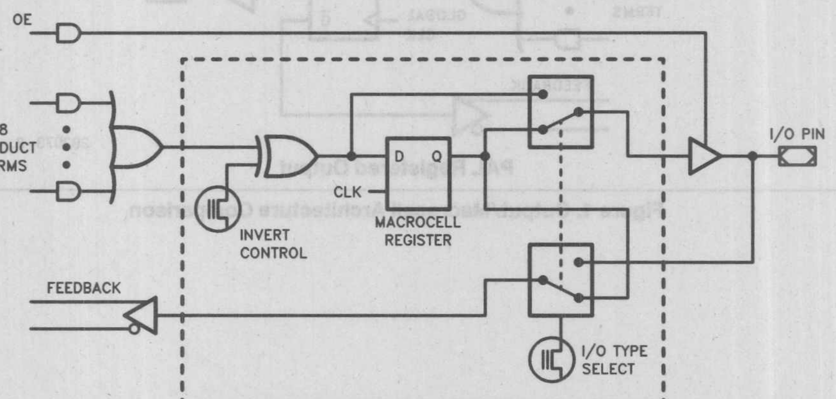
GAL Macrocell



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85C220/85C224 Macrocell

Figure 1. Output/Macrocell Architecture Comparison (Continued)

Architecture Summary

The combination of PAL/GAL compatibility along with the superset features on the 85C220/85C224 μPLDs allows more logic to be implemented in these devices than in standard PAL/GAL architectures. The need to stock several different PAL/GAL architectures (in multiple packages) is reduced when using the 85C220/85C224 architectures. 85C220/85C224 users will find that their designs outgrow their PLDs significantly less often than PAL/GAL users.

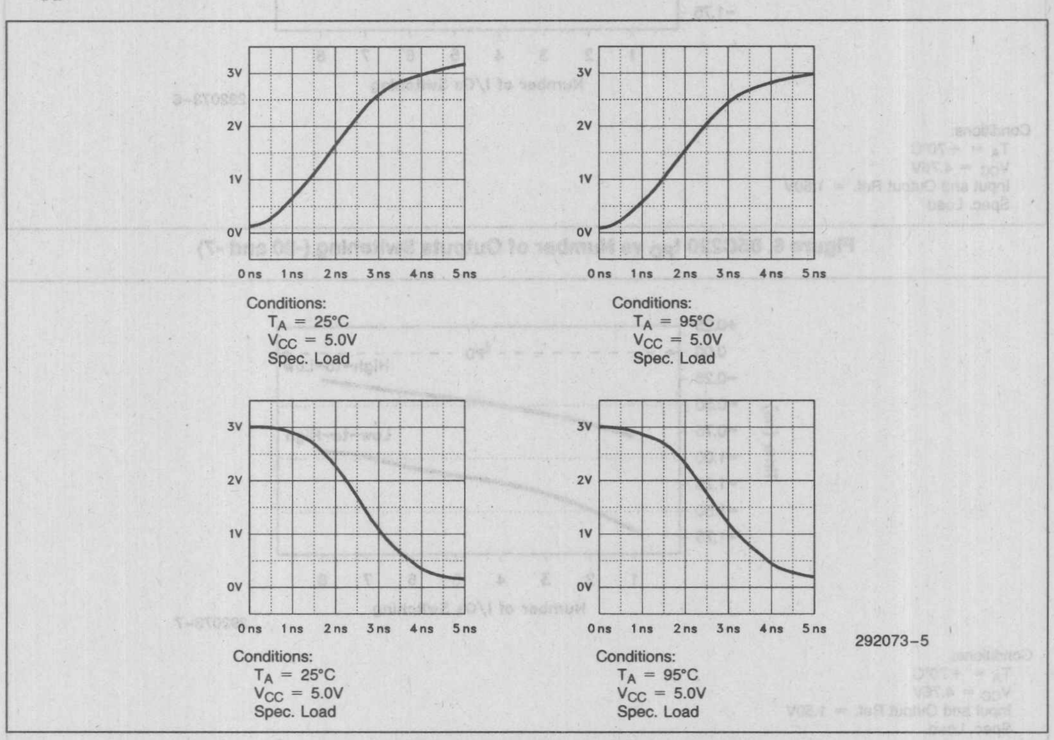
ELECTRICAL CHARACTERISTICS

This section provides characterization data for the 85C220/85C224 that can be of great help to designer's working on high-speed systems. Information is presented in the following order:

- Output Slew Rates
- t_{PD} Characteristics
- t_{CO} Characteristics
- I_{OL} Characteristics
- Tracking Critical Parameters over Temperature
- Ground Bounce/Noise on Unswitched Outputs

Output Slew Rates

Output buffers for 85C220/85C224-80 devices have a nominal slew rate of 1 V/ns low-to-high and 1.5 V/ns high-to-low. At 95°C, the slew rate slows slightly to 0.8 V/ns low-to-high, and 1.2 V/ns high-to-low. This slew rate is fast enough to meet the requirements of all data sheet specifications, but slow enough to minimize problems such as ground bounce and transmission line effects. Figures 2 through 5 show slew rates as measured on 85C220/85C224-80 devices.



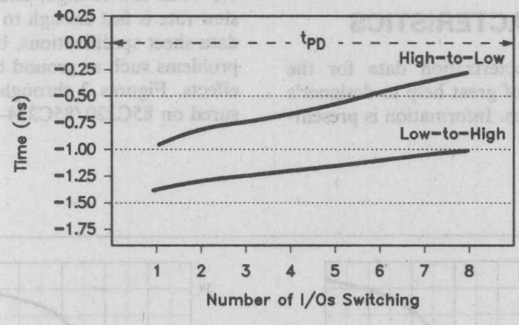
Figures 2–5. 85C220/85C224-80 Output Slew Rates

t_{PD} Characteristics

This section shows how propagation delay for the 85C220/85C224 PLDs is affected by factors that vary from one application to another.

t_{PD} vs Number of Outputs Switching

As the number of device outputs switching simultaneously increases, average propagation delay through devices also increases. This increase is related to the ability of package power and ground leads to channel the additional current. Figures 6 and 7 show the relation of t_{PD} to the number of outputs switching for the 85C220 and 85C224, respectively. Note that this data reflects worst case values. Typical parts can be 1 ns–2 ns faster. This data helps designers estimate how much margin exists in a high-speed design.



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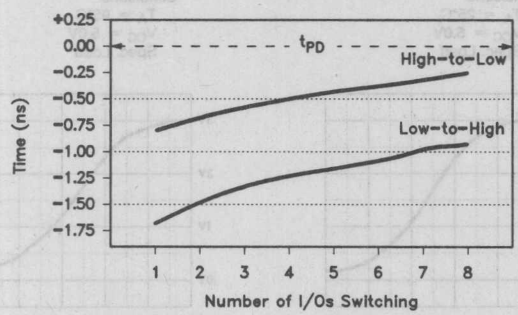
Conditions:
$T_A = +70°C$
$V_{CC} = 4.75V$
Input and Output Ref. = 1.50V
Spec. Load

Figure 6. 85C220 t_{PD} vs Number of Outputs Switching (-80 and -7)



292073-7

Conditions:
$T_A = +70°C$
$V_{CC} = 4.75V$
Input and Output Ref. = 1.50V
Spec. Load

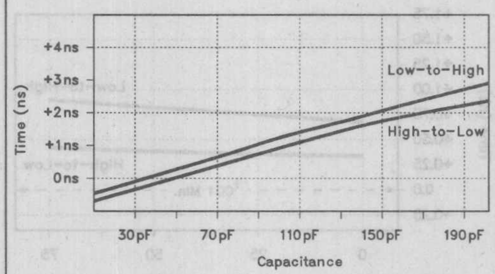
Figure 7. 85C224 t_{PD} vs Number of Outputs Switching (-80 and -7)

t_{PD} vs C_L

Knowledge of how PLDs behave as capacitive loading is increased is an important consideration when designing high-speed systems. Figure 8 shows derating from specified values for a typical 85C220/85C224-80 at high temperature, low V_{CC} conditions for both low-to-high and high-to-low transitions as capacitance increases. These characteristics can help designers trade off system margin for additional delays incurred due to higher capacitive loads.

t_{PD} vs Number of P-Terms Switching

As additional p-terms for a macrocell are used, internal device loading causes propagation delay to increase or decrease slightly. Figure 9 shows this slowdown for the 85C220/85C224-80 and -7 at room temperature conditions with 2 outputs switching. Data is shown for both low-to-high and high-to-low transitions.



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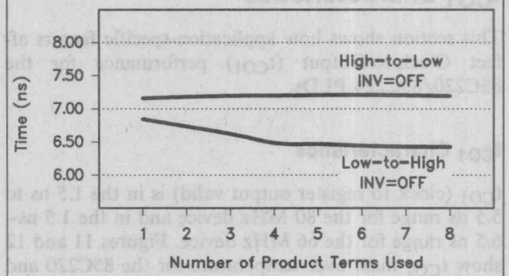
Conditions:
T_A = +70°C
V_{CC} = 4.75V

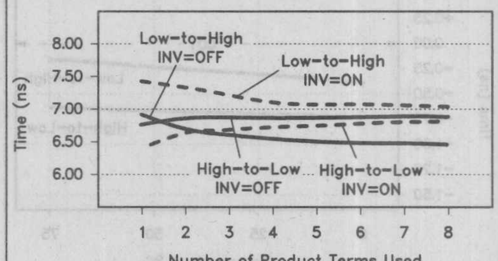
Figure 8. 85C220/85C224-80 t_{PD} vs C_L



292073-9

Conditions:
T_A = 25°C
V_{CC} = 5.0V
Input and Output Ref. = 1.50V
Spec. Load
2 Outputs Switching

Figure 9. 85C220 t_{PD} vs Number of P-Terms Switching



292073-10

Conditions:
T_A = +25°C
V_{CC} = 5.0V
Input and Output Ref. = 1.50V
Spec. Load
2 Outputs Switching

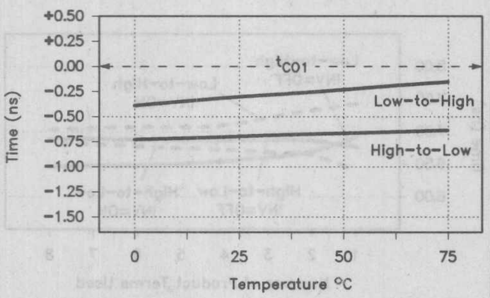
Figure 10. 85C224 t_{PD} vs Number of P-Terms Switching

t_{CO1} Characteristics

This section shows how application-specific factors affect Clock-to-Output (t_{CO1}) performance for the 85C220/85C224 PLDs.

t_{CO1} Characteristics

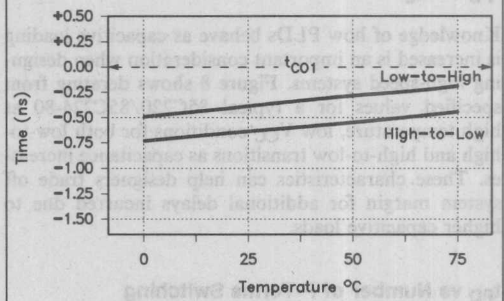
t_{CO1} (clock to register output valid) is in the 1.5 ns to 5.5 ns range for the 80 MHz device and in the 1.5 ns–6.5 ns range for the 66 MHz device. Figures 11 and 12 show t_{CO1} max. over temperature for the 85C220 and 85C224, respectively. This data was taken with 8 outputs switching at high temperature. For some designs, t_{CO1} minimum is also a key parameter. Figures 13 and 14 show t_{CO1} min. under worst case (fastest) conditions (low temperature, high V_{CC}, 1 output switching, probe capacitance only). Figures 15 and 16 show t_{CO1} for the devices with 1 to 8 outputs switching under worst case conditions (high temperature, low V_{CC}).



292073-11

Conditions:
V_{CC} = 5.0V
Spec. Load
8 Outputs Switching

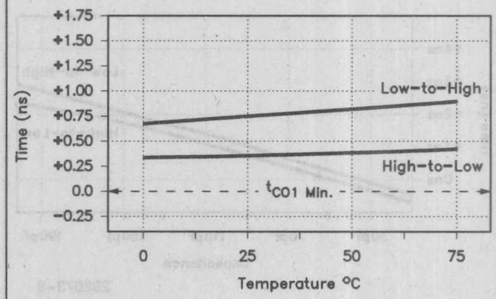
Figure 11. 85C220-80 t_{CO1} vs Temperature (Max.)



292073-12

Conditions:
V_{CC} = 5.0V
Spec. Load
8 Outputs Switching

Figure 12. 85C224-80 t_{CO1} vs Temperature (Max.)



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Conditions:
V_{CC} = 5.25V
Scope Load Only
1 Output Switching

Figure 13. 85C220-80 t_{CO1} vs Temperature (Min.)

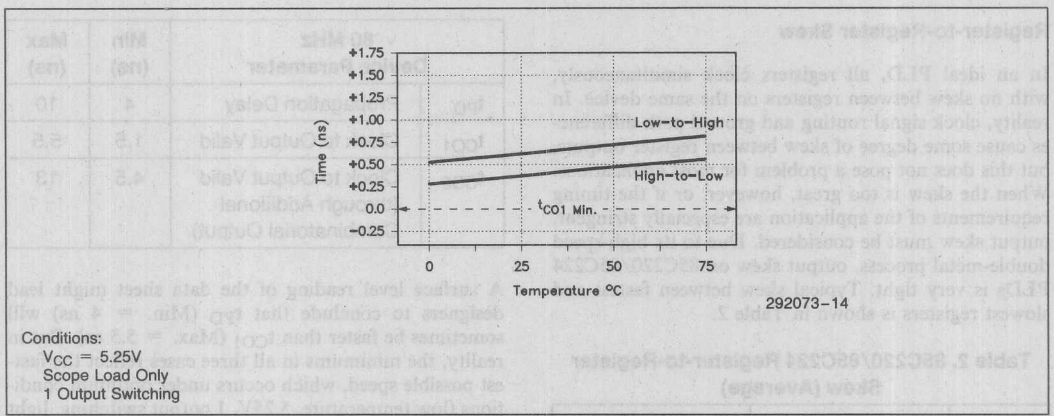

Figure 14. 85C224-80 t_{CO1} vs Temperature (Min.)

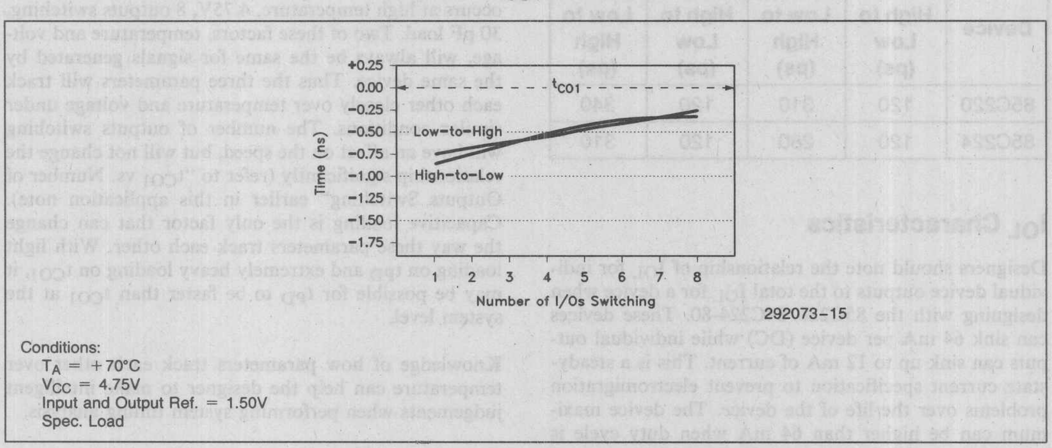

Figure 15. 85C220-80 t_{CO1} vs Number of Outputs Switching

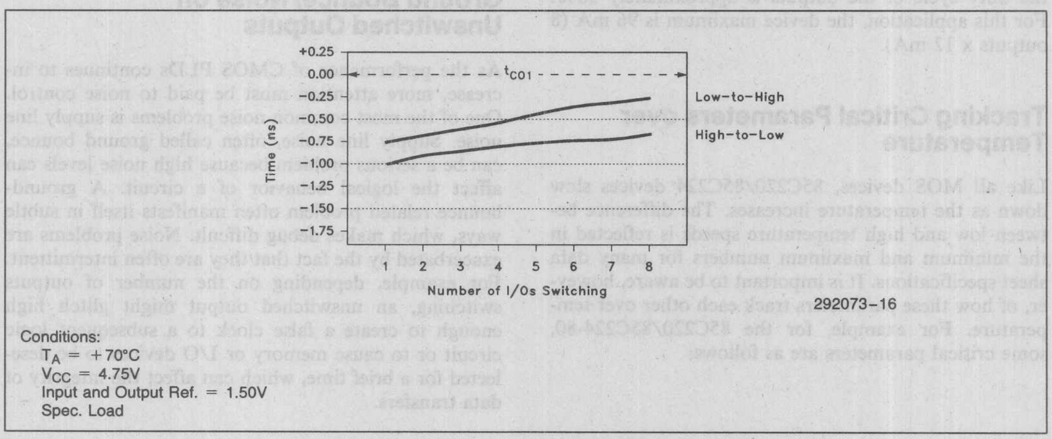

Figure 16. 85C224-80 t_{CO1} vs Number of Outputs Switching

Register-to-Register Skew

In an ideal PLD, all registers clock simultaneously, with no skew between registers on the same device. In reality, clock signal routing and ground path differences cause some degree of skew between register outputs, but this does not pose a problem for most applications. When the skew is too great, however, or if the timing requirements of the application are especially stringent, output skew must be considered. Due to its high-speed double-metal process, output skew on 85C220/85C224 PLDs is very tight. Typical skew between fastest and slowest registers is shown in Table 2.

Table 2. 85C220/85C224 Register-to-Register Skew (Average)

Device	0°C		+70°C	
	High to Low (ps)	Low to High (ps)	High to Low (ps)	Low to High (ps)
85C220	120	310	120	340
85C224	120	280	120	310

I_{OL} Characteristics

Designers should note the relationship of I_{OL} for individual device outputs to the total I_{OL} for a device when designing with the 85C220/84C224-80. These devices can sink 64 mA per device (DC) while individual outputs can sink up to 12 mA of current. This is a steady-state current specification to prevent electromigration problems over the life of the device. The device maximum can be higher than 64 mA when duty cycle is taken into account. For example, in an 8-bit counter the duty cycle of the outputs is approximately 50%. For this application, the device maximum is 96 mA (8 outputs x 12 mA).

Tracking Critical Parameters over Temperature

Like all MOS devices, 85C220/85C224 devices slow down as the temperature increases. The difference between low and high temperature speeds is reflected in the minimum and maximum numbers for many data sheet specifications. It is important to be aware, however, of how these parameters track each other over temperature. For example, for the 85C220/85C224-80, some critical parameters are as follows:

80 MHz Device Parameter		Min (ns)	Max (ns)
t_{PD}	Propagation Delay	4	10
t_{CO1}	Clock to Output Valid	1.5	5.5
t_{CO2}	Clock to Output Valid (through Additional Combinatorial Output)	4.5	13

A surface level reading of the data sheet might lead designers to conclude that t_{PD} (Min. = 4 ns) will sometimes be faster than t_{CO1} (Max. = 5.5 ns). But in reality, the minimums in all three cases reflect the fastest possible speed, which occurs under optimum conditions (low temperature, 5.25V, 1 output switching, light load). The maximums reflect the slowest speed, which occurs at high temperature, 4.75V, 8 outputs switching, 30 pF load. Two of these factors, temperature and voltage, will always be the same for signals generated by the same device. Thus the three parameters will track each other closely over temperature and voltage under similar conditions. The number of outputs switching will have an affect on the speed, but will not change the relationship significantly (refer to "t_{CO1} vs. Number of Outputs Switching" earlier in this application note). Capacitive loading is the only factor that can change the way these parameters track each other. With light loading on t_{PD} and extremely heavy loading on t_{CO1}, it may be possible for t_{PD} to be faster than t_{CO1} at the system level.

Knowledge of how parameters track each other over temperature can help the designer to make intelligent judgements when performing system timing analysis.

Ground Bounce/Noise on Unswitched Outputs

As the performance of CMOS PLDs continues to increase, more attention must be paid to noise control. One of the most common noise problems is supply line noise. Supply line noise, often called ground bounce, can be a serious problem because high noise levels can affect the logical behavior of a circuit. A ground-bounce related problem often manifests itself in subtle ways, which makes debug diffcult. Noise problems are exacerbated by the fact that they are often intermittent. For example, depending on the number of outputs switching, an unswitched output might glitch high enough to create a false clock to a subsequent logic circuit or to cause memory or I/O devices to be deselected for a brief time, which can affect the integrity of data transfers.

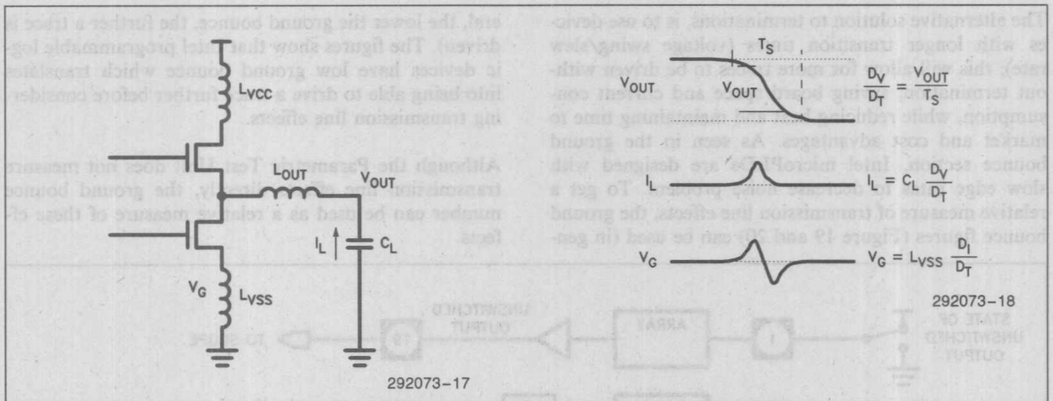

Figure 17. Basic Cause of Ground Bounce

Basic Cause of Ground Bounce

The fundamental cause of ground bounce is switching loaded output pins very quickly. Outputs are normally capacitively loaded, and there is always intrinsic inductance in device bond wires and package lead frames. The resulting structure is a classic LC circuit, as shown in Figure 17. Charging or discharging the circuit creates a damped oscillation. The magnitude, frequency, and duration of the oscillation are determined by the component values that make up the circuit.

V_{OUT} in Figure 17 is normally between 3V and 5V. Switching time (T_S) is in the range of 2 ns–4 ns. Load capacitance (C_L) is in the 30 pF–100 pF range. Inductance depends on the package design and materials, and is typically in the 7 nH–25 nH range. Based on these conditions, it is easy to see that ground bounce (V_G) can be a problem. Ground bounce further increases as more outputs switch simultaneously. In actual practice, the noise levels are less than the simple analysis shown in Figure 17 suggests. This is due to the self limiting nature of the output drivers. As the ground noise causes the local (internal) ground to rise, the drive of the device is reduced, which in turn reduces d_i/d_t.

Figure 18 shows the test setup for measurements. Measurements were made on 85C220-80 devices with 7 outputs switching simultaneously and the remaining output held high or low. The noise generated on the static output by the 7 outputs switching was then measured and recorded (worst case noise condition for a static output). All outputs have 22 pF of capacitance (>30 pF with scope probe), a 220Ω resistor to ground, and 330Ω resistor to V_{CC}. Decoupling is implemented with a 4.7 μF and a multi-layer 0.1 μF (ceramic) capacitor.

For more information on measuring ground bounce, see AP-354, Guide to the PLD Parametric Test Unit.

Figure 19 shows waveforms for the devices with 7 outputs switching. The unswitched outputs are held low. Waveforms are shown for the 85C220-80 (10 ns), 16V8A-10, 16L8-10, and 16L8-7 in Plastic DIP. An 85C220-80 and 16V8A-10 PLCC comparison is shown in Figure 20. Table 3 shows the relative inductance of the different packages.

The values shown represent a lumped load. In an actual system, the distributed load will reduce the values slightly.

Table 3. Package vs. Typical Inductance

Package Type	Typical Inductance
Plastic DIP (with Copper Leadframe)	11 nH
PLCC	6 nH

TRANSMISSION LINE EFFECTS/ NOISE ON SWITCHED OUTPUTS

Although a thorough discussion of transmission line effects is beyond the scope of the application note, a few key points will be discussed. Transmission line effects, like ground bounce, is a slew rate related noise issue. While ground bounce is noise on unswitched outputs, transmission line effects is noise on switched outputs.

In order to minimize transmission line effects, an engineer could use common termination techniques described in many system design guides. Adding terminations does have drawbacks of:

- Increased board space
- Increased cost
- Increased current consumption
- Increased heat

The alternative solution to terminations, is to use devices with longer transition times (voltage swing/slew rate); this will allow for more traces to be driven without termination, saving board space and current consumption, while reducing heat and maintaining time to market and cost advantages. As seen in the ground bounce section, Intel microPLDs are designed with slow edge rates to decrease noise problem. To get a relative measure of transmission line effects, the ground bounce figures (Figure 19 and 20) can be used (in general, the lower the ground bounce, the further a trace is driven). The figures show that Intel programmable logic devices have low ground bounce which translates into being able to drive a trace further before considering transmission line effects.

Although the Parametric Test Unit does not measure transmission line effects directly, the ground bounce number can be used as a relative measure of these effects.

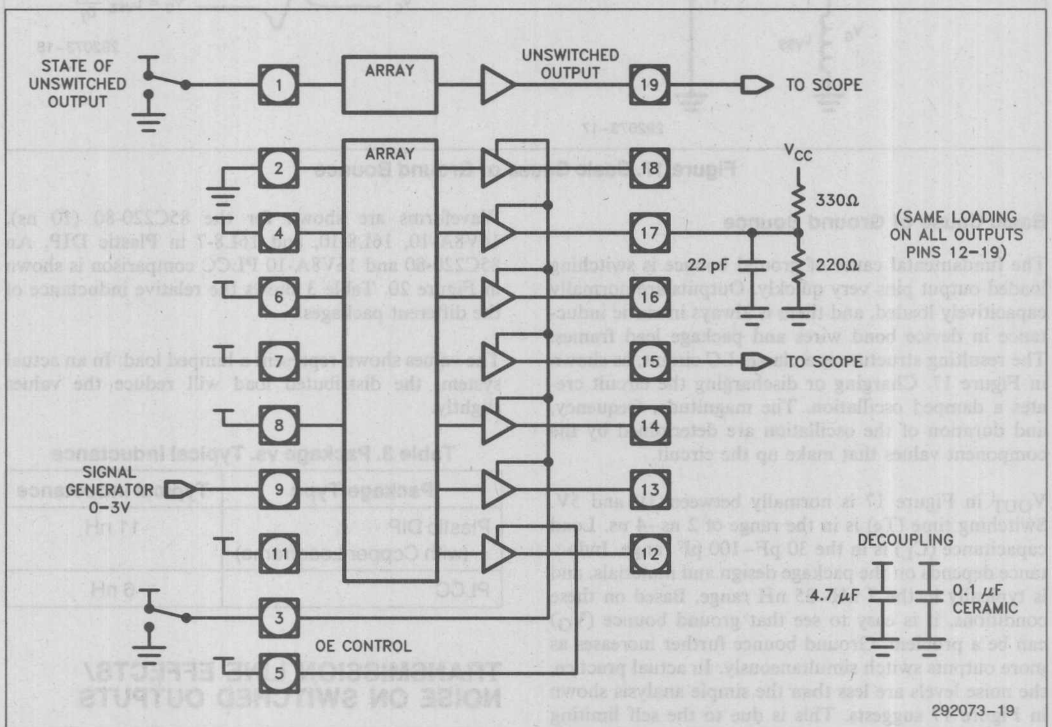

Figure 18. Ground Bounce Test Circuit

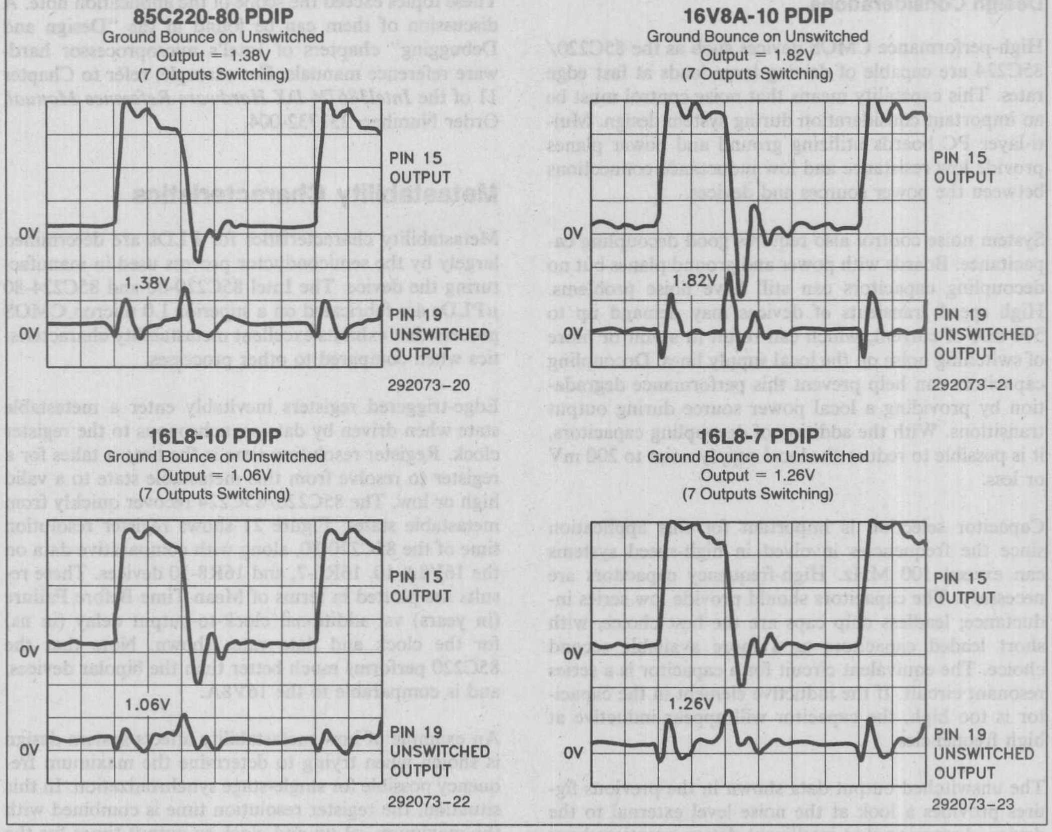

Figure 19. Ground Bounce (PDIP)—7 Outputs Switching

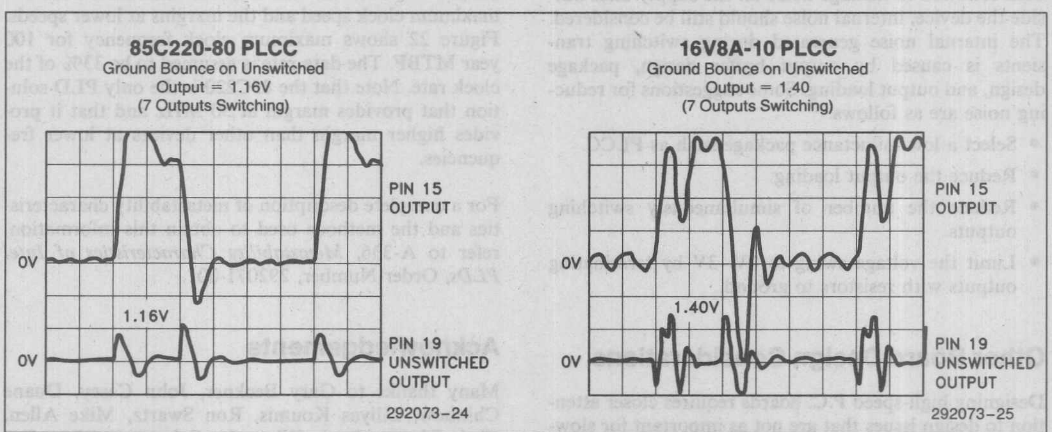

Figure 20. Ground Bounce (PLCC)—7 Outputs Switching

3

Design Considerations

High-performance CMOS devices such as the 85C220/85C224 are capable of driving large loads at fast edge rates. This capability means that noise control must be an important consideration during system design. Multi-layer PC boards utilizing ground and power planes provide low resistance and low inductance connections between the power sources and devices.

System noise control also requires good decoupling capacitance. Boards with power and ground planes but no decoupling capacitors can still have noise problems. High speed transients of devices may demand up to 500 mA of current, which can result in a volt or more of switching noise on the local supply lines. Decoupling capacitors can help prevent this performance degradation by providing a local power source during output transitions. With the addition of decoupling capacitors, it is possible to reduce the local supply noise to 200 mV or less.

Capacitor selection is important for this application since the frequencies involved in high-speed systems can exceed 100 MHz. High-frequency capacitors are necessary. The capacitors should provide low series inductance; leadless chip caps are the best choice, with short leaded capacitors as a more available second choice. The equivalent circuit for a capacitor is a series resonant circuit. If the inductive element in the capacitor is too high, the capacitor will appear inductive at high frequencies.

The unswitched output data shown in the previous figures provides a look at the noise level external to the device. Assuming that intelligent design practices have been followed to manage noise on the supply lines outside the device, internal noise should still be considered. The internal noise generated during switching transients is caused by output buffer design, package design, and output loading. Some suggestions for reducing noise are as follows:

- Select a low-inductance package such as PLCC.
- Reduce the output loading.
- Reduce the number of simultaneously switching outputs.
- Limit the voltage swing to 0V–3V by terminating outputs with resistors to ground.

Other Board Design Considerations

Designing high-speed P.C. boards requires closer attention to design issues that are not as important for slower systems. These elements include:

- Termination of transmission lines
- Clock signal routing
- Power distribution and heat dissipation

These topics exceed the scope of the application note. A discussion of them can be found in the "Design and Debugging" chapters of Intel's microprocessor hardware reference manuals. For example, refer to Chapter 11 of the *Intel386™ DX Hardware Reference Manual,* Order Number: 231732-004.

Metastability Characteristics

Metastability characteristics for PLDs are determined largely by the semiconductor process used in manufacturing the device. The Intel 85C220-80 and 85C224-80 μPLDs are fabricated on a superior 1.0 micron CMOS process that exhibits excellent metastability characteristics when compared to other processes.

Edge-triggered registers inevitably enter a metastable state when driven by data asynchronous to the register clock. Register resolution time is the time it takes for a register to resolve from this metastable state to a valid high or low. The 85C220/85C224 recover quickly from metastable states. Figure 21 shows register resolution time of the 85C220-80, along with comparative data on the 16V8A-10, 16R6-7, and 16R8-10 devices. These results are plotted in terms of Mean Time Before Failure (in years) vs. additional clock-to-output delay (in ns) for the clock and data rates shown. Note that the 85C220 performs much better than the bipolar devices, and is comparable to the 16V8A.

An example of how metastability affects system design is shown when trying to determine the maximum frequency possible for single-stage synchronization. In this situation, the register resolution time is combined with the maximum set-up and clock-to-output times for the device. The total is then used to determine both the maximum clock speed and the margins at lower speeds. Figure 22 shows maximum clock frequency for 100 year MTBF. The data rate is assumed to be 33% of the clock rate. Note that the 85C220 is the only PLD solution that provides margin at 50 MHz and that it provides higher margin than other devices at lower frequencies.

For a complete description of metastability characteristics and the methods used to obtain this information, refer to A-336, *Metastability Characteristics of Intel PLDs*, Order Number, 292071-001.

Acknowledgements

Many thanks to Gary Beckner, John Casey, Duane Chinnow, Liliyas Koumis, Ron Swartz, Mike Allen, Chris Wawro, Darla Wirtz, Joe Salmon and Lisa Endres, for providing technical data and/or direction for this application note.

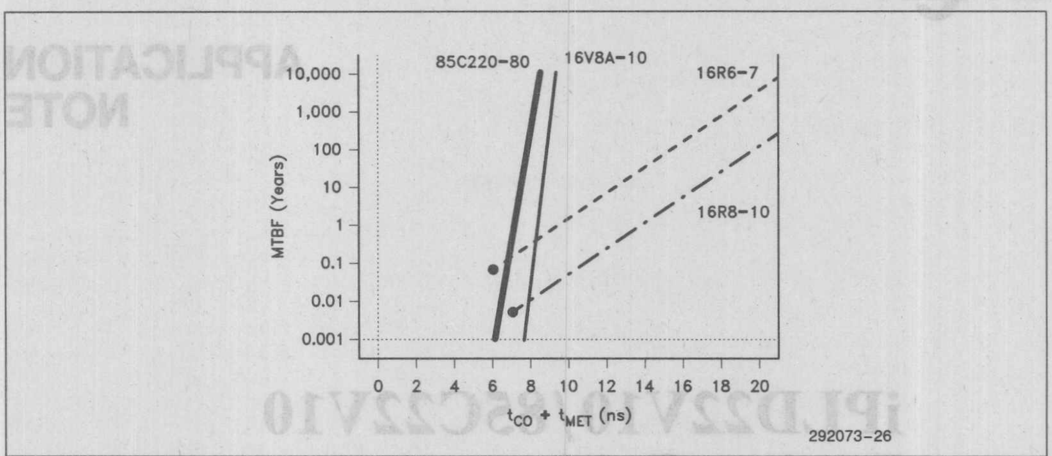

Figure 21. 85C220-80 Clock-to-Output Resolution vs MTBF

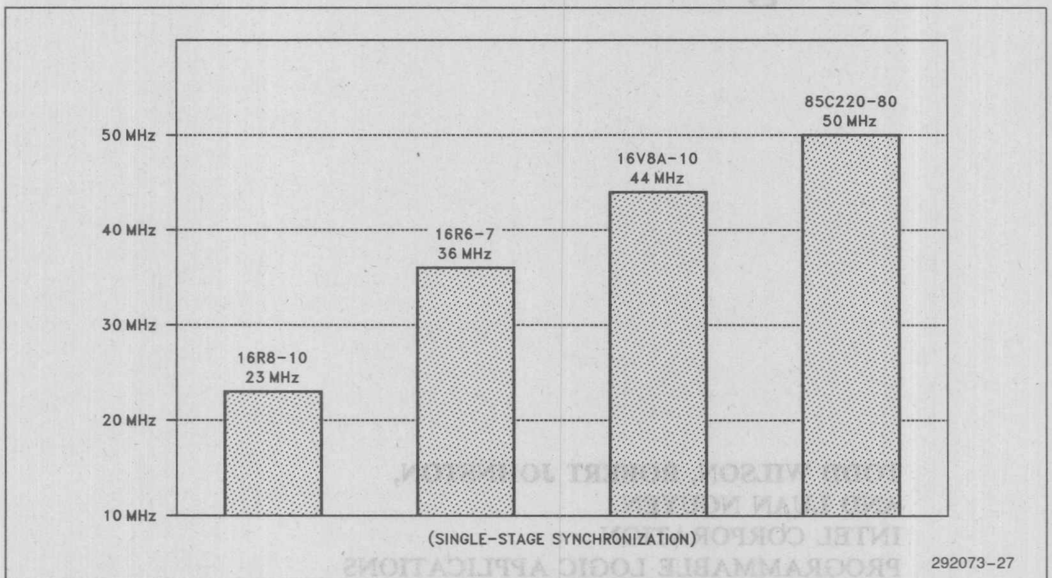

Figure 22. Maximum Frequency for 100 Year MTBF

APPLICATION NOTE

iPLD22V10/85C22V10 Design Guide

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INTEL CORPORATION
PROGRAMMABLE LOGIC APPLICATIONS

September 1993

Order Number: 292106-002

iPLD22V10/85C22V10 Design Guide

CONTENTS

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3

1.0 INTRODUCTION

Background

For years, designers have grown to depend on Programmable Logic Devices (PLDs) for low cost, high performance implementation of random logic and interface circuits. The combination of low cost, high performance, flexibility, and programming/development support make PLDs very attractive to both designers and design managers.

Intel's Programmable Logic Devices (PLDs) meet today's system requirements, as well as map the path to the needs of next generation's products. Intel PLDs provide the high-speed CMOS logic solution required by current and future microprocessors and VLSI peripherals.

The Intel PLD22V10 is a low cost, high-speed, low-power upgrade from PAL and GAL devices. Pin- and JEDEC-compatibility with industry standard 22V10s make the iPLD22V10 a drop-in upgrade requiring NO additional engineering effort.

The 85C22V10 PLD provides all the same features as the iPLD22V10. In addition, the 85C22V10's enhanced macrocell architecture gives the designer a greater range of feedback and clock options without sacrificing pin- and JEDEC-compatibility with industry standard 22V10 parts. The 85C22V10 may be programmed as a standard 22V10 device by using a standard 22V10 JEDEC file. Optional *superset* features are accessed through an extended JEDEC file compiled by popular design tools such as ABEL and CUPL, or through Intel's PLDshell Plus.

Document Overview

This design guide provides technical support for designers, design managers, and others interested in using Intel's PLD22V10 and 85C22V10 PLDs. The information contained in this document is intended to support both the decision making process prior to design and the qualification process that occurs during and after the design is complete. The format of the design guide is as follows:

Section 2-Product Overview: Highlights and architecture of the iPLD22V10 and the 85C22V10 PLDs.

Section 3-Specification Analysis: The key D.C. and A.C. specs (from the data sheet) are discussed and compared against competitive devices. This section provides a baseline for comparison and device selection. Also, some insights are provided on how to best use the data sheet specifications.

Section 4-Advanced Design Issues: This section discusses issues affecting high-speed systems designs. Topics include output slew rates, effects of capacitive loading on outputs, and synchronous/asynchronous register operation.

Section 5-Design Examples: Design ideas using the unique performance and architecture combination of the Intel 85C22V10 are presented.

2.0 OVERVIEW

Product Overview

The 22V10 architecture is one of several industry standard PLD architectures. While bipolar implementations of this architecture have worked well in the past, the speed and power consumption requirements of today's applications are beyond the limitations of bipolar devices. Intel's iPLD22V10 and 85C22V10 PLDs, based on CHMOS IIIE technology, meet the power and speed requirements of today's high-speed systems while maintaining pin- and JEDEC-compatibility with standard 22V10 devices.

Related Document Listing	
Document	**Order Number**
iPLD22V10-7 Data Sheet	290485
iPLD22V10 Data Sheet	290487
85C22V10 Data Sheet	290416
Metastability Characteristics of Intel EPLD's	292071
PLD Quality and Reliability Data Summary	293003

Features

The iPLD22V10 and 85C22V10 are high-performance, high-integration, general-purpose CMOS PLDs. The features provided by these devices include:

- High Speed Operation (t_{PD} = 10 ns, t_{CO1} = 7 ns, 95.2 MHz State Machine Frequency, 100 MHz with No Feedback)
- Typical I_{CC} = 90 mA @ 15 MHz
- 10 Programmable Macrocells (I/O Pins)
- EPROM Cell, CMOS Technology
- 100% Silicon Testability
- 24-pin DIP, 28-pin PLCC Packages
- Programmable Security Bit
- *Superset* Clock and Feedback Features (85C22V10)

PACKAGING

Figure 1 shows the pinouts of the DIP and PLCC packages for the iPLD22V10 and 85C22V10 PLDs. Both the iPLD22V10 and the 85C22V10 are available in a plastic One-Time-Programmable (OTP) DIP package and in a plastic OTP PLCC package. In addition, the 85C22V10 is available in a UV erasable/reprogrammable Ceramic DIP package.

PROCESS

The high performance of the iPLD22V10 and 85C22V10 is a result of combining an industry-standard architecture with Intel's advanced 1-micron CHMOS IIIE EPROM technology. This technology brings high speed and significant power savings to a well known architecture.

TESTABILITY

The CHMOS IIIE EPROM technology used in the iPLD22V10 and 85C22V10 allows complete testability of every part Intel produces. At the wafer level, all device programmable elements are programmed and tested, and all data paths are 100% tested. The device is then completely erased. Once the device is packaged, special manufacturing test modes are utilized to ensure post packaging device functionality and performance. Intel's rigorous test procedures ensure high yields for our customers, and high reliability for their customers.

Architecture

GLOBAL ARCHITECTURE

Figure 2 shows the global architecture for both devices. The iPLD22V10 and 85C22V10 feature 12 dedicated input pins (including CLK/INP0) and 10 I/O pins. Each of the I/O pins is associated with a macrocell. All inputs and feedback signals and their compliments are available to all product (AND) terms. The product terms are summed by a single OR-gate, thus forming an AND-OR logic array. The sum-of-products (SOP) is fed into the macrocell. Each macrocell is fed by a maximum of from 8 to 16 product terms, depending on the position of the particular macrocell.

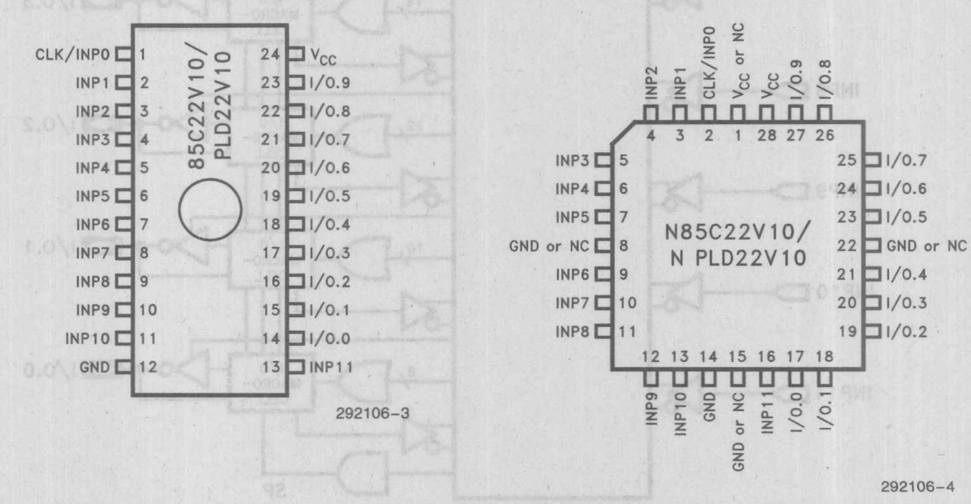


Figure 1. Pinout Diagrams for iPLD22V10 and 85C22V10

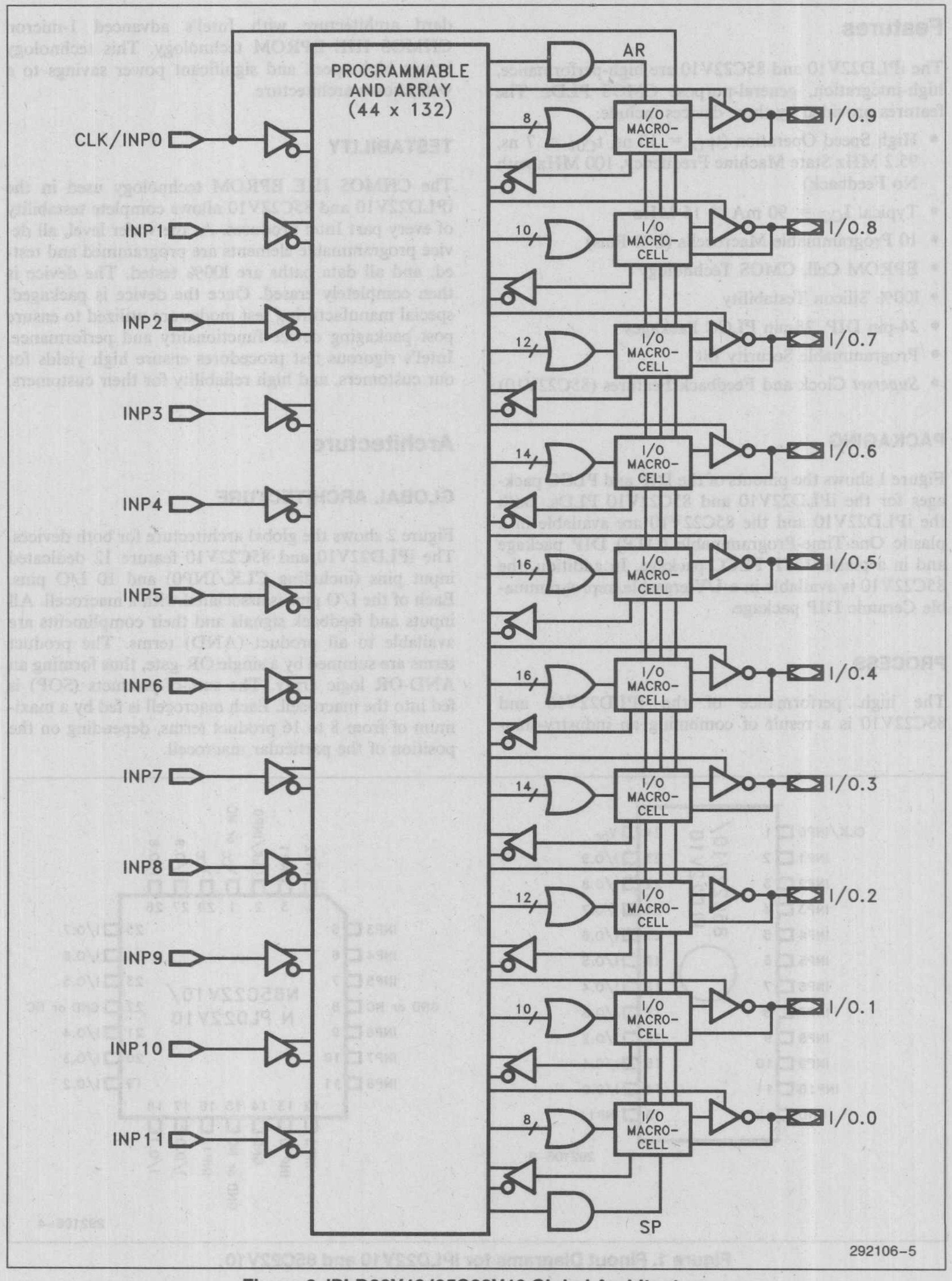


Figure 2. iPLD22V10/85C22V10 Global Architecture

GLOBAL PRESET AND RESET

The iPLD22V10 and 85C22V10 registers may be synchronously set and asynchronously reset on a global basis. The synchronous preset signal (SP) is determined for all macrocells by a single global p-term that is separate from macrocell sum-of-products (SOP). After SP is asserted, the next clock transition that triggers the macrocell registers will cause the Q outputs to be set to logic HI. Note that if post-register inversion is programmed (active-low output), the macrocell's pin will be set to a logic LOW.

The asynchronous reset signal (AR) is also derived from a single independent global p-term. Macrocell registers are reset by AR asynchronously with respect to the device clock. If post-register inversion is programmed (active-low output), the macrocell's pin will be reset to a logic HI. For details on timing parameters that relate to preset and reset, please refer to A.C. Specifications.

Macrocell Architecture

iPLD22V10

Figure 3 shows the macrocell architecture for the iPLD22V10. The architecture allows registered or combinatorial logic with active-high or active-low output. Note that in the iPLD22V10, the output type determines the feedback type (if any feedback is used): registered output dictates registered feedback, and combinatorial output dictates pin feedback. Also, because outputs may be programmed as either active-high or active-low on a macrocell-by-macrocell basis, the polarity or "sense" of the output pin associated with a macrocell register is independent of the register itself. Table 1 lists the output configurations for the iPLD22V10.

Table 1. iPLD22V10 Macrocell Configurations

S1	S0	Output/Polarity	Feedback
0	0	Registered/Active Low	Registered
0	1	Registered/Active High	Registered
1	0	Combinatorial/Active Low	Pin
1	1	Combinatorial/Active High	Pin

The Clock (CLK) input for macrocell registers comes from PIN 1. If a CLK signal is not needed, i.e. if all outputs are combinatorial, PIN 1 may be used as another generic input to the logic array. Output Enable (OE) for each macrocell is controlled by a single p-term in the logic array. This p-term is not taken from the product terms that feed the macrocell (as is the case in traditional PAL devices), so there is no penalty for using the OE p-term. OE for each macrocell is independent and asynchronous.

85C22V10

The 85C22V10 macrocell architecture is shown in Figure 4. This is an enhanced version of the iPLD22V10 macrocell. Note the additions to the clock and feedback selection sections. The addition of the XOR gate at the clock input to the macrocell flip-flop allows the clock to be *inverted*. When this feature is programmed, the macrocell flip-flop will latch at the falling edge of the CLK input, rather than the rising edge. This gives the system designer greater flexibility to determine clock timing for each macrocell.

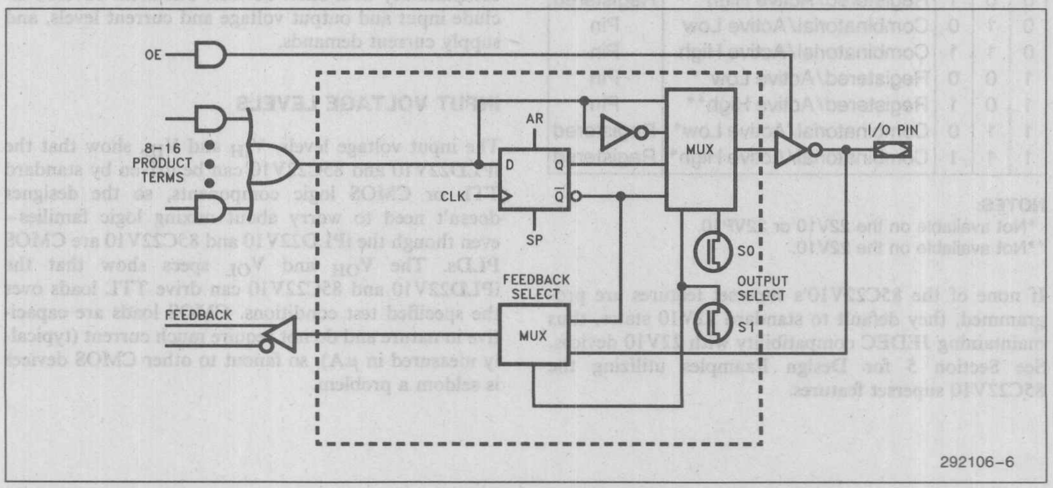


Figure 3. iPLD22V10 Macrocell Architecture

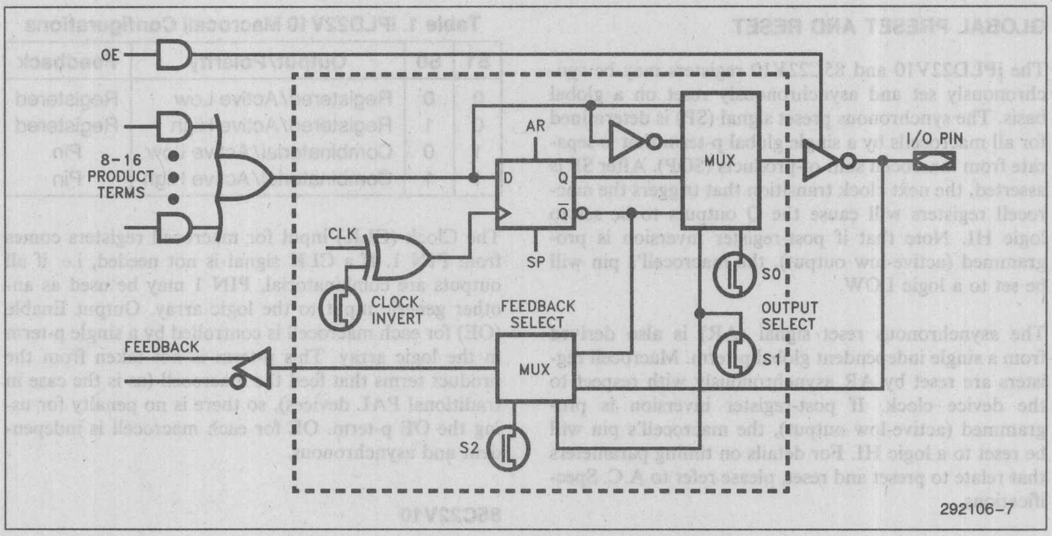


Figure 4. 85C22V10 Macrocell Architecture

The other addition to this macrocell is the S2 switch in the feedback selection. The effect of S2 is clearly seen in Table 2. All combinations of output and feedback can now be supported. This opens up the possibility of using the macrocell pins as true I/O ports. For instance, a bi-directional register can now be implemented on a single 85C22V10. The 85C22V10 also allows a combinatorial signal to drive a macrocell pin while a registered version of that signal is fed back into the device. See Design Example 2.

Table 2. 85C22V10 Macrocell Configurations

S2	S1	S0	Output/Polarity	Feedback
0	0	0	Registered/Active Low	Registered
0	0	1	Registered/Active High	Registered
0	1	0	Combinatorial/Active Low	Pin
0	1	1	Combinatorial/Active High	Pin
1	0	0	Registered/Active Low**	Pin
1	0	1	Registered/Active High**	Pin
1	1	0	Combinatorial/Active Low*	Registered
1	1	1	Combinatorial/Active High*	Registered

NOTES:
*Not available on the 22V10 or 22VP10.
**Not available on the 22V10.

If none of the 85C22V10's superset features are programmed, they default to standard 22V10 states, thus maintaining JEDEC compatibility with 22V10 devices. See Section 5 for Design Examples utilizing the 85C22V10 superset features.

3.0 SPECIFICATION ANALYSIS

This section is intended to expand on some of the data sheet details. Those qualities that the specifications characterize are interpreted.

Typical data taken from in-circuit applications is presented in Section 4, Advanced Design Issues.

D.C. Characteristics

D.C. characteristics describe the steady-state behavior of a device. These specs provide insight into the iPLD22V10/85C22V10's power consumption and compatibility with other devices. The areas covered include input and output voltage and current levels, and supply current demands.

INPUT VOLTAGE LEVELS

The input voltage levels, V_{IH} and V_{IL}, show that the iPLD22V10 and 85C22V10 can be driven by standard TTL or CMOS logic components, so the designer doesn't need to worry about mixing logic families—even though the iPLD22V10 and 85C22V10 are CMOS PLDs. The V_{OH} and V_{OL} specs show that the iPLD22V10 and 85C22V10 can drive TTL loads over the specified test conditions. CMOS loads are capacitive in nature and do not require much current (typically measured in μA), so fanout to other CMOS devices is seldom a problem.

OUTPUT SPECIFICATIONS: I_O AND V_O

The best measure of a device's ability to handle loads is I_{OL}. Most devices can "sink" more current than they can "source", so I_{OL} is usually quoted in connection with load driving ability. The data sheet test condition for V_{OL} shows that the iPLD22V10 and 85C22V10 are guaranteed to handle 16 mA loads while maintaining the output voltage at or below 0.45V.

I_{OH} is generally specified at minimum voltage-high output, V_{OH}. The iPLD22V10 and 85C22V10 outputs are guaranteed to supply −4 mA at a minimum of 2.4V. This is information applicable for driving TTL loads, but CMOS devices will consume less current internally if their inputs are driven closer to V_{CC}. For this reason, Intel PLD22V10 and 85C22V10 PLDs have a built-in pullup circuit to drive their outputs to near V_{CC}, and are specified to provide a minimum of −100 μA for $V_O = V_{CC} - 0.3V$. Refer to Figure 14 for typical I_O vs V_O data.

I_{CC} SPECIFICATIONS

The D.C. specification of greatest interest to most designers is I_{CC}. This value not only specifies how much current the device will require, but also indicates how much heat (watts) the device will dissipate. For this reason, the I_{CC} specification will affect both the power supply requirements and the board reliability. I_{CC} is measured with the device unloaded, so the value indicates how much current the device itself requires.

I_{CC} is specified at 15 MHz, but because CMOS devices consume most of their power during transitions, I_{CC} varies with the frequency of the clock and other inputs. For more precise current/power calculations see Figure 5: Typical I_{CC} vs Frequency for a 10-bit counter.

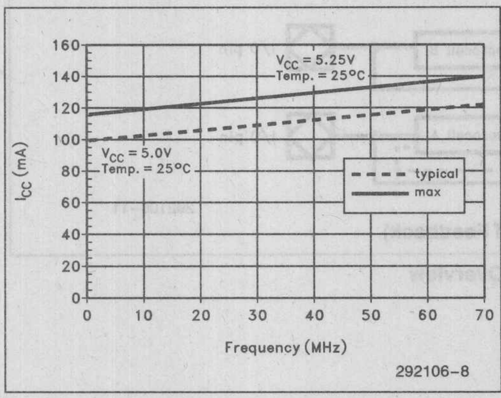


Figure 5. iPLD22V10/85C22V10-10 I_{CC} vs Frequency

A.C. Characteristics

The A.C specifications describe the guaranteed switching frequencies and timing properties of the device. In this section, the meanings of data sheet quantities are clarified, and comparisons are made with competitive parts.

COMBINATORIAL PARAMETERS

Timing for combinatorial functions is determined by the total pin-to-pin propagation delay and the output enable/disable times t_{PD}, t_{PZX} and t_{PXZ}. t_{PD} is the delay between the time that valid data is present on an input pin, and the time that the effect of that input data is seen at an output pin. t_{PD} is measured with output enable asserted; it does not include t_{PZX} or t_{PXZ}. Figure 6 shows t_{PD}, t_{PZX} and t_{PXZ} in the form of a timing diagram.

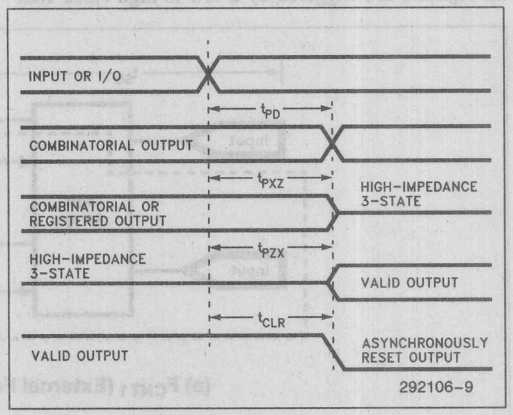


Figure 6. Combinatorial Timing Parameters

SYNCHRONOUS PARAMETERS

Registered output requires that valid data be present at the register's data input before the register is clocked. The user of a device ensures that this condition is met by adhering to the setup time, t_{SU}. The setup time determines how long before the clock edge arrives at the CLK pin that valid data must already be at the input pin(s).

The time between the arrival of the clock edge at the CLK pin and valid data being present at the *output pin* is t_{CO1}. The minimum time needed to affect a valid registered output is then $t_{SU} + t_{CO1}$. If the device is configured as a counter using external feedback from a macrocell output pin to an input pin, the maximum frequency with which it can be clocked is $F_{CNT1} = 1/(t_{SU} + t_{CO1})$.

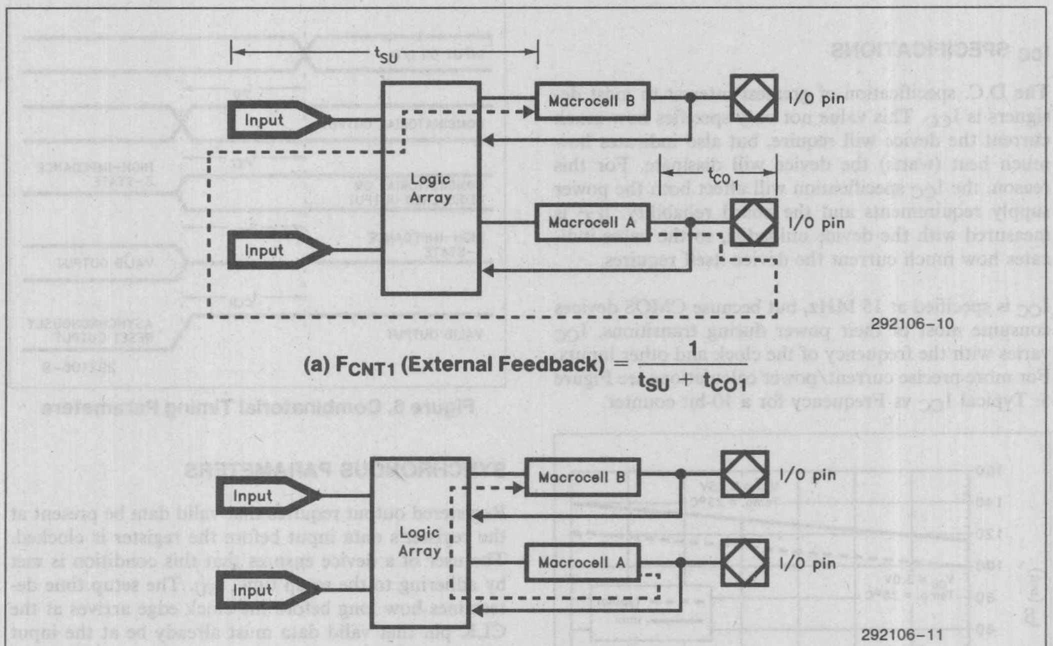
If internal feedback is used, then input and output buffers are no longer in the data path. Propagation time is decreased, and the maximum counter frequency is increased to F_{CNT2}. Figure 7 provides an overview of both F_{CNT} values.

The device may be used to output a registered sum of products without feedback. In this case, the maximum clock frequency is limited by the minimum clock period: $f_{MAX} = 1/t_{CP}$.

PRESET AND RESET SPECIFICATIONS

The **Synchronous Preset (SP)** signal is derived from a single independent p-term. To insure predictable preset results, the designer will make sure that SP will meet the Synchronous Preset to CLK ↑ Setup Time, t_{SP}, before a clock edge is applied to the CLK pin to trigger a global register preset. In the case of the iPLD22V10, all registers are triggered by a low-to-high clock transition, and t_{SP} is measured from that transition. However, in the case of the 85C22V10, the sense of the CLK signal can be selected for each macrocell on an individual basis. The astute designer will see that this raises the possibility of synchronously presetting a subset of the registers on the device.

For example, consider two state machines implemented on the same 85C22V10. The first state machine's registers are programmed to respond to a low-to-high clock transition at the CLK pin, while the second state machine's registers are programmed to respond to the inverted high-to-low clock transition. If SP is asserted t_{SP} before a low-to-high clock transition, then the first state machine will be preset. But if SP is unasserted t_{SU} before the high-to-low clock transition, the second state machine will NOT be preset. In a similar fashion, the second state machine may be preset without affecting the first. A timing diagram of this *superset* capability is presented in Figure 8.



(a) F_{CNT1} (External Feedback) $= \dfrac{1}{t_{SU} + t_{CO1}}$

(b) F_{CNT2} (Internal Feedback)

Figure 7. F_{CNT} Overview

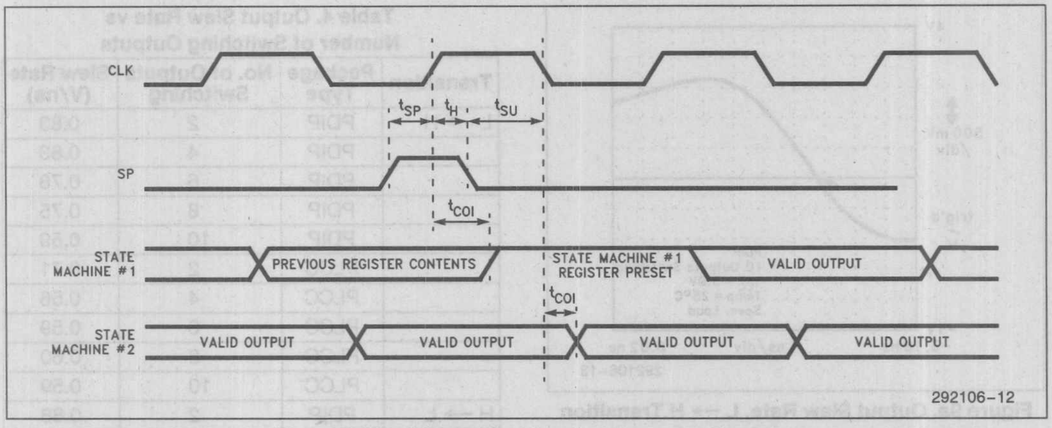


Figure 8. Dual State Machine Synchronous Preset

The **Asynchronous Reset (AR)** signal is also determined by a single global p-term. However, because this is an asynchronous signal, no setup time with respect to CLK ↑ is required. The time that elapses between the assertion of the reset condition and the time that the actual reset occurs at the output pin is t_{CLR}.

Asynchronous Reset Recovery time, t_{ARR}, is the *maximum* amount of time required for macrocell registers to begin correctly responding to CLK after AR is removed. No minimum recovery time is specified. To insure predictable results, AR should be removed (unasserted) at least t_{ARR} before the next active clock edge appears at the CLK input. Other approaches here might be to disable outputs or hold inputs constant until t_{ARR} after AR is removed. Since t_{ARR} is a setup time with respect to CLK, it is given as a synchronous specification. On the other hand, t_{CLR} does not depend on CLK, so it is included in the combinatorial specifications.

4.0 ADVANCED DESIGN ISSUES

As end users demand higher speeds and time to market becomes more critical, designers require more detailed information than is typically available in the data sheet. The purpose of this section is to provide designers with data that characterizes the effects of loading, temperature, and internal resource utilization on device performance. This data is intended to help support engineering decisions in all phases of product development, from design to production.

Data were measured with the output load specified in the 85C22V10 data sheet unless otherwise specified. The topics covered in this section are:

- Output Slew Rates
- t_{PD} Characteristics for Combinational Logic
- Output Skew Characteristics for Synchronous Register Operation
- Asynchronous Register Operation Characteristics
- Output Current Characteristics
- Design Considerations

Output Slew Rate (Edge Rate)

The output buffers in the iPLD22V10 and 85C22V10 are designed to reduce transmission line effects through controlling output slew rates. Rapid voltages changes contain high-frequency components that can produce unwanted transmission line effects on circuit board traces. Possible effects include ringing, dispersion, and radiation losses. Overcoming these effects can be time consuming and expensive. The iPLD22V10 and 85C22V10 output buffer design limits transmission line effects through providing low output slew rates. These low slew rates contain fewer of the high-frequency signal components that give board designers headaches.

Figure 9 provides sample iPLD22V10/85C22V10 output waveforms expanded to highlight slew rate. Tables 3 and 4 show that the slew rate is very consistent with respect to both temperature and number of outputs switching, though the slew rate does decrease slightly as temperature or the number of switching outputs increases.

The consistent, slow edge rates provided by the Intel PLD22V10 and 85C22V10 allow the designer to use the full capabilities of these devices without having to worry about transmission line effects.

3

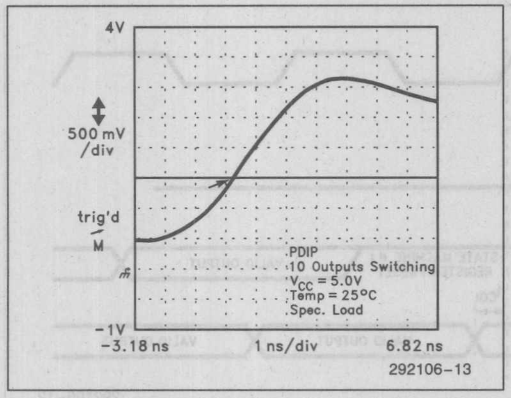


Figure 9a. Output Slew Rate, L → H Transition (PDIP, 10 Outputs Switching, V_{CC} = 5V, Temp = 25°C, Spec. Load)

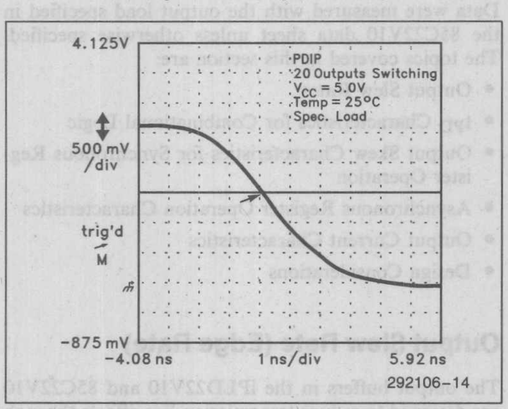


Figure 9b. Output Slew Rate, H → L Transition (PDIP, 10 Outputs Switching, V_{CC} = 5V, Temp = 25°C, Spec. Load)

Table 3. Output Slew Rate vs Temperature

Transition	Package Type	Temperature (°C)	Slew Rate (V/ns)
L → H	PDIP	0	0.72
	PDIP	25	0.72
	PDIP	70	0.70
	PLCC	0	0.56
	PLCC	25	0.59
	PLCC	70	0.53
H → L	PDIP	0	0.67
	PDIP	25	0.67
	PDIP	70	0.62
	PLCC	0	0.87
	PLCC	25	0.80
	PLCC	70	0.77

TEST CONDITIONS:
V_{CC} = 5V, 10 Outputs Switching, Spec. Load.

Table 4. Output Slew Rate vs Number of Switching Outputs

Transition	Package Type	No. of Outputs Switching	Slew Rate (V/ns)
L → H	PDIP	2	0.83
	PDIP	4	0.83
	PDIP	6	0.78
	PDIP	8	0.75
	PDIP	10	0.59
	PLCC	2	0.71
	PLCC	4	0.56
	PLCC	6	0.59
	PLCC	8	0.60
	PLCC	10	0.59
H → L	PDIP	2	0.88
	PDIP	4	0.78
	PDIP	6	0.75
	PDIP	8	0.70
	PDIP	10	0.67
	PLCC	2	1.17
	PLCC	4	1.0
	PLCC	6	1.0
	PLCC	8	1.0
	PLCC	10	0.80

TEST CONDITIONS:
V_{CC} = 5V, Temp = 25°C, Spec. Load.

Ground Bounce

The rapid current changes that occur inside all high-speed logic devices during normal state transitions cause short-term voltage changes, or "glitches", on pins that are not changing state. This phenomenon is called *ground bounce.* Ground bounce is typically seen during the rising or falling edges of a state change, where internal currents must change most rapidly.

Table 5 shows typical ground bounce levels for the Intel iPLD22V10 and 85C22V10 PLDs compared to several competing parts. Data presented in Table 5 was taken using the load specified in "EDN's advanced CMOS logic ground-bounce tests", EDN, March 2, 1989.

The low ground bounce levels of the Intel PLDs guard against glitch problems in high-performance systems, and free high-performance designers from a major headache.

The Intel iPLD22V10 and 85C22V10 PLDs in the plastic PLCC package provide the option of additional ground and V_{CC} connections. Table 6 shows the effect of using these additional connections. While the use of these pins is not required for normal specified operation, connecting these pins produces a positive effect on ground bounce and glitch immunity.

Table 5. Ground Bounce vs Competition

	Intel 85C22V10	AMD PALCE22V10	Lattice GAL22V10	Cypress PAL22V10	ICT PEEL22V10
Package	PDIP	PDIP	PDIP	PDIP	PDIP
Pk to Pk	1.40V	1.48V	1.84V	1.40V	1.56V
Peak	0.800V	0.92V	1.04V	0.76V	0.92V

TEST CONDITIONS:
V_{CC} = 5V, Temperature = 25°C, EDN Load.

Table 6. Ground Bounce with Additional V_{CC} and GND Pins

	Intel 85C22V10	Intel 85C22V10
Package Connections	PLCC Pins 1, 8, 15, 22 Open (NC)	PLCC Pins 1, 8, 15, 22 Connected
Pk to Pk	1.48V	1.32V
Peak	0.88V	0.68V

TEST CONDITIONS:
V_{CC} = 5V, Temperature = 25°C, Spec Load.

Propagation Delay: t_{PD}

The maximum propagation delay (t_{PD}) specified in the data sheet for -10 devices is 10 ns. This is guaranteed for worst-case voltage and temperature while driving the spec load. Factors that effect typical t_{PD} include the number p-terms in the data path, the number of outputs switching simultaneously, and load capacitance.

Figure 10 shows typical t_{PD} vs p-terms characteristics. As the number of p-terms increases, internal device loading causes the propagation delay to increase or decrease slightly.

Figure 11 shows the relation of t_{PD} to number of outputs switching. As the-number of outputs simultaneously switching increases, t_{PD} also increases. This effect is related to the ability of the package power and ground leads to channel additional current to the device.

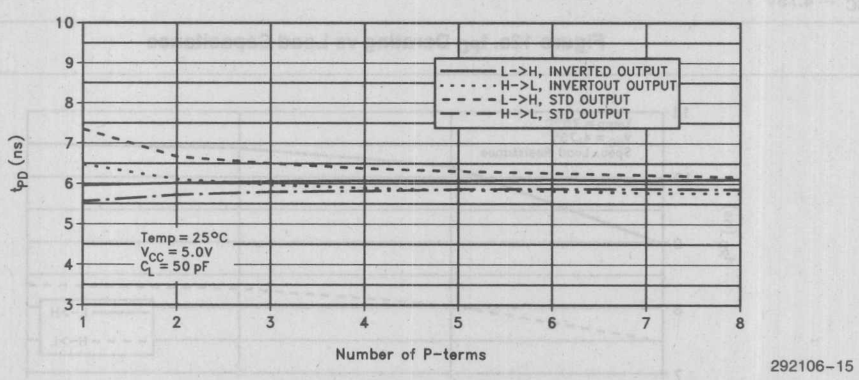


Figure 10. t_{PD} vs Number of P-Terms

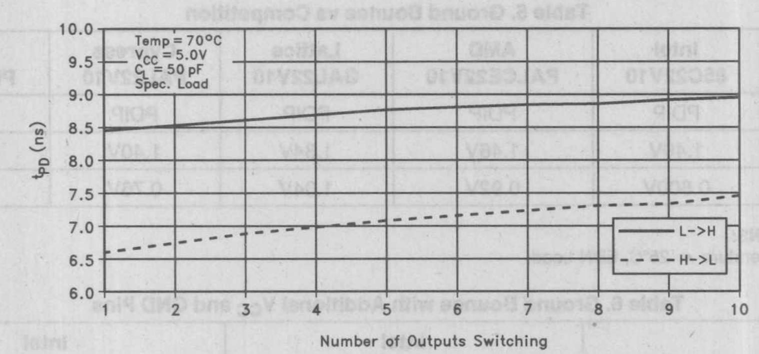
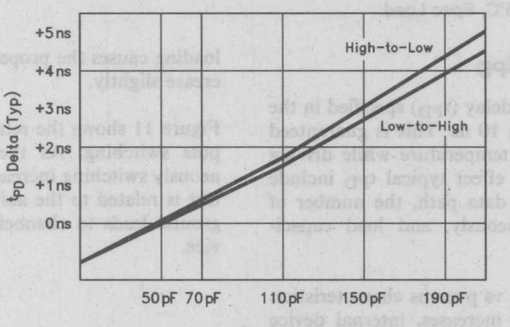


Figure 11. t_{PD} vs Number of Switching Outputs

Figure 12a is the data sheet derating curve for t_{PD} as a function of load capacitance. A large load capacitance will require a long time to charge up to an acceptable voltage level, and thus increase t_{PD}. Typical values for t_{PD} taken over a range of load capacitances are shown in Figure 12b. The typical value for t_{PD} at 160 pF load capacitance is approximately 10.5 ns. Since t_{PD} is specified to be 10 ns max with a load capacitance of 50 pF, this represents a derating of 0.5 ns. This is well within the 3.5 ns maximum derating specified in Figure 12a.



CONDITIONS:
T_A = 70°C
V_{CC} = 4.75V

Figure 12a. t_{PD} Derating vs Load Capacitance

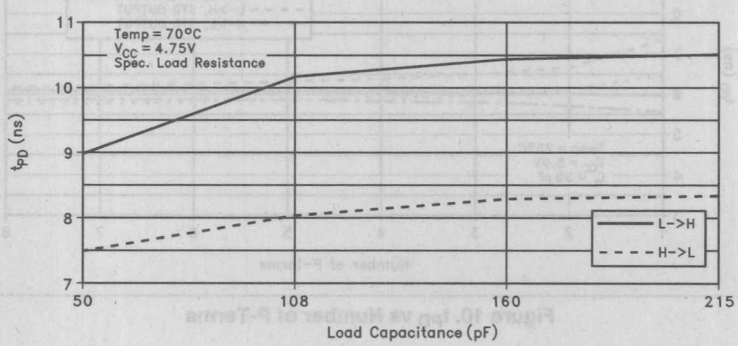


Figure 12b. Typical t_{PD} vs Load Capacitance

CLK to Valid Output: t_{CO1}

The time that elapses between the appearance of an active clock transition at the CLK pin and the effect of that transition on data at an output pin is t_{CO1}. Intel PLDs are compensated to reduce the effect of temperature on performance. A t_{CO1} Derating vs Temperature curve is included in the datasheet.

t_{CO1} skew is the difference in timing of one output pin with respect to another. This phenomenon is a result of different internal path lengths from the CLK pin to the various macrocells. Note that only minimum and maximum values are specified for t_{CO1}. No values for skew are quoted in the datasheet. Figure 13 shows typical t_{CO1} skew measurements for different temperatures. The greatest measured skew was well under 1 ns for L → H transitions. The largest measured variation with respect to temperature was under 0.6 ns in the case of H → L transitions.

A look at the 85C22V10 datasheet shows that the specified t_{CO1} ranges are identical for standard CLK and optional inverted CLK. The architecture of the 85C22V10 macrocell reveals that the CLK signal passes through the XOR clock inversion gate whether or not clock inversion is used. Thus, programming the inverted clock *superset* feature introduces no speed penalty.

I/O Drive

The ability of a device to drive a load is directly reflected by I_O. Obviously, output current depends on the nature of the load, so only the short-circuit current, I_{SC}, appears in the data sheet. Figure 14 gives greater insight into the output current capabilities of the iPLD22V10 and 85C22V10. This graph shows output current as a function of load voltage for both output-high and output-low conditions. Notice that in this graph, the polarity of the current is ignored. For the output-low condition (I_{OL}), positive conventional current is flowing into the device: the device is sinking current. For output-high condition (I_{OH}), current is flowing out of the device: the device is sourcing current.

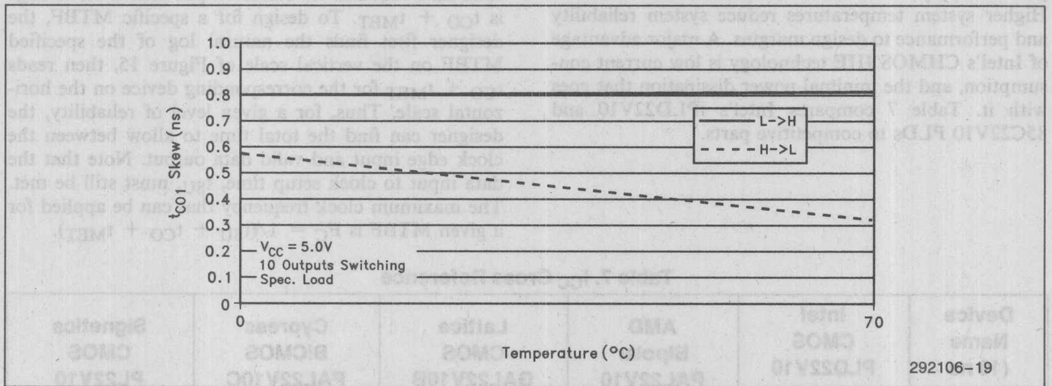


Figure 13. Typical t_{CO1} Skew vs Temperature

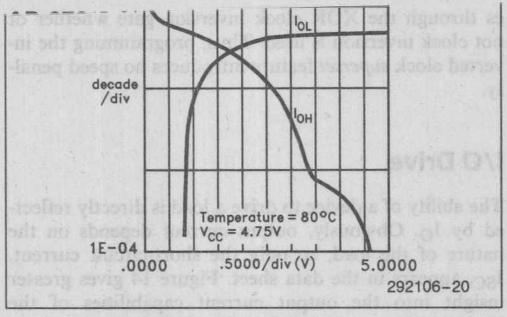


Figure 14. I_O vs V_O

Current Consumption: I_{CC}

The best indication of a device's power consumption is I_{CC}. One of the limitations of older bipolar devices is their high current consumption that requires a large power supply and overheats system circuit boards. Higher system temperatures reduce system reliability and performance to design margins. A major advantage of Intel's CHMOS IIIE technology is low current consumption, and the minimal power dissipation that goes with it. Table 7 compares Intel's iPLD22V10 and 85C22V10 PLDs to competitive parts.

"Metastable" may be defined as the condition of a bistable system before it has entered one of its stable states. Metastability may be perceived as oscillation or "hovering" between stable states for a short period of time before the system resolves into a stable state. Metastability may be introduced into a logic system by violating timing or voltage parameters laid out in data sheets, but it may also appear as a result of random noise, ambient conditions, or other conditions beyond the control of the system designer. For this reason, metastability is usually predicted on a statistical basis and measured as Mean Time Between Failures (MTBF) for a given variable.

Figure 15 shows typical MTBF as a function of $t_{CO} + t_{MET}$ for the iPLD22V10/85C22V10-10 and for the PAL 22V10-10. These parts were programmed as 10-bit counters. Data for the 74F74 D flip-flop is also presented for comparison. t_{CO} is taken from the data sheet. t_{MET} is the amount of time after t_{CO} that is required for the device to produce a stable output. The total time required for stable output after a clock edge is $t_{CO} + t_{MET}$. To design for a specific MTBF, the designer first finds the natural log of the specified MTBF on the vertical scale of Figure 15, then reads $t_{CO} + t_{MET}$ for the corresponding device on the horizontal scale. Thus, for a given level of reliability, the designer can find the total time to allow between the clock edge input and valid data output. Note that the data input to clock setup time, t_{SU}, must still be met. The maximum clock frequency that can be applied for a given MTBF is $F_C = 1/(t_{SU} + t_{CO} + t_{MET})$.

Table 7. I_{CC} Cross Reference

Device Name (10 ns Parts)	Intel CMOS PLD22V10 85C22V10	AMD Bipolar PAL22V10	Lattice CMOS GAL22V10B	Cypress BiCMOS PAL22V10C	Signetics CMOS PL22V10
I_{CC} @ 15 MHz	130 mA	180 mA	130 mA	190 mA	120 mA + 0.5 mA/MHz

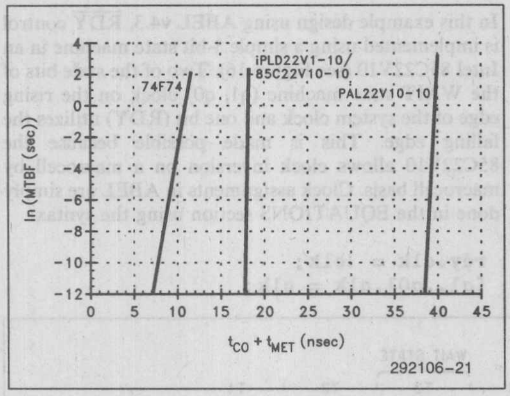


Figure 15. Tau Curves for Intel PLD22V10/85C22V10-10 vs Competition

The Intel PLD22V10 and 85C22V10 are protected from metastability through careful register design and the use of high-gain output amplifiers driven by the macrocell. This provides immunity from metastability by ensuring that the output will be driven to one extreme state or the other: either logic HI or LOW. For more information on metastability, please refer to the Intel Application Note "Metastability Characteristics of Intel EPLDs", order number 292071-002.

5.0 DESIGN EXAMPLES

Design Example # 1—Split Phase State Machine

INTRODUCTION

It is sometimes desirable in synchronous system design to have events occur on both the rising and falling edge of the system clock. This allows events to be processed with greater timing granularity.

This example is intended to illustrate one possible use of the programmable clock invert feature of the Intel 85C22V10. In doing this, it is also shown how to access this feature using Data I/O's ABEL design tool.

```
module WAIT
title 'wait state controller'
wait device 'p22vl0ic';     "Intel 85C22V10 in PLCC package
clk, cs0, csl, cs2, cs3 pin 2, 3, 4, 5, 6;    "Inputs
rdy , q0, ql pin 23, 24, 25;                  "Outputs
"WAIT statemachine bits defined
start = ^h0; wait2 = ^h4; halfl = ^h2;
idle = ^h7; waitl = ^h6;
wait3 = ^h5; ready = ^h3;
state_diagram [rdy, ql, q0]
state start: goto idle;
state idle: if ( !cs0 & csl & cs2 & cs3) then ready
            else if ( cs0 & !csl & cs2 & cs3 ) then waitl
            else if ( cs0 & csl & !cs2 & cs3 ) then wait2
            else if ( cs0 & csl & cs2 & !cs3 ) then wait3
            else idle;
state wait3: goto wait2;        "insert 3 waitstates
state wait2: goto waitl;        "insert 2 waitstates
state waitl: goto ready;        "insert 1 waitstate
state halfl: goto ready;        "half state between waitl and ready
state ready: goto idle;
equations
rdy.clk = !clk;          "specify /clk for rdy state bit
[ql..q0].clk = clk;
end WAIT
```

Figure 16. ABEL Source Code for Split Phase State Machine

BACKGROUND

When the Intel486™ microprocessor communicates with memory or I/O devices, several mechanisms exist for extending the bus cycles to accommodate slow memory or I/O devices. Bus cycle extensions are usually referred to as wait-states. One method for requesting wait-states from the Intel486 microprocessor during a bus cycle is to keep the $\overline{RDY}$ line inactive until the desired number of wait states have been incurred.

In this example design using ABEL v4.3, $\overline{RDY}$ control is implemented using a simple 3-bit state machine in an Intel 85C22V10 (see Figure 16). Two of the state bits of the WAIT state machine (q1, q0) clock on the rising edge of the system clock and one bit (RDY) utilizes the falling edge. This is made possible because the 85C22V10 allows clock inversion on a macrocell by macrocell basis. Clock assignments in ABEL are simply done in the EQUATIONS section using the syntax:

```
rdy.clk = !clk;
[q1..q0].clk = clk;
```

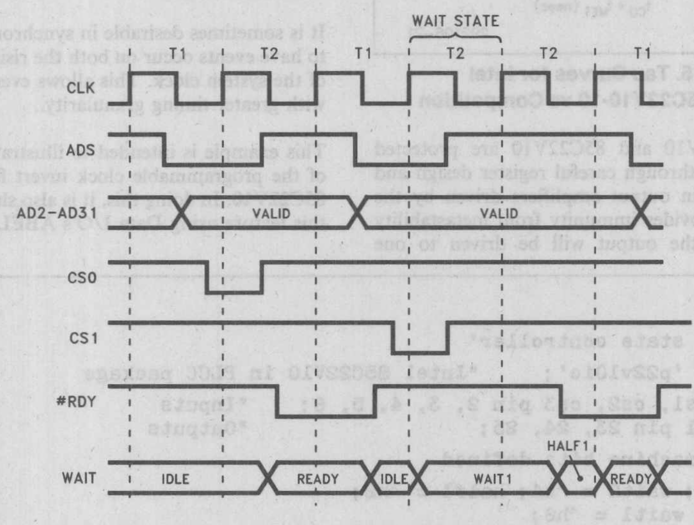


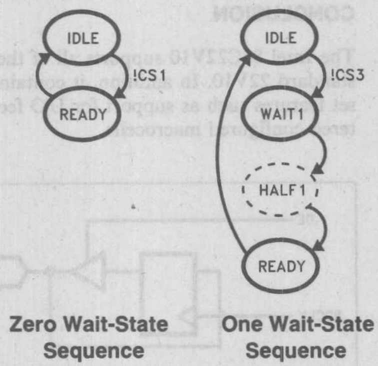
Figure 17. Bus Cycle Diagram

DESCRIPTION

By watching the Chip Select ($\overline{CS}$) lines, the WAIT state machine determines the correct number of wait states to insert, the range being from 0–3 in this example. $\overline{CS}$ signals are typically decoded from the address signals out of the Intel 486.

Referring to Figure 17, two bus cycles are shown, illustrating only the signals critical to this example. Address signals are not guaranteed to be valid out of a 33 MHz Intel486 until 16 ns after the rising edge of T1 which is already past the falling edge of T1 (assuming 50% duty cycle, 30 ns clock period). The next opportunity for a clock edge is the rising edge of T2. Using a fast PLD, such as the 7 ns Intel 85C224, the decoding of the address lines into a $\overline{CS}$ signal can be done in time to meet the required 7 ns setup time (t_{SU}) into an 85C22V10 that contains the WAIT state machine. Since the first bus cycle shown involves $\overline{CS0}$, it is a zero wait-state cycle. $\overline{RDY}$ is generated by the WAIT state machine on the falling edge of T2, in time to make the 8 ns setup time into the Intel486 before the rising edge of the next T1. Since $\overline{RDY}$ is asserted until the falling edge of T1, ample hold time is provided.

The second bus cycle requires the insertion of a wait-state. This is dictated by the assertion of $\overline{CS1}$. Now, instead of returning a $\overline{RDY}$ at the end of one T2 cycle, the WAIT state machine will wait through one additional T2 cycle. Note that for this state sequence WAIT goes through an intermediate "half state" between WAIT1 and READY. This is because the transition from WAIT1 to READY begins on the rising edge of the last T2 and is completed on the falling edge. This is illustrated as a state diagram in Figure 18. When designing a mixed clock phase state machine, care must be taken to account for intermediate half states. Valid state assignments must not conflict with half states or else proper results will not be achieved.



Assignments

	Rdy	q1	q2
Idle	1	1	1
WAIT1	1	1	0
Half1	0	1	0
Ready	0	1	1

292106–1

Figure 18. WAIT State Machine State

CONCLUSION

Obviously this design only utilizes a small portion of the 85C22V10. Ample room exists to add a bus arbiter or additional random logic.

As long as close attention is paid to state assignments, mixed clock phase state machines can be a powerful design tool for meeting tough system timing requirements.

Design Example # 2—Status Register

INTRODUCTION

The need often arises in digital system design to store a status data bit or bits in a register for later reference. Typically a bi-directional databus is used for reading and writing this data.

BACKGROUND

One of the superset features of the Intel 85C22V10 is the ability to take feedback into the device from an I/O pin on a macrocell that is configured for registered operation. Recall that the standard 22V10 provides only buried feedback when the macrocell is configured as a register. Access to this feature is available via popular 3rd party tools such as ABEL, CUPL and MINC. But for this example, Intel's PLDshell was used.

DESCRIPTION

A schematic of the desired circuit is given in Figure 19. Data is strobed into the status register via RDCLK. When it is desired to read back the value of the data, this process is controlled by OE. Up to 10 such data registers may be implemented on a single 85C22V10 with separate OE control for each.

CONCLUSION

The Intel 85C22V10 supports all of the features of the standard 22V10. In addition, it contains several superset features such as support for I/O feedback on registered configured macrocells.

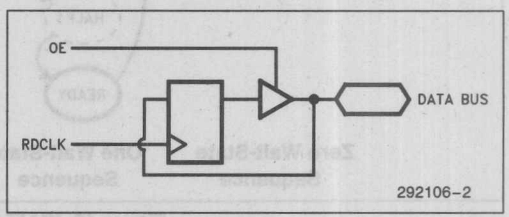


Figure 19. Status Register

```
chip STATUS_REG  85C22V10

; Inputs
PIN RDCLK
PIN CS1
PIN OE

; BIDIRECTIONAL PIN

PIN STAT REGISTERED PINFBK      ; Registered output, pin feedback

EQUATIONS

STAT = STAT                     ; Register input tied to output
STAT.CLKF = RDCLK
STAT.TRST = OE
```

Figure 20. PLDshell PLUS Design File

APPLICATION BRIEF

16-Bit Binary Counter Implementation Using the iPLD610 PLD

KARL-HEINZ WEIGL
INTEL CORPORATION
MUNICH, GERMANY

October 1993

Order Number: 292015-003

16-BIT BINARY COUNTER IMPLEMENTATION USING THE iPLD610 PLD

CONTENTS

INTRODUCTION

System designers often use programmable logic devices to implement counters. Use of PLA devices lets the user build customized counters to suit individual applications. In most cases such counters are not available, 'off-the-shelf' SSI/MSI devices. In other applications, the PLA implementation allows the designer to squeeze the counter function along with other 'glue' tasks into a single PLA, with the attendant higher integration benefits.

Use of traditional 20-pin and 24-pin PLAs, however, does not allow for the construction of large counters having greater than 10 significant bits. This is because these traditional PLAs have register and product term restrictions (even the larger bipolar PLAs have only 8 to 10 registers and less than 8 product terms per register). In contrast, the iPLD610 24-pin erasable programmable logic device (EPLD) contains 16 registers that are programmable as 'D', 'T', 'RS' or 'JK' types. These 16 programmable registers enable the construction of Up/Down counters with up to 16 significant bits.

This application brief details the implementation of a 16-bit binary counter in the iPLD610 PLD. The design also demonstrates efficient counter construction utilizing toggle flip-flops (T-FF) that allows for minimum product term utilization.

DESIGN OBJECTIVE

The objective of the design is to implement a counter with the following features: (i) 16-bit binary count, (ii) toggle flip-flops, (iii) asynchronous clear, (iv) RUN/$\overline{\text{STOP}}$ function and (v) UP/$\overline{\text{DOWN}}$ function. The function table is shown in Figure 1.

RESET	UP/DOWN	RUN/STOP	Function
X	X	0	Inhibit Counting
0	0	1	Count Down
0	1	1	Count Up
1	X	X	Reset All Outputs to 'LOW'

Figure 1

TOGGLE FLIP-FLOPS

Counters can be most effectively implemented in PLA architectures using toggle flip-flops. This is because counters constructed with 'D' type flip-flops require an additional product term for every successive significant bit, whereas toggle flip-flop implementation requires only **one** product term per significant bit. Thus, the toggle flip-flop counter design is more miserly in product term consumption than the 'D' register design. Since product term minimization is the key element to maximizing PLA utilization, the T-FF counter design is more efficient. The truth table for the toggle flip-flop is shown in Fig. 2.

T	Q(N)	Q (N + 1)
0	0	0
0	1	1
1	0	1
1	1	0

Figure 2

SOLUTION

The 16-bit binary counter function was implemented in the iPLD610 EPLD using the PLDshell Plus Development System (iPLDS). The equations for the 16-bit binary counter with the RESET, UP/$\overline{\text{DOWN}}$ and RUN/$\overline{\text{STOP}}$ functions are shown in the 'EQUATIONS' section of the PLDasm file (Fig. 3). The pinout of the iPLD610 with the implemented counter is shown in the RPT file (Utilization Report) Fig. 4. This RPT file also shows, under the 'EQUATIONS' section, that in each macrocell only one out of 8 product terms is used. In contrast the same 16-bit counter designed using 'D' type flip-flops would have required more than 16 product terms for the last significant bit.

```
TITLE           16-bit Counter Using Toggle Flip-Flops
PATTERN         AB-11
REVISION        1.0
AUTHOR          Example
COMPANY         Intel
DATE            4/27/93

CHIP    16bit_counter  PLD610

; Inputs

PIN     RS        ; RUN STOP (0 ==> INHIBIT COUNTING, 1 ==> COUNT)
PIN     RESET     ; RESET ALL OUTPUTS TO LOW (0)
PIN     UD        ; UP/DOWN (0 ==> COUNT DOWN, 1 ==> COUNT UP)
PIN     CLK       ; DEVICE SYNCHRONOUS CLOCK

; Outputs
; 16 BIT COUNTER:  (MSB) Q15 Q14 ... Q1 Q0 (LSB)

PIN     Q[15:0]      ; MSB --> LSB defined in vector notation

; CREATE "INTERMEDIATE" EQUATIONS WITH THE CONTROL SIGNALS

STRING  Q0U     '(UD * RS)'
STRING  Q1U     '(UD * Q0 * Q0U)'
STRING  Q2U     '(UD * Q1 * Q1U)'
STRING  Q3U     '(UD * Q2 * Q2U)'
STRING  Q4U     '(UD * Q3 * Q3U)'
STRING  Q5U     '(UD * Q4 * Q4U)'
STRING  Q6U     '(UD * Q5 * Q5U)'
STRING  Q7U     '(UD * Q6 * Q6U)'
STRING  Q8U     '(UD * Q7 * Q7U)'
STRING  Q9U     '(UD * Q8 * Q8U)'
STRING  Q10U    '(UD * Q9 * Q9U)'
STRING  Q11U    '(UD * Q10 * Q10U)'
STRING  Q12U    '(UD * Q11 * Q11U)'
STRING  Q13U    '(UD * Q12 * Q12U)'
STRING  Q14U    '(UD * Q13 * Q13U)'
STRING  Q15U    '(UD * Q14 * Q14U)'

STRING  Q0D     '(/UD * RS)'
STRING  Q1D     '(/UD * /Q0 * Q0D)'
STRING  Q2D     '(/UD * /Q1 * Q1D)'
STRING  Q3D     '(/UD * /Q2 * Q2D)'
STRING  Q4D     '(/UD * /Q3 * Q3D)'
STRING  Q5D     '(/UD * /Q4 * Q4D)'
STRING  Q6D     '(/UD * /Q5 * Q5D)'
STRING  Q7D     '(/UD * /Q6 * Q6D)'
STRING  Q8D     '(/UD * /Q7 * Q7D)'
STRING  Q9D     '(/UD * /Q8 * Q8D)'
STRING  Q10D    '(/UD * /Q9 * Q9D)'
STRING  Q11D    '(/UD * /Q10 * Q10D)'
STRING  Q12D    '(/UD * /Q11 * Q11D)'
STRING  Q13D    '(/UD * /Q12 * Q12D)'
STRING  Q14D    '(/UD * /Q13 * Q13D)'
STRING  Q15D    '(/UD * /Q14 * Q14D)'
```

292015–1

Figure 3. Example .PDS

```
; OUTPUTS
        Q0.T  := Q0U + Q0D
        Q1.T  := Q1U + Q1D
        Q2.T  := Q2U + Q2D
        Q3.T  := Q3U + Q3D
        Q4.T  := Q4U + Q4D
        Q5.T  := Q5U + Q5D
        Q6.T  := Q6U + Q6D
        Q7.T  := Q7U + Q7D
        Q8.T  := Q8U + Q8D
        Q9.T  := Q9U + Q9D
        Q10.T := Q10U + Q10D
        Q11.T := Q11U + Q11D
        Q12.T := Q12U + Q12D
        Q13.T := Q13U + Q13D
        Q14.T := Q14U + Q14D
        Q15.T := Q15U + Q15D

; SYNCHRONOUS CLOCKS
        Q[15:0].CLKF  = CLK

; ASYNCHRONOUS CLEAR
        Q[15:0].RSTF  = RESET

; end of design
```

292015–2

Figure 3. Example .PDS (Continued)

```
TITLE          16-BIT COUNTER USING TOGGLE FLIP-FLOPS
PATTERN        AB-11
REVISION       1.0
AUTHOR         EXAMPLE
COMPANY        INTEL
DATE           4/27/93

OPTIONS
    TURBO = ON
    SECURITY = OFF

CHIP  16BIT_COUNTER PLD610

PIN          2    RS
PIN         14    RESET
PIN         11    UD
PIN         13    CLK

PIN         22    Q15
PIN    [21:15]    Q[14:8]
PIN     [10:3]    Q[7:0]

EQUATIONS

Q15.T := UD * Q14 * Q13 * Q12 * Q11 * Q10 * Q9 * Q8 * Q7 * Q6 * Q5 * Q4
                * Q3 * Q2 * Q1 * Q0 * RS
       + /UD * /Q14 * /Q13 * /Q12 * /Q11 * /Q10 * /Q9 * /Q8 * /Q7 * /Q6
                * /Q5 * /Q4 * /Q3 * /Q2 * /Q1 * /Q0 * RS
Q15.CLKF = CLK
Q15.RSTF = RESET
Q15.SETF = GND
Q15.TRST = VCC

Q14.T := UD * Q13 * Q12 * Q11 * Q10 * Q9 * Q8 * Q7 * Q6 * Q5 * Q4 * Q3
                * Q2 * Q1 * Q0 * RS
       + /UD * /Q13 * /Q12 * /Q11 * /Q10 * /Q9 * /Q8 * /Q7 * /Q6 * /Q5
                * /Q4 * /Q3 * /Q2 * /Q1 * /Q0 * RS
Q14.CLKF = CLK
Q14.RSTF = RESET
Q14.SETF = GND
Q14.TRST = VCC

Q13.T := UD * Q12 * Q11 * Q10 * Q9 * Q8 * Q7 * Q6 * Q5 * Q4 * Q3 * Q2
                * Q1 * Q0 * RS
       + /UD * /Q12 * /Q11 * /Q10 * /Q9 * /Q8 * /Q7 * /Q6 * /Q5 * /Q4
                * /Q3 * /Q2 * /Q1 * /Q0 * RS
Q13.CLKF = CLK
Q13.RSTF = RESET
Q13.SETF = GND
Q13.TRST = VCC

Q12.T := UD * Q11 * Q10 * Q9 * Q8 * Q7 * Q6 * Q5 * Q4 * Q3 * Q2 * Q1 * Q0
                * RS
       + /UD * /Q11 * /Q10 * /Q9 * /Q8 * /Q7 * /Q6 * /Q5 * /Q4 * /Q3 * /Q2
                * /Q1 * /Q0 * RS
Q12.CLKF = CLK
Q12.RSTF = RESET
Q12.SETF = GND
Q12.TRST = VCC
```

292015-3

Figure 4. Example .RPT

```
Q11.T  := UD * Q10 * Q9 * Q8 * Q7 * Q6 * Q5 * Q4 * Q3 * Q2 * Q1 * Q0 * RS
       + /UD * /Q10 * /Q9 * /Q8 * /Q7 * /Q6 * /Q5 * /Q4 * /Q3 * /Q2 * /Q1
               * /Q0 * RS
Q11.CLKF = CLK
Q11.RSTF = RESET
Q11.SETF = GND
Q11.TRST = VCC

Q10.T  := UD * Q9 * Q8 * Q7 * Q6 * Q5 * Q4 * Q3 * Q2 * Q1 * Q0 * RS
       + /UD * /Q9 * /Q8 * /Q7 * /Q6 * /Q5 * /Q4 * /Q3 * /Q2 * /Q1 * /Q0
               * RS
Q10.CLKF = CLK
Q10.RSTF = RESET
Q10.SETF = GND
Q10.TRST = VCC

Q9.T  := UD * Q8 * Q7 * Q6 * Q5 * Q4 * Q3 * Q2 * Q1 * Q0 * RS
      + /UD * /Q8 * /Q7 * /Q6 * /Q5 * /Q4 * /Q3 * /Q2 * /Q1 * /Q0 * RS
Q9.CLKF = CLK
Q9.RSTF = RESET
Q9.SETF = GND
Q9.TRST = VCC

Q8.T  := UD * Q7 * Q6 * Q5 * Q4 * Q3 * Q2 * Q1 * Q0 * RS
      + /UD * /Q7 * /Q6 * /Q5 * /Q4 * /Q3 * /Q2 * /Q1 * /Q0 * RS
Q8.CLKF = CLK
Q8.RSTF = RESET
Q8.SETF = GND
Q8.TRST = VCC

Q7.T  := UD * Q6 * Q5 * Q4 * Q3 * Q2 * Q1 * Q0 * RS
      + /UD * /Q6 * /Q5 * /Q4 * /Q3 * /Q2 * /Q1 * /Q0 * RS
Q7.CLKF = CLK
Q7.RSTF = RESET
Q7.SETF = GND
Q7.TRST = VCC

Q6.T  := UD * Q5 * Q4 * Q3 * Q2 * Q1 * Q0 * RS
      + /UD * /Q5 * /Q4 * /Q3 * /Q2 * /Q1 * /Q0 * RS
Q6.CLKF = CLK
Q6.RSTF = RESET
Q6.SETF = GND
Q6.TRST = VCC

Q5.T  := UD * Q4 * Q3 * Q2 * Q1 * Q0 * RS
      + /UD * /Q4 * /Q3 * /Q2 * /Q1 * /Q0 * RS
Q5.CLKF = CLK
Q5.RSTF = RESET
Q5.SETF = GND
Q5.TRST = VCC

Q4.T  := UD * Q3 * Q2 * Q1 * Q0 * RS
      + /UD * /Q3 * /Q2 * /Q1 * /Q0 * RS
Q4.CLKF = CLK
Q4.RSTF = RESET
Q4.SETF = GND
Q4.TRST = VCC

Q3.T  := UD * Q2 * Q1 * Q0 * RS
      + /UD * /Q2 * /Q1 * /Q0 * RS
```

292015-4

Figure 4. Example .RPT (Continued)

```
Q3.CLKF = CLK
Q3.RSTF = RESET
Q3.SETF = GND
Q3.TRST = VCC

Q2.T := UD * Q1 * Q0 * RS
      + /UD * /Q1 * /Q0 * RS
Q2.CLKF = CLK
Q2.RSTF = RESET
Q2.SETF = GND
Q2.TRST = VCC

Q1.T := UD * Q0 * RS
      + /UD * /Q0 * RS
Q1.CLKF = CLK
Q1.RSTF = RESET
Q1.SETF = GND
Q1.TRST = VCC

Q0.T := RS
Q0.CLKF = CLK
Q0.RSTF = RESET
Q0.SETF = GND
Q0.TRST = VCC
```

292015-5

Figure 4. Example .RPT (Continued)

APPLICATION NOTE

iPLD610 Design Guide

JOHN CASEY
PROGRAMMABLE LOGIC APPLICATIONS
INTEL CORPORATION

October 1993

Order Number: 292074-003

CONTENTS

1.0 INTRODUCTION

Designers today are faced with the challenge of implementing very high performance systems in a cost-effective and timely manner. When these responsibilities are factored with concerns about reliability, power consumption, and migrating the design to the next performance level, the designer's job becomes more complex. When all these requirements are compared against the possible solutions spanning full-custom, semi-custom, application-specific, and programmable logic, the only sure result is a headache.

Intel's Microcomputer Programmable Logic Devices (μPLDs) can meet many of today's system requirements, as well as map the path to the next generation of products. Intel μPLDs provide a high-speed CMOS logic solution required by current microprocessors and VLSI peripherals.

DOCUMENT OVERVIEW

This design guide provides technical support for designers, design managers, components engineers, and others interested in using Intel's iPLD610. The information provided here is intended to support both the decision making process prior to the design and, the qualification process which occurs during and after the design. The format of this design guide is as follows:

Section 2—Product Overview: This section discusses the device highlights and architecture of the iPLD610.

Section 3—Specification Analysis: The key D.C. and A.C. Specs (from the data sheet) are discussed and compared against competitive devices. This section provides a baseline for comparison and device selection. Also, some insights are provided on how to best use the data sheet specifications.

Section 4—Advanced Design Issues: This section includes presentation of data and discussion of issues affecting high-speed systems designs. Topics include output slew rates, effects of capacitive loading of outputs, and synchronous/asynchronous register operation.

Section 5—Application Ideas: This section offers some ideas on how to use the unique performance/architecture combination offered by the Intel iPLD610.

Section 6—Programming/Development Support: This section offers details on existing Intel development/programming tools as well as third-party support. Also discussed is programming compatibility with other devices.

Section 7—Design Upgrade: There may be a desire to upgrade an existing design to the Intel iPLD610. This task is discussed, specifically vis-a-vis the Intel 5C060, Altera/TI/EP6x0, 22V10, and 20RA10.

Related Documents

Title	Intel Order No
iPLD610 CMOS μPLD Data Sheet	290455
iPLD910 CMOS μPLD Data Sheet	290456
Intel Programmable Logic Handbook	296083
Metastability Characteristics of Intel PLDs	292071
PLD Quality and Reliability Data Summary	293003

2.0 PRODUCT OVERVIEW

In programmable logic, several architectures have arisen as industry standards. Each architecture has a unique set of features. The Intel iPLD610 represents the top performer in one of these industry standard architectures. The iPLD610 is an upgrade of the existing Intel 5C060 and Altera EP600 devices. Although the architectures (i.e., pin-out, logic array, macrocell features, JEDEC map) are *exactly* the same, the iPLD610 represents a very significant performance upgrade. It should also be noted that devices with this same architecture are manufactured by other leading programmable logic vendors including AMD and TI.

FEATURES

The features provided by the Intel iPLD610 include the following highlights:

— 16 programmable macrocells (I/O pins)

— 28-pin PLCC package

— EPROM cell, CMOS Technology (UV Erasable)

— 100% Silicon Testability

— Programmable Standby Current Mode ($<$100 μA)

— Low Operating Power (105 mA Max)

— High Performance Operation (10 ns t_{PD}, 6.5 ns t_{CO_1}, 85 MHz State Machine Frequency)

— Programmable Security Bit

— Programmable Register Type

PACKAGING

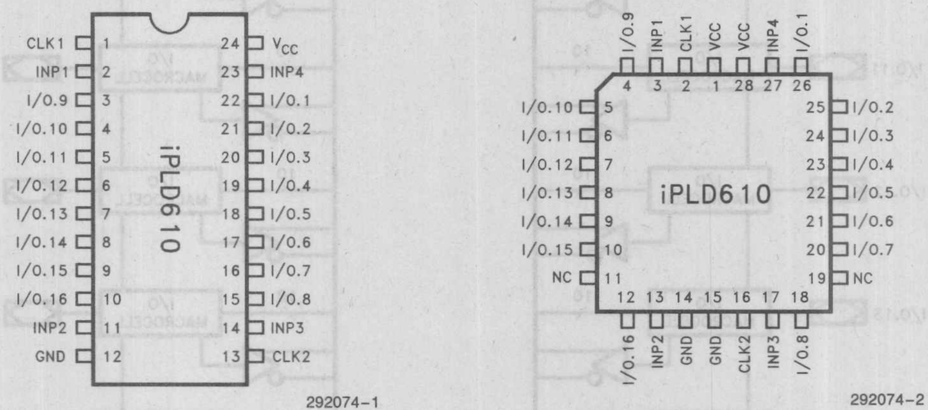
Figure 1 shows the pinouts of the DIP and PLCC packages for the iPLD. The DIP version is available in plastic, one-time-programmable (OTP). The PLCC version comes in a 28-pin OTP package.

PROCESS

The iPLD610 uses CMOS EPROM (floating gate) cells as logic control elements instead of fuses. The CMOS EPROM technology reduces power consumption in comparision to bipolar devices without sacrificing speed performance. In addition, Intel's advanced CMOS III-E EPROM process technology enables higher logic densities to be achieved with superior speed and low-power performance over other comparable devices. Intel's μPLDs add the benefits of "zero" stand-by power not available on other programmable logic devices. EPROM technology allows these devices to be 100% factory tested by programming and erasing all the EPROM logic control elements.

DEVICE ARCHITECTURE

The overall device architecture, as presented in Figure 2, shows several architectural highlights of this device. In this 24/28 pin device there are 16 macrocells, each of which represents an I/O pin, buried register or dedicated input. There are also four dedicated input pins and two dedicated clock pins.



(a) DIP Pinout

(b) PLCC Pinout

Figure 1. iPLD610 Pinout Diagrams

*CMOS is a patented process of Intel Corporation.

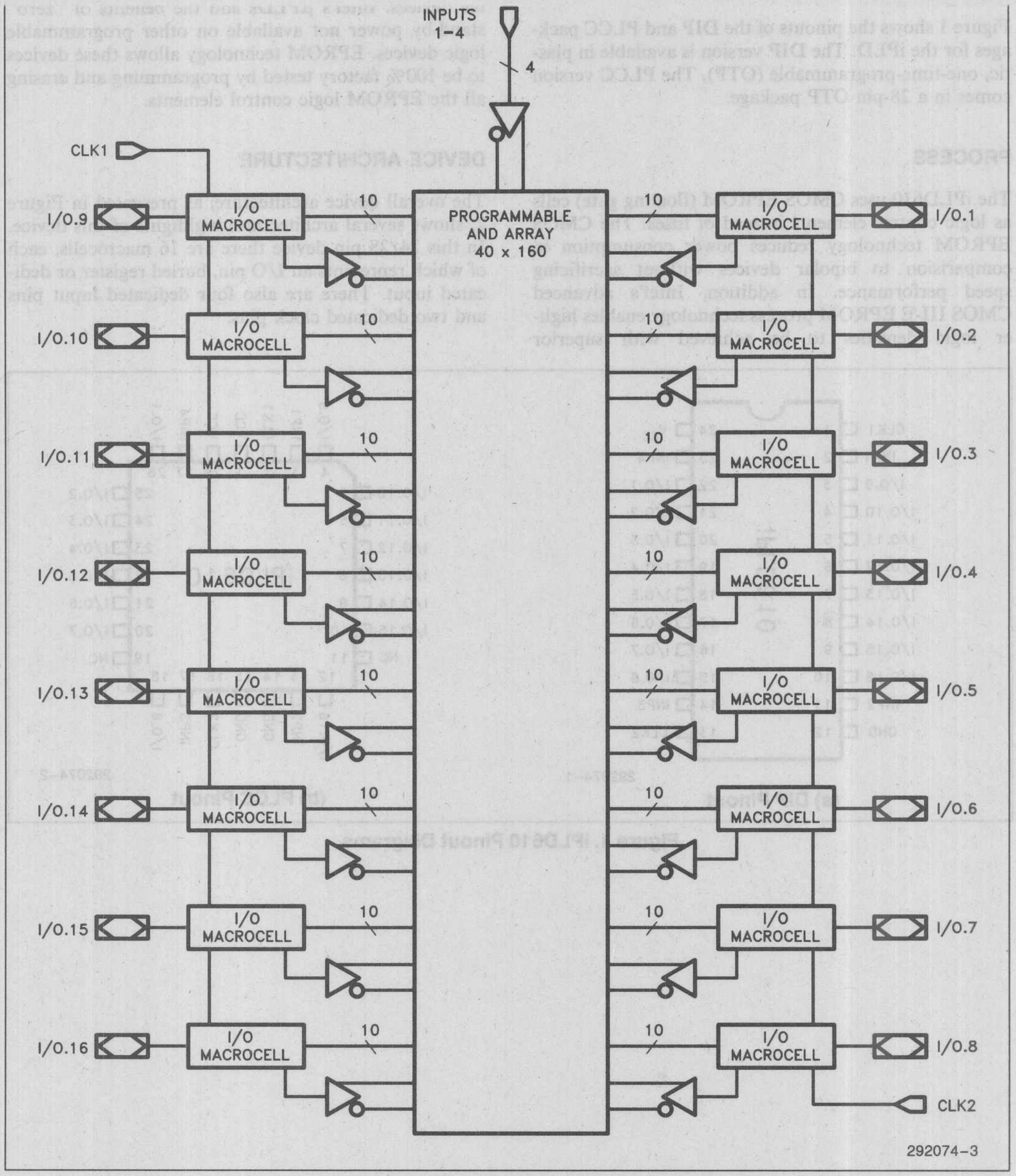


Figure 2. iPLD610 Global Architecture

The dedicated clock pins offer the system designer added flexibility. The CLK1 pin provides a synchronous clock input to macrocells 9–16 and the CLK2 pin provides a dedicated synchronous clock input for macrocells 1–8. The advantages of this architecture feature are quite obvious as the list of applications could include:

a) Dual state-machine operation within the same device

b) Using logic that requires operations at CLK_X and $\overline{CLK_X}$

c) Implementing system control logic requiring both a 1x CLK and a 2x CLK (as can often be the case with the Intel 80386DX/SX and 80286 microprocessors)

d) Use of some macrocells as "input latches" accepting asynchronous inputs, whose states are subsequently acted upon using another clock input.

MACROCELL ARCHITECTURE

The next level of detail to examine the iPLD610 is at the macrocell level. Figure 3 provides an overview of the macrocell architecture. There are several key features that make this device very useful to system designers by overcoming limitations of the standard PAL*/GAL**/22V10 capabilities. Every macrocell of the iPLD610 has 8 sum of product terms for standard logic implementation. There is a separate product term for Asynchronous Register clear (Reset) for each register. In addition, there is a product term that can be programmed as either an asynchronous clock input to the register or as an output enable control. This asynchronous clocking capability for each macrocell provides yet another level of clocking flexibility to an already advanced architecture. The output enable control available on each macrocell allows any I/O pin to be tri-stated and provides for full control of pins used as both inputs and outputs. The feedback from each macrocell can be direct register feedback or pin feedback. Several macrocell options are detailed in the iPLD610 Data Sheet (Lit. No. 290455). Each macrocell can be configured to implement registered or combinational logic. Register types available include D, T, JK and RS. This provides designers register types not found in many of the common programmable logic devices. Register type selection is also a common way to reduce product term requirements (rather than just going to higher product term devices), as logic development tools can minimize equations for the best fit. Whether registered or combinational logic is implemented, there is also an inversion control within each macrocell. Again, this can help designers minimize logic and control output polarities by using DeMorgan's inversion rules on equations.

*PAL is a registered trademark of Advanced Micro Devices.
**GAL is a registered trademark of Lattice Semiconductor, Inc.

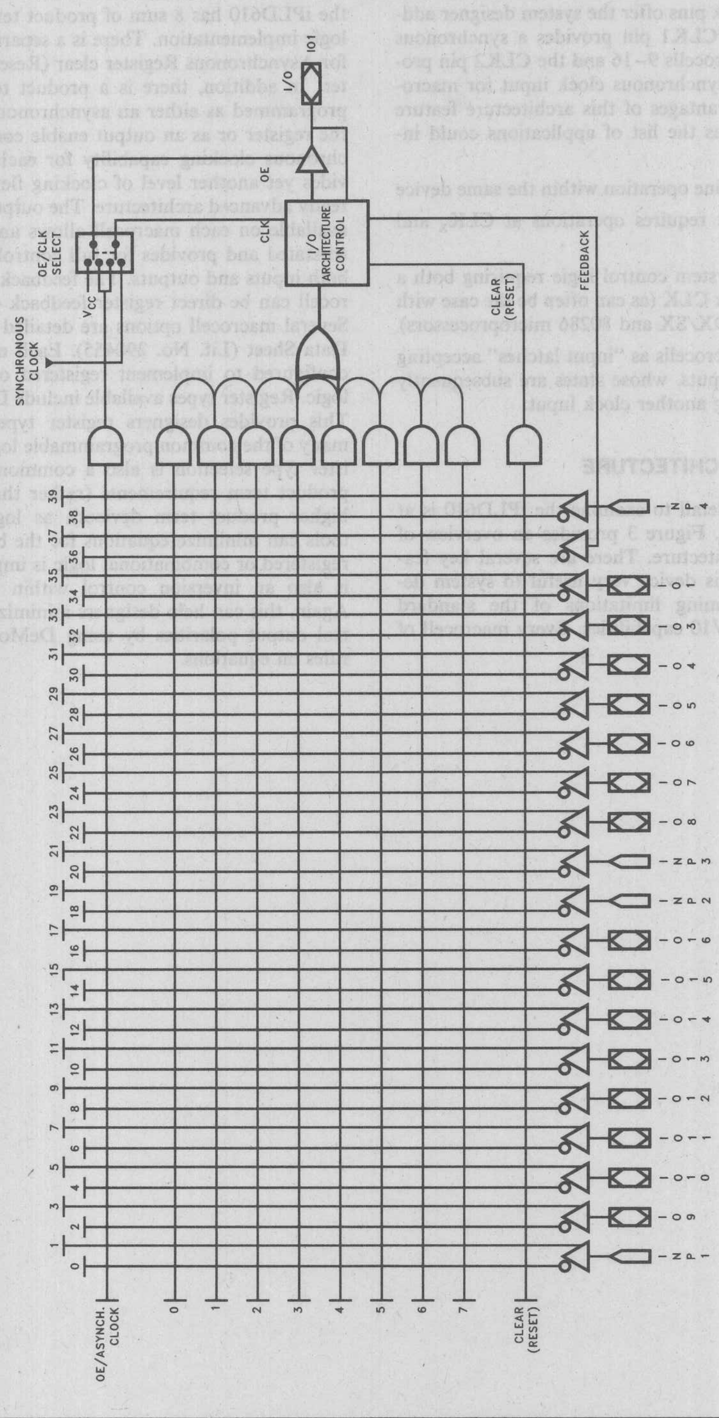


Figure 3. iPLD610 Macrocell Architecture

3.0 SPECIFICATION ANALYSIS

When designing with any IC, a designer would like to know two things:

1) How is the part guaranteed to act (i.e., what are its specifications)

2) How will it act in it's actual design environment

The first item above will be covered in this section. Using the data sheet A.C. and D.C. specifications a designer can perform a "paper analysis" of the circuit. The questions to be answered here are "How does the Intel iPLD610 compare with competitive devices" and "How can the A.C. and D.C. specs best be used?"

The second item is much harder to quantify due to the vast differences between designs. However, a great deal of bench data has been collected and presented in Section 4, which will help the designer make these assessments.

D.C. characteristics of the Intel iPLD610 are covered first. Next follows a comparison of these values with competitive devices. Following this is an overview of the A.C. specifications for the iPLD610 and, finally, a comparison of these specifications with other devices.

3.1 D.C. Characteristics Analysis

TTL Compatibility

D.C. characteristics address the direct current components of operating any IC. The areas covered include input and output voltage and current levels, and I_{CC} supply current consumption.

The input voltage levels (V_{IH} and V_{IL}) show that the iPLD610 can be driven by standard TTL or CMOS logic components, so the designer doesn't need to worry about mixing logic families—even though the iPLD610 is a CMOS PLD. The V_{OH} and V_{OL} show that the iPLD610 can drive TTL loads over the specified test conditions. CMOS loads are capacitive in nature and do not require much current (typically measured in μA).

I_{OL} Specifications

The V_{OL} test condition shows that each iPLD610 is capable of handling a 12 mA load while maintaining the output at or below 0.45V. Refer to Figure 17 (in Section 4) if another V_{OL}/V_{OH} value is required. That figure provides typical values for the output driver of the iPLD610.

Also in the D.C. specifications of the iPLD610 is a note specifying the total I_{OL} for each "bank" of 8 macrocells is 64 mA. This is the maximum recommended D.C. (steady state) current for this device. Even though the iPLD610 can sink 12 mA on each output, this 64 mA/bank limit should be observed to reduce electromigration effects. The duty cycle of each output should be incorporated when calculating the steady state device current. For example, each output of a 4-bit counter is active 50% of the time. The maximum current for each bank is 96 mA.

The input and output leakage current specifications are ± 10 μA (per pin). This is an average value for CMOS devices. Typically, though, the total leakage for all pins (combined) will be within this ± 10 μA range.

I_{CC} Specifications

Probably the D.C. specification of the greatest concern to most designers is the I_{CC} value. This value tells the designer how much current will be required and how much heat (watts) will be generated by each device. Therefore, the I_{CC} specifications of a device will affect both the power supply requirements and the board reliability. To generate I_{CC} values, the device is tested with no load to find out how much power is consumed by the device itself.

Since CMOS devices consume most of their power during transitions, I_{CC} will greatly vary with the frequency of the clock or other inputs. For this reason not only are two values of I_{CC} specified in the D.C. characteristics (at 1 MHz), but an I_{CC} versus frequency graph is given at the back of the data sheet allowing more precise current/power calculations. This graph provides "typical" I_{CC} values (i.e., V_{CC} = 5.0V, temp = 25°C).

Another specification related to I_{CC} is the standby current specification, I_{SB}. This specification gives both typical and maximum values for power consumption when the iPLD610 is in standby mode.

To be in standby mode the device must be programmed with TURBO = OFF and no inputs can have changed state for 75 ns. Wakeup time adds an additional 25 ns to the propagation delay through the device as measured from the first input change (see Figure 4). The standby mode programming option provides designers of power-sensitive applications such as laptop PCs with the capability to greatly reduce the system's power budget.

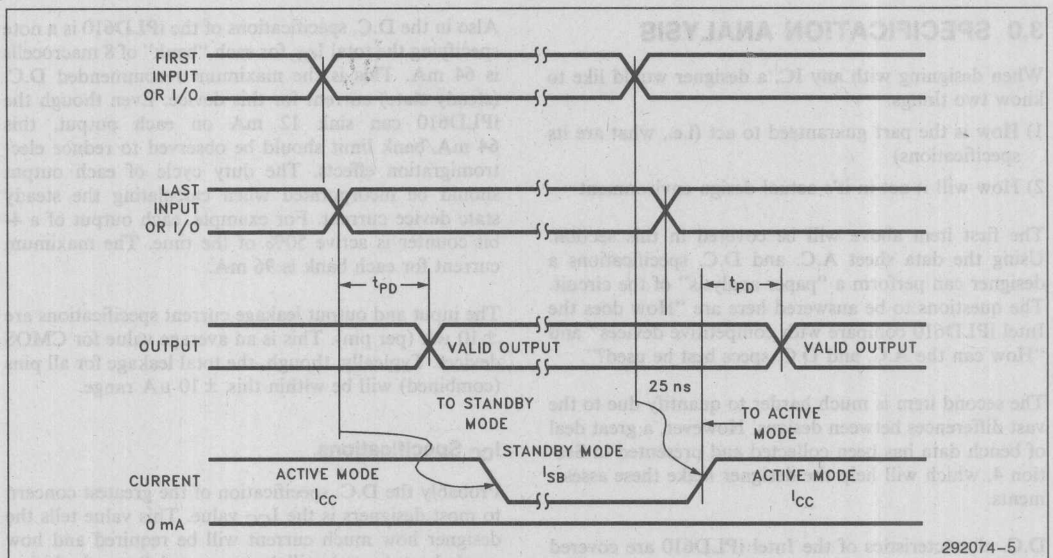


Figure 4. iPLD610 Standby and Active Mode Transitions

3.2 D.C. Specification Comparison

The voltage specifications for the iPLD610 and competitive devices do not differentiate where these devices can be used. For this reason Table 1, below, concentrates on the current specifications.

The conclusions from this table are clear. The Intel iPLD610 provides the lowest power consumption (I_{CC}) while providing the highest output drive capability (12 mA). Also, it's values for standby current are comparable to the other devices (although the AMD PALCE630 does not offer a standby mode).

Table 1. D.C. Specification Comparison

Spec	I_{CC} (@ 1 MHz)		I_{SB}		Output Current	
Part No.	Typical	Max	Typ	Max	I_{OL}	I_{OH}
Intel iPLD610	3 mA	8 mA	20 μA	150 μA	12 mA	−4 mA
Intel 5C060	10 mA	15 mA	20 μA	100 μA	4 mA	−4 mA
Altera EP630	5 mA	10 mA	20 μA	150 μA	4 mA	−4 mA
Altera EP610	3 mA	10 mA	20 μA	100 μA	4 mA	−4 mA
TI EP610	3 mA	10 mA	20 μA	100 μA	4 mA	−4 mA
AMD PALCE630	Not Availl.	Not Avail.	Not Supported	Not Supported	8 mA	−4 mA

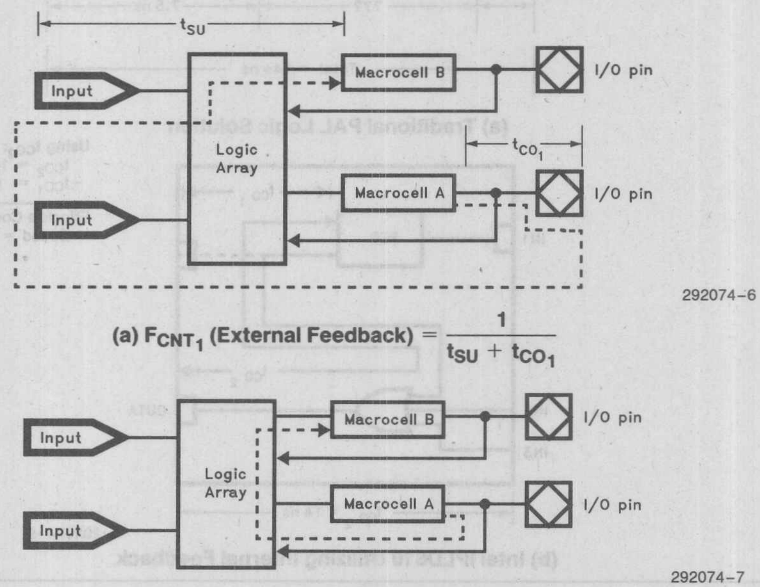
COMBINATORIAL

A.C. specifications provide the real "meat" of the data sheet by stating the guaranteed performance of the device. The first section of A.C. characteristics are the combinatorial mode A.C. characteristics. These state timings of non-registered logic paths in the iPLD610 including propagation delays (t_{PD1} and t_{PD2}), output enable/disable times (t_{PZX} and t_{PXZ}), and asynchronous reset time for any register (t_{CLR}). These specifications are stating the times from any I/O or input pin until the selected function is performed. Propagation delays include AND/OR logic provided by up to eight product terms.

SYNCHRONOUS

The next table in the iPLD610 data sheet is the "Register Mode—Synchronous Clock A.C. Characteristics" which includes specifications related to using any macrocell in registered mode which is clocked with CLK1 or CLK2. The specifications of primary importance here revolve around the register setup time (t_{SU}) and register clock to output time (t_{CO_1}). The setup time is the minimum time allowed between valid data appearing on an input and the active clock edge. The is clocked at the register until valid data shows up at the output pin. The reason these two specifications are of concern is that together they determine the worst case throughput performance in registered mode. One highlight of the iPLD610 is how closely they match standard "E-PAL" specifications. Section 3.4 includes a summary of iPLD610 versus PAL performance. The maximum counter frequency, F_{CNT_1}, represents the maximum counter frequency with the iPLD610 using external feedback. External feedback means routing an output pin to another pin as an input. In this case the designer incurs both input and output buffer delays—but, this also simulates the activity of a multiple device counter or state machine. A related specification, F_{CNT_2}, represents the maximum counter (state machine) frequency using internal device feedback. F_{CNT_2} is higher than F_{CNT_I} due to elimintion of an input and output buffer from the feedback path. Figure 5 provides an overview of both F_{CNT} values.

The designer must also be aware that the F_{MAX} specification states the maximum frequency at which the registers in the iPLD610 can be clocked. This is due to the physical limitations on the period of the clock input (it could also be limited by register setup time). Therefore, $F_{MAX} = 1/t_{CW}$ (= 1/min clock width).



(a) F_{CNT_1} (External Feedback) $= \dfrac{1}{t_{SU} + t_{CO_1}}$

(b) F_{CNT_2} (Internal Feedback)

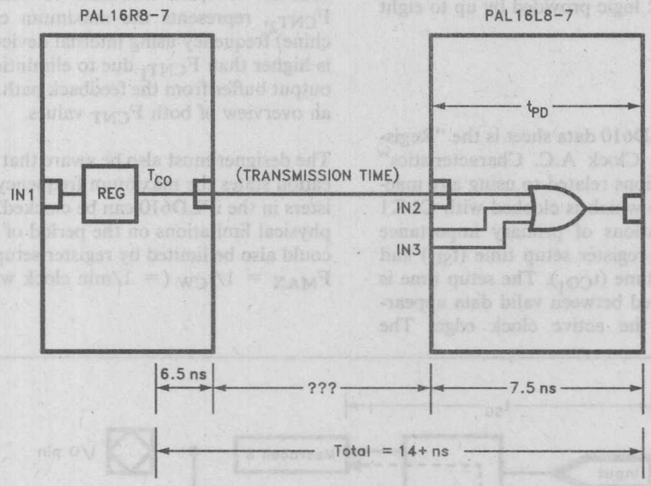
Figure 5. F_{CNT} Overview

Designs utilizing programmable logic can make full use of the iPLD610 by understanding the applications of F_{CNT_1} (used for multiple device state machines), F_{CNT_2} (used for smaller, single device state machines), and F_{MAX} (used for register pipelining applications).

Another A.C. specification of interest is t_{CO_2} which represents the time from CLK high to output valid fed through a combinatorial macrocell. Figure 6 depicts the difference between t_{CO_1} and t_{CO_2}. The t_{CO_2} specification shows the advantages of using internal feedack to gain speed when register output signals are used in combinatorial logic equations.

ASYNCHRONOUS

For each of the synchronous clock A.C. characteristics there is an asynchronous clock A.C. characteristic specified in the data sheet. Each macrocell of the iPLD610 can be programmed to be clocked with an asynchronous clock (generated by a separate product term in each macrocell). The asynchronous clock values closely mirror the synchronous specifications in both definition and value, but, there are a few notable differences.



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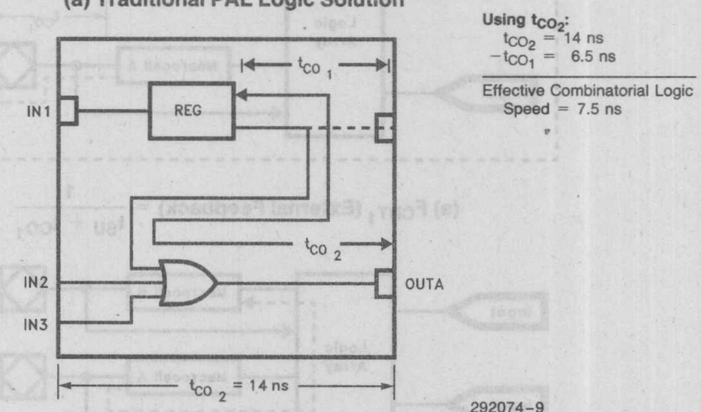
(a) Traditional PAL Logic Solution



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(b) Intel iPLD610 Utilizing Internal Feedback

Figure 6. Equivalent Combination Logic Speed Using t_{CO_2}

The synchronous register setup and hold time specifications (t_{SU} and t_H) are 7 ns and 0 ns, respectively. The asynchronous register specifications show a shifting of specifications due to differences in internal paths. The asychronous register setup and hold time specifications (t_{ASU} and t_{AH}) are 2 ns and 3 ns, respectively. A similar shifting is seen if register setup and clock-to-output specifications are compared for synchronous and asynchronous operation as detailed in Figure 7.

Understanding of these differences between synchronous and asynchronous specifications can be useful to a designer. If a system design requires a short setup time (in the 2 ns–5 ns range) one or more of the macrocells of the iPLD610 could be used in the asynchronous clocking mode. Either a control input or the system's synchronous clock could be routed to an input or I/O pin to establish the necessary "asynchronous" clock. With this technique, setup times as low as 3 ns can be met by the iPLD610, although there is the trade off of a longer register clock-to-output delay. Low setup times are often required to accommodate output valid delay specifications of many microprocessors and system peripherals.

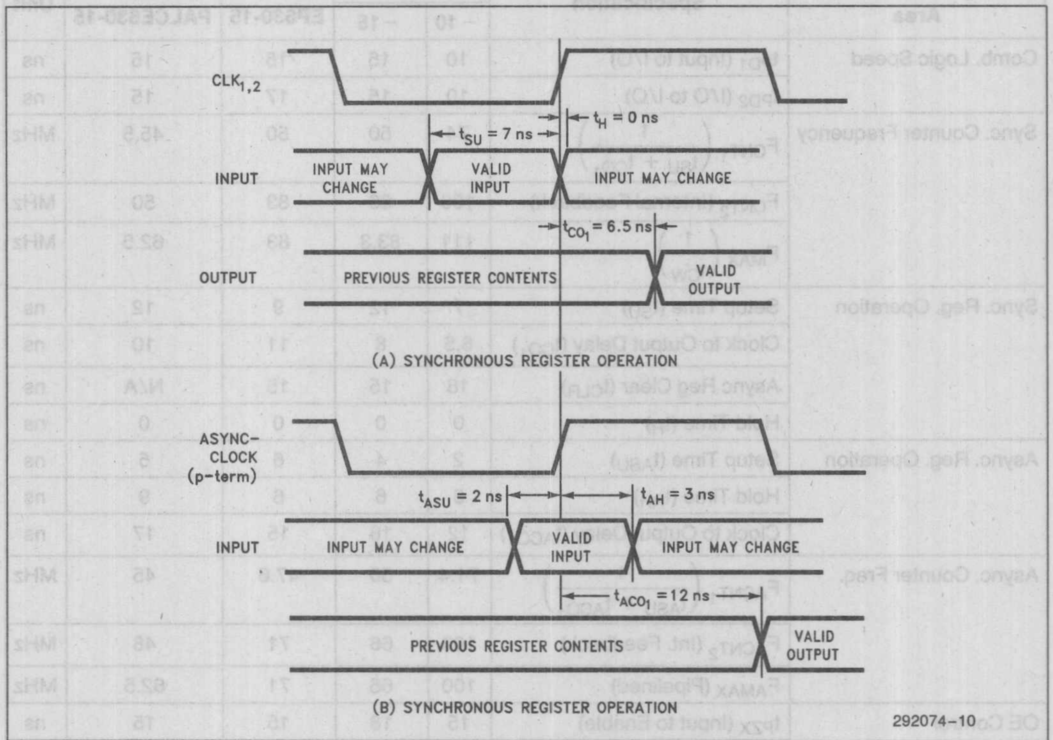


Figure 7. iPLD610 Register Timings

The comparison made here involves other devices with the same architecture as the Intel iPLD610. This includes devices from Altera, TI and AMD. It should be noted that Tables 2 and 3 (below) do not compare all A.C. specifications, rather only those best reflecting the performance of these devices. Even though the architectures of these devices (i.e., pinout, product term, there are some differences in the test conditions used to generate A.C. specification. These differences are noted.

The first comparison involves the higher speed parts—those in the 10 ns–15 ns range for t_{PD}. The second comparison will involve slower parts—those with a t_{PD} of 25 ns. The final comparison shows a summary of iPLD610 performance versus standard PAL devices.

Table 2. A.C. Specification Comparison—High Performance

Specification Area	Specification	iPLD610		Altera	AMD	Unit
		−10	−15	EP630-15	PALCE630-15	
Comb. Logic Speed	t_{PD1} (Input to I/O)	10	15	15	15	ns
	t_{PD2} (I/O to I/O)	10	15	17	15	ns
Sync. Counter Frequency	$F_{CNT_1}\left(\frac{1}{t_{SU} + t_{CO_1}}\right)$	74	50	50	45.5	MHz
	F_{CNT_2} (Internal Feedback)	100	66	83	50	MHz
	$F_{MAX}\left(\frac{1}{t_{CW}}\right)$	111	83.3	83	62.5	MHz
Sync. Reg. Operation	Setup Time (t_{SU})	7	12	9	12	ns
	Clock to Output Delay (t_{CO_1})	6.5	8	11	10	ns
	Async Reg Clear (t_{CLR})	18	15	15	N/A	ns
	Hold Time (t_H)	0	0	0	0	ns
Async. Reg. Operation	Setup Time (t_{ASU})	2	4	6	5	ns
	Hold Time (t_{AH})	3	6	6	9	ns
	Clock to Output Delay (t_{ACO_1})	12	16	15	17	ns
Async. Counter Freq.	$F_{ACNT_1}\left(\frac{1}{t_{ASU} + t_{ACO_1}}\right)$	71.4	50	47.6	45	MHz
	F_{ACNT_2} (Int. Feedback)	100	66	71	48	MHz
	F_{AMAX} (Pipelined)	100	66	71	62.5	MHz
OE Control	t_{PZX} (Input to Enable)	15	18	15	15	ns
	t_{PXZ} (Input to Disable)	13	18	15	15	ns

Table 3. A.C. Specification Comparison—Mid Range Device Propagation Delay = 25 ns

Specification Area	Specification	iPLD610-25	Altera/TI EP610-25	AMD PALCE630-25	Unit
Comb. Logic Speed	t_{PD1} (Input to I/O)	25	25	25	ns
	t_{PD2} (I/O to I/O)	25	27	25	ns
	t_{CLR} (Async Reg Clear)	25	27	N/A	ns
Sync. Register Performance	$F_{CNT_1}\left(\frac{1}{t_{SU} + t_{CO_1}}\right)$	40	27.8	37	MHz
	F_{CNT_2} (Int Feedback)	40	40	40	MHz
	$F_{MAX}\left(\text{Pipelined} = \frac{1}{t_{CP}}\right)$	66	47.6	50	MHz
Sync Register Operation	t_{SU} (Setup Time)	15	21	15	ns
	t_H (Hold Time)	0	0	0	ns
	t_{CO_1} (Clock to Output Delay)	10	15	12	ns
Async Register Performance	F_{ACNT_1} (Ext. Feedback)	33.3	28.5	28.6	MHz
	F_{ACNT_2} (Int. Feedback)	40	40	29	MHz
	F_{AMAX} (Pipelined)	50	47.6	41.6	MHz
Async Register Operation	t_{ASU} (Setup Time)	5	8	8	ns
	t_{AH} (Hold Time)	8	12	12	ns
	t_{ACO_1} (Clock to Output Delay)	25	27	27	ns
OE Control	t_{PZX} (Input to Enable)	25	25	25	ns
	t_{PXZ} (Input to Disable)	25	25	25	ns

3

At the "slower" end of the product line (t_{PD} = 25 ns), the iPLD610 provides an upgrade to existing 25 ns t_{PD} devices—especially in the area of synchronous register operations. From there a designer can migrate a design to the iPLD610-15 and finally to the state-of-the-art in architecture/performance, the Intel iPLD610-10.

PAL Comparison

A common application for higher integration devices such as the iPLD610 μPLD is upgrading existing PAL designs. Table 4 summarizes the performance specifications of the iPLD610 and standard PAL devices. The primary register-related specifications of the iPLD610, t_{SU} and t_{CO_1}, are equal to E-PAL performance levels. This results in F_{CNT_1} specifications between the two devices which are very close. Also of note is that F_{MAX} of the iPLD610 is 111 MHz, compared to 100 MHz for the E-PAL. The major differences between the iPLD610 and the PAL devices are in the t_{PD} and I_{CC} values. The iPLD610 cannot meet the faster combinational logic speeds of PAL devices, however, PALs require about 2 times more current than the iPLD610. This I_{CC} difference is important in many design areas including power supply sizing, cooling requirements, and overall system reliability.

Table 4. iPLD610 vs PAL Performance Summary

Specification	iPLD610	"E-PAL" 20xx-7	"D-PAL" 20xx-10	Units
t_{SU}	7	7	10	ns
t_{CO_1}	6.5	6.5	8	ns
F_{CNT_1}	74	74	55.5	MHz
F_{MAX}	111	100	71.4	MHz
t_{PD}	10	7.5	10	ns
I_{CC}(max)	105	210	210	mA

4.0 ADVANCED DESIGN ISSUES

As system designs climb to higher speeds and time to market becomes more critical, designers require more detailed information than is available in the data sheet. The main emphasis here is to provide designers with characterization data of key aspects of the iPLD610. This data will help avoid unforseen problems in the design, prototype, and production phases.

Data was measured with the output load specified in the iPLD610 data sheet (shown also in Figure 8), unless otherwise specified. The topics covered in this section are:

- Output Slew Rates
- Combinational Logic Concerns (t_{PD} Characteristics)
- Synchronous Register Operation Characteristics
- Asynchronous Register Operation Characteristics
- Output Current Characteristics
- Design Considerations

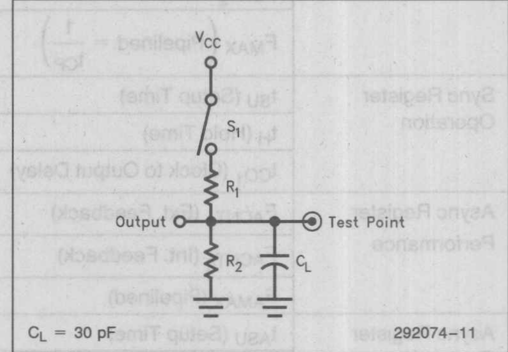
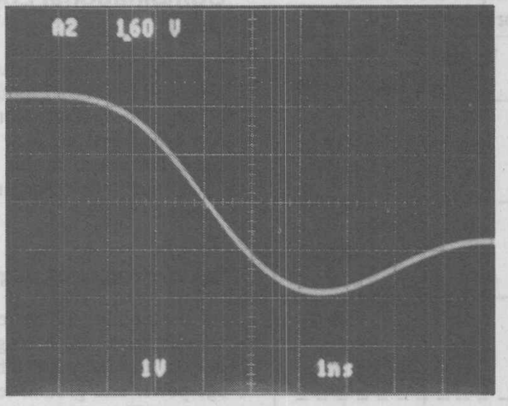


Figure 8. A.C. Testing Load Circuit

Output Slew Rates

Several key advantages of using Intel μPLDs are derivatives of the output buffer design. One of these is slow output slew rates which minimizes system noise. Signal ringing (noise) can result if output rise times are shorter then twice the signal transmission time. Thus, the faster the edge rate of any device output the shorter the board trace that is allowable before transmission line effects must be considered. This generally involves series or parallel termination and more consideration of device location and signal routing. The iPLD610 seeks to limit these design problems by providing lower output slew (edge) rates.

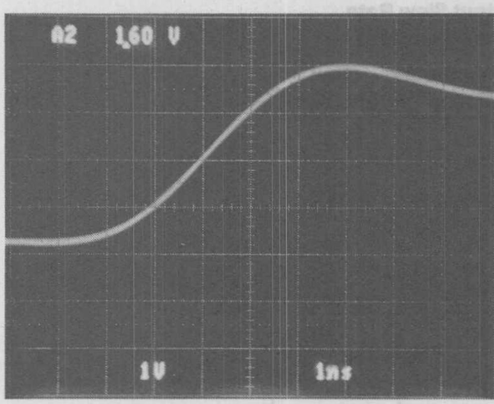
Figures 9 and 10 provide a sample of the iPLD610 output slew rate characterization. Table 5 shows there is very little variation over temperature, although the values do decrease as temperature increases. Table 6 shows there is very little variation over the number of outputs switching simultaneously, although it does decrease as the number of outputs increases. The results show output slew rates comparable to those of bipolar PALs and much lower than CMOS GALs (which are in the 3–5 V/ns range). The edge rates provided by the iPLD610 provide designers with flexibility without constantly worrying about transmission line effects.



292074-12

Temp. = 25°C
Spec. Load
V_{CC} = 5.0V
8 Outputs Switching

Figure 9. iPLD610 Output Slew—H → L Transition



292074-13

Temp. = 25°C
Spec. Load
V_{CC} = 5.0V
8 Outputs Switching

Figure 10. iPLD610 Output Slew—L → H Transition

vs Temperature

Transition	Package Type	Temp (°C)	Slew Rate (V/ns)
L → H	PDIP	0	1.1
	PDIP	25	1.1
	PDIP	70	1.0
	CerDIP	0	1.0
	CerDIP	25	1.0
	CerDIP	70	0.9
H → L	PDIP	0	1.2
	PDIP	25	1.2
	PDIP	70	1.1
	CerDIP	0	1.2
	CerDIP	25	1.2
	CerDIP	70	1.1

V_{CC} = 5.0V
No outputs switching = 8

Table 6. iPLD610 Output Slew Rate vs Number of Outputs Switching

Transition	Package Type	No. of Outputs Switching	Slew Rate (V/ns)
L → H	PDIP	2	1.1
	PDIP	8	1.1
	PDIP	15	1.0
	CerDIP	2	1.1
	CerDIP	8	1.0
	CerDIP	15	0.9
H → L	PDIP	2	1.3
	PDIP	8	1.2
	PDIP	15	1.2
	CerDIP	2	1.3
	CerDIP	8	1.2
	CerDIP	15	1.1

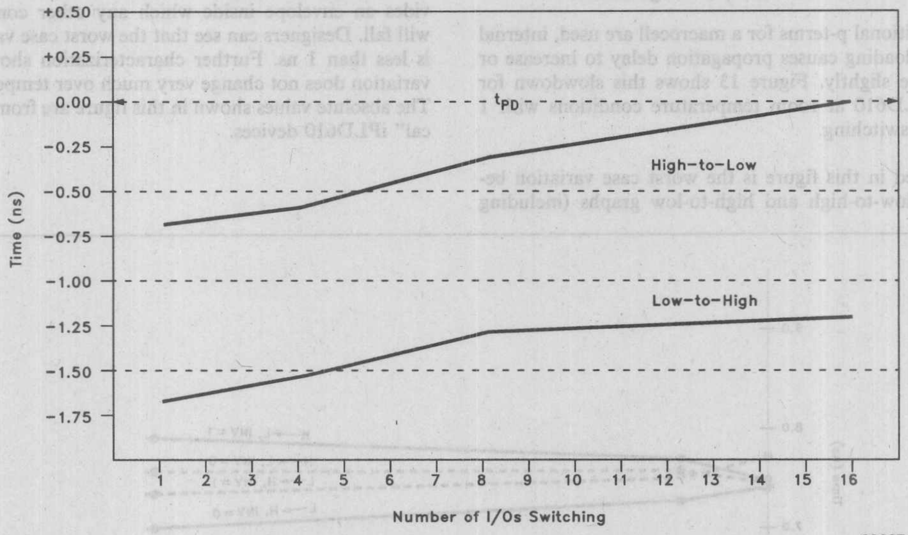
V_{CC} = 5.0V
Temp. = 25°C

Combinational Logic Performance (t_{PD})

This section shows how propagation delay for the iPLD610 is affected by factors that vary from one application to another. Note typical parts have propagation delays 1–2 ns below the value specified in the data sheet. Data such as this can aid designers required to "fine tune" their designs and/or provide worst-case timing analyses.

t_{PD} vs Number of Outputs Switching

As the number of device outputs switching simultaneously increases, average propagation delay through devices also increases. This increase is related to package power and ground leads to channel the additional current. Figure 11 shows the relation of t_{PD} to the number of outputs switching. Note, this data reflects worst case conditions (high temperature, low V_{CC}) and all outputs have loads as specified in the iPLD610 data sheet.

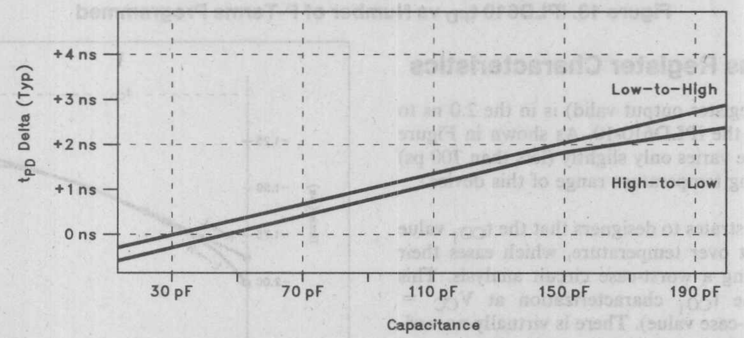


Conditions:
$T_A = 70°C$
$V_{CC} = 4.75V$
$C_L = 30$ pF

Figure 11. iPLD610 t_{PD} vs Number of Outputs Switching

t_{PD} vs C_L

Knowledge of how devices behave as capacitive loading is increased is an important consideration when designing high-speed systems. Figure 12 shows derating from specified values for a typical iPLD610 at high temperature, low V_{CC} conditions for both low-to-high and high-to-low transitions as capacitance increases.



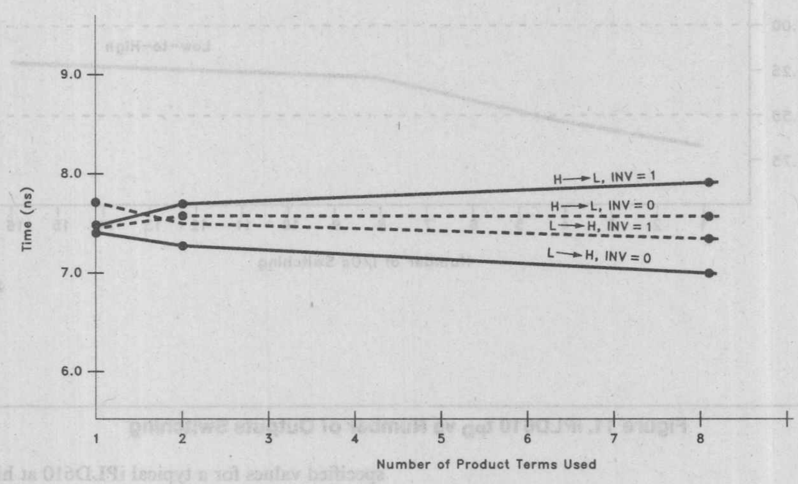
Conditions:
$T_A = 70°C$
$V_{CC} = 4.75V$

Figure 12. iPLD610 t_{PD} vs C_L

t_{PD} vs Number of P-Terms Programmed

As additional p-terms for a macrocell are used, internal device loading causes propagation delay to increase or decrease slightly. Figure 13 shows this slowdown for the iPLD610 at room temperature conditions with 1 output switching.

Provided in this figure is the worst case variation between low-to-high and high-to-low graphs (including variation due to logic inversion (ON or OFF). This provides an envelope inside which any other conditions will fall. Designers can see that the worst case variation is less than 1 ns. Further characterization shows this variation does not change very much over temperature. The absolute values shown in this figure are from "typical" iPLD610 devices.



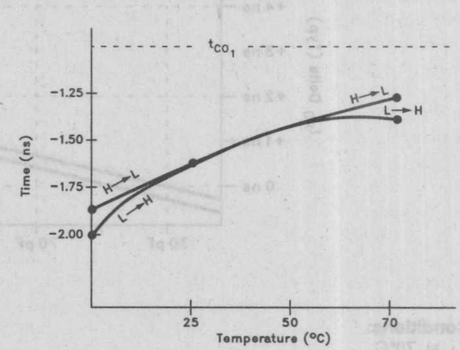
Temp. = 25°C
V_{CC} = 5.0V
C_L = 30 pF
1 Output Switching

Figure 13. iPLD610 t_{PD} vs Number of P-Terms Programmed

Synchronous Register Characteristics

t_{CO_1} (clock to register output valid) is in the 2.0 ns to 7.0 ns range for the iPLD610-10. As shown in Figure 14 the t_{CO_1} value varies only slightly (less than 700 ps) over the operating temperature range of this device.

This data demonstrates to designers that the t_{CO_1} value is fairly constant over temperature, which eases their task in performing a worst-case circuit analysis. This figure shows the t_{CO_1} characterization at V_{CC} = 4.75V (the worst-case value). There is virtually no variation in H → L characterization with V_{CC} varied from 4.75V to 5.25V. There is a small variation (less than 0.5 ns) in the L → H transition due to V_{CC} changes. The result is a t_{CO_1} value that does not change much over temperature and V_{CC}.



V_{CC} = 4.75V
1 Output Switching
Spec. Load

Figure 14. t_{CO_1} vs Temperature

Register-to-Register Skew

When registers within the same programmable logic device are clocked (using the synchronous clock input), ideally all outputs would change state simultaneously. This does not reflect the reality of differences in internal clock routing and ground path differences. Thus, there is some skew between outputs. As long as this skew remains small there is no impact on system design. Large skews can cause a need for additional synchronization logic and re-evaluation of system timing constraints.

Due to its high-speed double metal process, the output skew on the iPLD610 is very tight. Typical skew between fastest and slowest register within one "bank" (i.e., clocked by the same clock pin) is shown in Table 7.

Table 7. iPLD610 Register-to-Register Skew Characterization

0°C		70°C	
High to Low (ps)	Low to High (ps)	High to Low (ps)	Low to High (ps)
120	310	120	340

ASYNCHRONOUS REGISTER OPERATION CHARACTERISTICS

In addition to combinational logic and synchronous registered logic, the iPLD610 can implement asynchronously-clocked registered logic. This means a product (AND) term can be used to control the register in any macrocell. Each macrocell has a separate product term which can be used for this purpose. Also, as discussed in Section 3 there are a separate set of A.C. specifications for asynchronous register operation. Two of the key specifications are the asynchronous clock-to-output delay (t_{ACO_1}) and the asynchronous register setup time (t_{ASU}).

t_{ACO_1} Characteristics

Knowing how this specification varies over supply voltage (V_{CC}) and temperature may be useful to a designer concerned with detailed system timing analysis. Figure 15 shows this t_{ACO_1} characterization (H → L transition only) and how small the changes are over both of these variables. This figure shows t_{CO_1} will increase if V_{CC} is decreased or if system temperature increases, although temperature has a much greater impact on its value. The total variation over both of these parameters is fairly small (less than 2 ns) showing the solid design of the asynchronous circuitry of the iPLD610.

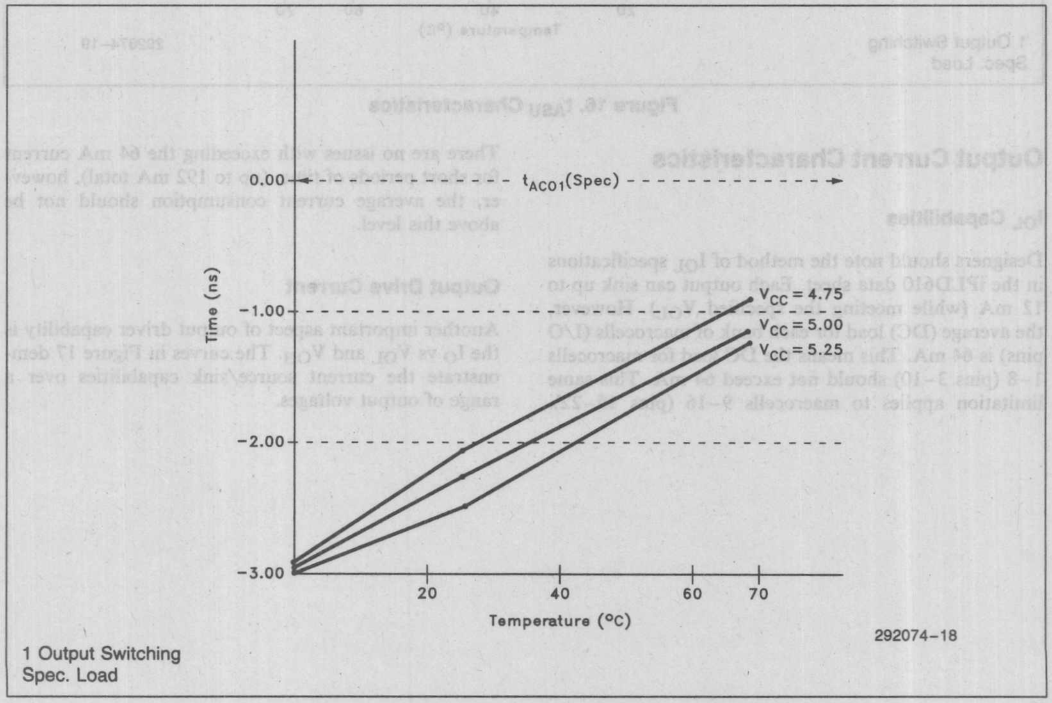


Figure 15. iPLD610 t_{ACO_1} Characteristics (H → L)

t_{ASU} Characteristics

Another important specification related to asynchronous register operation is t_{ASU}, the register setup time. A designer performing circuit analysis may need to know how this may vary over temperature and supply voltage. Figure 16 presents the characterization of this specification. Of note are the very small changes over both temperature (less than 50 ps over 0°C–70°C range) and supply voltage (less than 350 ps variation over a 4.75V–5.25V range). Both of these show the exceptional stability of this circuitry.

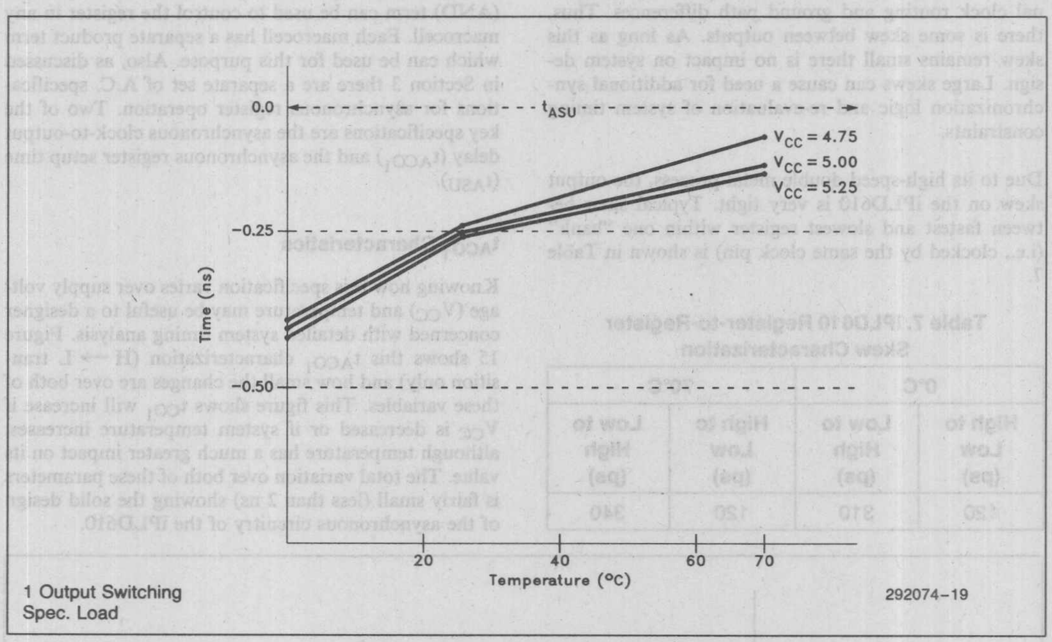


Figure 16. t_{ASU} Characteristics

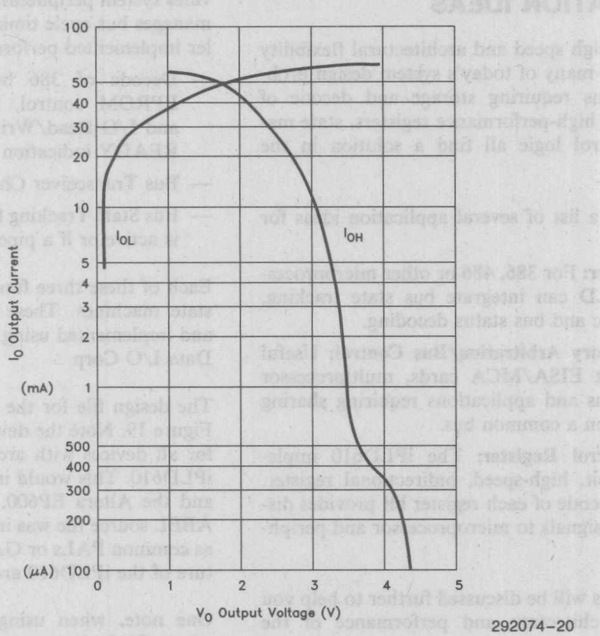
Output Current Characteristics

I_{OL} Capabilities

Designers should note the method of I_{OL} specifications in the iPLD610 data sheet. Each output can sink up to 12 mA (while meeting the specified V_{OL}). However, the average (DC) load for each bank of macrocells (I/O pins) is 64 mA. This means the DC load for macrocells 1–8 (pins 3–10) should not exceed 64 mA. This same limitation applies to macrocells 9–16 (pins 15–22). There are no issues with exceeding the 64 mA current for short periods of time, (up to 192 mA total), however, the average current consumption should not be above this level.

Output Drive Current

Another important aspect of output driver capability is the I_O vs V_{OL} and V_{OH}. The curves in Figure 17 demonstrate the current source/sink capabilities over a range of output voltages.



292074–20

Conditions:
$T_A = +80°C$
$V_{CC} = 4.75V$

Figure 17. iPLD610 Output Drive Current

Other Design Considerations

High-performance CMOS devices such as the iPLD610 are capable of driving large loads at fast edge rates. This capability means that noise control must be an important consideration during system design. Multilayer PC boards utilizing ground and power planes provide low resistance and low inductance connections between the power sources and devices.

System noise control also requires good decoupling capacitance. Boards with power and ground planes but no decoupling capacitors can still have noise problems. High speed transients of devices may demand up to 500 mA of current, which can result in a volt or more of switching noise on the local supply lines. Decoupling capacitors can help prevent this performance degradation by providing a local power source during output transitions. With the addition of decoupling capacitors, it is possible to reduce the local supply noise to 200 mV or less.

Capacitor selection is important for this application since the frequencies involved in high-speed systems can exceed 100 MHz. High-frequency capacitors are called for. The capacitors should provide low series inductance; leadless chip caps are the best choice, with short leaded capacitors as a more available second choice. The equivalent circuit for a capacitor is a series resonant circuit. If the inductive element in the capacitor is too high, the capacitor will appear inductive at high frequencies.

Assuming that everything possible has been done to manage noise on the supply lines outside the device, internal noise can still be a problem. The internal noise generated during switching transients is caused by output buffer design, package design, and output loading. Some suggestions for reducing noise are as follows:

- Select a low-inductance package such as PLCC.
- Reduce the output loading.
- Reduce the number of simultaneously switching outputs.
- Limit the voltage swing to 0V–3V by correctly terminating outputs with resistors to ground.

Designing high-speed P.C. boards requires closer attention to design issues that are not as important for slower systems. These elements include:

- Termination of transmission lines.
- Clock signal routing.
- Power distribution and heat dissipation.

5.0 APPLICATION IDEAS

The iPLD610's high speed and architectural flexibility can be applied to many of today's system design problems. Applications requiring storage and decode of more than 8 bits, high-performance registers, state machines, and control logic all find a solution in the iPLD610.

The following is a list of several application ideas for the iPLD610:

(a) **Bus Controller:** For 386, 486 or other microprocessors. The PLD can integrate bus state tracking, READY logic and bus status decoding.

(b) **Shared Memory Arbitration/Bus Control:** Useful for intelligent EISA/MCA cards, multiprocessor system designs and applications requiring sharing of resources on a common bus.

(c) **Custom Control Register:** The iPLD610 implements an 8-bit, high-speed, bidirectional register. Additional decode of each register bit provides discrete control signals to microprocessor and peripheral devices.

These applications will be discussed further to help you fully use the architecture and performance of the iPLD610.

5.1 80386DX Bus Controller

In every 80386DX microprocessor system, bus control logic must be implemented to provide an interface to system peripherals, I/O devices, and system memory. The bus controller requirements can vary in complexity depending on system performance, memory hierarchy, and other factors. Figure 18 shows an example of an 80386 subsystem with an iPLD610 bus controller. The bus controller decodes processor status signals, promanages bus cycle timing. In this case the bus controller implemented performs the following functions:

— Decode of 386 bus status signals to generate EPROM control, Interrupt Acknowledge cycles and I/O Read/Write signals. In addition, the I/O READY indication is generated.

— Bus Transceiver Control (OE Control)

— Bus State Tracking functions to determine if the bus is active or if a pipelined bus cycle is occurring.

Each of these three functions represent interdependent state machines. These state machines were designed and implemented using the ABEL logic compiler from Data I/O Corp.

The design file for the 386 bus controller is shown in Figure 19. Note the device name used "E0600" is valid for all devices with architectures compatible with the iPLD610. This would include the Intel 85C060, 5C060 and the Altera EP600, 610, 630, among others. This ABEL source file was implemented in the same fashion as common PALs or GALs, although the extended feature of the iPLD610 are available to the designer.

One note, when using test vectors with an ABEL source file be sure to toggle the proper clock or clocks. The iPLD610 has two synchronous clock inputs and when in doubt, toggle both. Another ABEL feature which is relevant to the iPLD610 is the "ISTYPE" statement. This can be used by the designer if specific register types, feedback or invert options are required for any iPLD610 implementation. Upon successful compilation of this source file by ABEL, a .DOC file (see Figure 20) was generated (along with the required JEDEC file) which shows the reduced equations and device pin-out. This bus state tracker will work for 80386DX designs up to 33 MHz (CLK2 = 66 MHz) due to the iPLD610's state machine frequency specification (F_{CNT_1}) of 66 MHz.

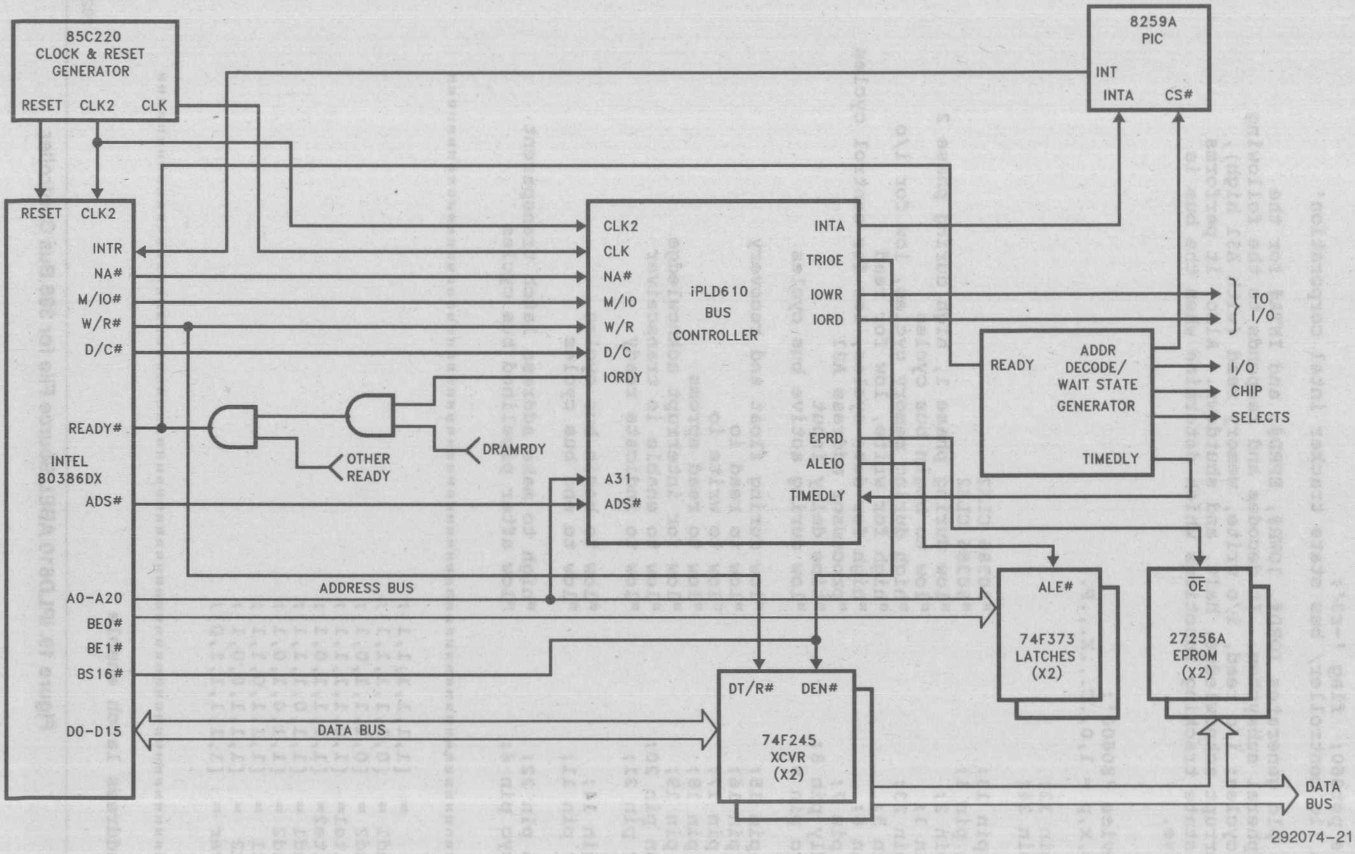


Figure 18. Typical 80386DX Microprocessor Subsystem

```
module pst060;  flag '-r3';
title 'io controller/ bus state tracker intel corporation'

"This pld generates IORD#, IOWR#, EPRD#, and INTA# for the
"peripheral subsystem.  It decodes and responds to the following
"bus cycles: i/o read, i/o write, memory read (with A31 high),
"interrupt acknowledge, halt, and shutdown.  Also, it performs
"bus state tracking functions which determine when the bus is
"active.


U1 device 'E0600';
h,l,c,x,p = 1,0,.C.,.X.,.P.;

gnd pin 12;
vcc pin 24;

clk2 pin 13;               "80386 CLK2
clk2a pin 1;               "80386 CLK2
clk pin 2;                 "low during phase 1, high during phase 2
na pin 3;                  "low to begin bus cycles
mio pin 23;                "high during memory cycles, low for i/o
wr pin 5;                  "high for write, low for read
dc pin 6;                  "high for data cycles, low for control cycles
pa31 pin 7;                "processor address A31
timedly pin 8;             "time delay input
buscyc pin 9;              "low during active bus cycles

recv pin 15;               "low during float and recovery
iord pin 16;               "low to read io
iowr pin 17;               "low to write io
eprd pin 18;               "low to read eproms
inta pin 19;               "low for interrupt acknowledge
trioen pin 20;             "low to enable io transceiver
iordy pin 21;              "low to indicate ready

ads pin 14;                "low to begin bus cycles
ready pin 11;              "low to end bus cycles

aleio pin 22;              "high to make address latch transparent
pipecyc pin 4;             "low after pipelined bus cycles


""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""


idle     =  [1,1,1,1,1,1];
ioread1 =  [0,1,1,1,1,1];
ioread2 =  [0,1,1,1,0,1];
iowrite1=  [1,0,1,1,1,1];
iowrite2=  [1,1,1,1,0,1];
epread1 =  [1,1,0,1,1,1];
epread2 =  [1,1,0,1,0,1];
intak1  =  [1,1,1,0,1,1];
intak2  =  [1,1,1,0,0,1];
recover =  [1,1,1,1,1,0];


""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""

"io address latch enable
```

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Figure 19. iPLD610 ABEL Source File for 386 Bus Controller

```
equations  !aleio :=     (!iord & clk) #
                         (!iowr & clk) #
                         (!inta & clk) #
                         (!aleio & !clk);

"io transceiver enable

state_diagram [trioen];
state 1:         "idle
        if (na & !buscyc & !mio & !pa31 & recv & clk) then 0
        else if (na & !buscyc & mio & pa31 & recv & clk) then 0
        else 1;

state 0:         "enable transceiver between processor and peripherals

        if (!iordy & clk) then 1
        else if (buscyc & clk) then 1
        else 0;
""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""

"io state machine

state_diagram [iord, iowr, eprd, inta, iordy, recv];
state idle:
  case  na & !buscyc & pa31 & !wr & clk: epreadl;
        na & !buscyc & !pa31 & !mio & dc & wr & clk: iowritel;
        na & !buscyc & !pa31 & !mio & dc & !wr & clk:ioreadl;
        na & !buscyc & !pa31 & !mio & !dc & !wr & clk: intakl;
        na & !buscyc & mio & !dc & wr & clk: iowrite2;  "halt
  endcase;

state epreadl:  if (!timedly & clk) then epread2 else epreadl;
state epread2:  if (clk) then idle else epread2;
state iowritel: if (!timedly & clk) then iowrite2 else iowritel;

state iowrite2: if (!mio & clk) then recover
                else if (mio & clk) then idle
                else iowrite2;
state ioreadl:  if (!timedly & clk) then ioread2 else ioreadl;
state ioread2:  if (clk) then recover else ioread2;
state intakl:   if (!timedly & clk) then intak2 else intakl;
state intak2:   if (clk) then recover else intak2;
state recover:  if (!timedly & clk) then idle else recover;
""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""

"bus cycle tracking

state_diagram [buscyc, pipecyc]
state[1,1]:      "idle
        if (!ads & clk) then [0,1]
        else [1,1];

state [0,1]:     "active
        if (!ready & ads & clk) then [1,1]
        else if (!ready & !ads & clk) then [1,0]
        else [0,1];
```

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Figure 19. iPLD610 ABEL Source File for 386 Bus Controller (Continued)

```
state [1,0]:    "pipelined
       if(clk) then [0,1]
       else [1,0];

state [0,0]:    "illegal
       goto [1,1];


""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""
test_vectors ([clk2,clk2a,clk,na,mio,wr,dc,pa31,timedly,buscyc] ->
             [iord,iowr,eprd,inta,iordy,recv]);

[c,c,h,h,h,h,h,h,h,h] -> [h,h,h,h,h,h];          "idle
[c,c,h,h,h,h,h,h,h,h]  ->  [h,h,h,h,h,h];        "idle
[c,c,h,h,h,h,h,h,h,h]  ->  [h,h,h,h,h,h];        "idle

[c,c,h,x,x,x,x,x,x,l]  ->  [h,h,h,h,h,h];        "preload buscyc
[c,c,h,h,h,l,l,h,h,l]  ->  [h,h,l,h,h,h];        "eprom read
[c,c,h,h,h,l,l,h,h,l] ->  [h,h,l,h,h,h];         "eprom read
[c,c,h,h,h,l,l,h,h,l]  ->  [h,h,l,h,h,h];        "eprom read
[c,c,h,h,h,l,l,h,h,l]  ->  [h,h,l,h,h,h];        "eprom read
[c,c,h,h,h,l,l,h,l,l]  ->  [h,h,l,h,l,h];        "eprom read
[c,c,h,h,h,h,h,h,h,h]  ->  [h,h,h,h,h,h];        "idle

[c,c,h,h,l,l,h,l,h,l]  ->  [l,h,h,h,h,h];        "io read
[c,c,h,h,l,l,h,l,h,l]  ->  [l,h,h,h,h,h];        "io read
[c,c,h,h,l,l,h,l,h,l] ->  [l,h,h,h,h,h];         "io read
[c,c,h,h,l,l,h,l,h,l] ->  [l,h,h,h,h,h];         "io read
[c,c,h,h,l,l,h,l,l,l] ->  [l,h,h,h,l,h];         "io read
[c,c,h,h,h,h,h,h,h,h]  ->  [h,h,h,h,h,l];        "recovery
[c,c,h,h,h,h,h,h,h,h]  ->  [h,h,h,h,h,l];        "recovery
[c,c,h,h,h,h,h,h,l,h] ->  [h,h,h,h,h,h];         "idle

[c,c,h,h,l,h,h,l,h,l] ->  [h,l,h,h,h,h];         "io write
[c,c,h,h,l,h,h,l,h,l]  ->  [h,l,h,h,h,h];        "io write
[c,c,h,h,l,h,h,l,h,l]  ->  [h,l,h,h,h,h];        "io write
[c,c,h,h,l,h,h,l,h,l]  ->  [h,l,h,h,h,h];        "io write
[c,c,h,h,l,h,h,l,l,l]  ->  [h,h,h,h,l,h];        "io write
[c,c,h,h,l,h,h,h,h,h] ->  [h,h,h,h,h,l];         "recovery
[c,c,h,h,h,h,h,h,h,h]  ->  [h,h,h,h,h,l];        "recovery
[c,c,h,h,h,h,h,h,l,h] ->  [h,h,h,h,h,h];         "idle

[c,c,h,h,l,l,l,l,h,l] ->  [h,h,h,l,h,h];         "interrupt ack
[c,c,h,h,l,l,l,l,h,l]  ->  [h,h,h,l,h,h];        "interrupt ack
[c,c,h,h,l,l,l,l,h,l] ->  [h,h,h,l,h,h];         "interrupt ack
[c,c,h,h,l,l,l,l,h,l]  ->  [h,h,h,l,h,h];        "interrupt ack
[c,c,h,h,l,l,l,l,l,l]  ->  [h,h,h,l,l,h];        "interrupt ack
[c,c,h,h,h,h,h,h,h,h]  ->  [h,h,h,h,h,l];        "recovery
[c,c,h,h,h,h,h,h,h,h]  ->  [h,h,h,h,h,l];        "recovery
[c,c,h,h,h,h,h,h,l,h]  ->  [h,h,h,h,h,h];        "idle

[c,c,h,h,h,h,l,l,h,l]  ->  [h,h,h,h,l,h];        "halt or shutdown

[c,c,h,h,h,h,h,h,h,h]  ->  [h,h,h,h,h,h];        "idle
[c,c,h,h,h,h,h,h,h,h]  ->  [h,h,h,h,h,h];        "idle
""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""

test_vectors ([clk2a, clk, ads, ready]  ->  [buscyc, pipecyc])
```

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Figure 19. iPLD610 ABEL Source File for 386 Bus Controller (Continued)

```
        [p,h,l,l]  ->  [x,x];
        [c,l,h,h]  ->  [x,h];                "idle-busy-idle
        [c,h,h,l]  ->  [h,h];
        [c,l,h,h]  ->  [h,h];
        [c,h,l,h]  ->  [l,h];
        [c,l,h,l]  ->  [l,h];
        [c,h,h,l]  ->  [h,h];

        [c,l,l,h]  ->  [h,h];                "idle-busy-pipe-busy
        [c,h,l,h]  ->  [l,h];
        [c,l,h,l]  ->  [l,h];
        [c,h,l,l]  ->  [h,l];
        [c,l,l,h]  ->  [h,l];
        [c,h,h,h]  ->  [l,h];

        [c,h,h,l]  ->  [h,h];                "idle-busy-busy-idle
        [c,l,h,h]  ->  [h,h];
        [c,h,l,h]  ->  [l,h];
        [c,l,l,h]  ->  [l,h];
        [c,h,h,h]  ->  [l,h];
        [c,l,h,h]  ->  [l,h];
        [c,h,h,h]  ->  [l,h];
        [c,l,h,c]  ->  [l,h];
        [c,h,h,l]  ->  [h,h];
        [c,l,h,h]  ->  [h,h];

end pst060;
```

292074-35

Figure 19. iPLD610 ABEL Source File for 386 Bus Controller (Continued)

3

```
                                                          Page 1
ABEL(tm) 3.20A  -  Document Generator          17-Jul-90 06:26 PM
io controller/ bus state tracker intel corporation
Equations for Module pst060

Device U1

- Reduced Equations for device U1:

    !aleio := (!clk & !aleio # clk & !inta # clk & !iowr # clk & !iord);

    !trioen := (!clk & !trioen
                # !buscyc & !trioen & iordy
                # clk & na & mio & pa31 & !buscyc & recv & trioen
                # clk & na & !mio & !pa31 & !buscyc & recv & trioen);


    !iord := (!clk & recv & !iord & iowr & eprd & inta
               # recv & !iord & iowr & eprd & inta & iordy
               # clk & na & !mio & !wr & dc & !pa31 & !buscyc & recv & iowr &
             eprd & inta & iordy);

    !iowr := (!clk & recv & iord & !iowr & eprd & inta & iordy
               # timedly & recv & iord & !iowr & eprd & inta & iordy
               # clk & na & !mio & wr & dc & !pa31 & !buscyc & recv & iord &
             iowr & eprd & inta & iordy);

    !eprd := (!clk & recv & iord & iowr & !eprd & inta
               # recv & iord & iowr & !eprd & inta & iordy
               # clk & na & !wr & pa31 & !buscyc & recv & iord & iowr & inta
             & iordy);

    !inta := (!clk & recv & iord & iowr & eprd & !inta
               # recv & iord & iowr & eprd & !inta & iordy
               # clk & na & !mio & !wr & !dc & !pa31 & !buscyc & recv & iord
             & iowr & eprd & iordy);

    !iordy := (!clk & recv & iord & iowr & eprd & !iordy
                # clk & !timedly & recv & iord & iowr & eprd & !inta & iordy

                # !clk & recv & iowr & eprd & inta & !iordy
                # clk & !timedly & recv & !iord & iowr & eprd & inta & iordy

                # clk & !timedly & recv & iord & !iowr & eprd & inta & iordy

                # !clk & recv & iord & iowr & inta & !iordy
                # clk & !timedly & recv & iord & iowr & !eprd & inta & iordy

                # clk & na & mio & wr & !dc & !buscyc & recv & iord & iowr &
              eprd & inta & iordy);

    !recv := (!clk & !recv & iord & iowr & eprd & inta & iordy
              # timedly & !recv & iord & iowr & eprd & inta & iordy
              # clk & recv & iord & iowr & eprd & !inta & !iordy
              # clk & recv & !iord & iowr & eprd & inta & !iordy
              # clk & !mio & recv & iowr & eprd & inta & !iordy);
```

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Figure 20. 386-PST .DOC File

```
Device U1

!buscyc := (clk & buscyc & !pipecyc
          # !clk & !buscyc & pipecyc
          # !buscyc & ready & pipecyc
          # clk & buscyc & !ads);

!pipecyc := (!clk & buscyc & !pipecyc
          # clk & !buscyc & !ads & !ready & pipecyc);
```

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```
                 E0600
          ----------\     /----------
    clk2a | 1        \___/       24 | vcc
      clk | 2                    23 | mio
       na | 3                    22 | aleio
  pipecyc | 4                    21 | iordy
       wr | 5                    20 | trioen
       dc | 6                    19 | inta
     pa31 | 7                    18 | eprd
  timedly | 8                    17 | iowr
   buscyc | 9                    16 | iord
          | 10                   15 | recv
    ready | 11                   14 | ads
      gnd | 12                   13 | clk2
          ---------------------------
```

292074–22

Figure 20. 386-PST .DOC File (Continued)

3

5.2 Shared Memory Arbitration/Bus Control

Sharing resources (usually memory) on a common bus is becoming more and more common in today's system designs. Not only are many systems, including personal computers, being implemented as multiprocessors, but peripheral controllers are becoming more intelligent and capable of controlling the bus by themselves. Thus, arbitration logic is required to determine which processor/controller currently has control of each shared resource. In addition, the designer may want to incorporate a variety of associated functions including:

- READY Logic (Bus Cycle Control)
- Address Pipelining Support
- Memory Burst Control
- Wait-State Generation
- I/O Chip Select Logic
- Bus Throttling Logic
- DRAM Control/Refresh Logic (if used instead of SRAM)
- EPROM Control Logic (if microprocessor code is not in SRAM)

The example to be discussed here is an intelligent EISA communications add-in card (see Figure 21). The arbitration logic must decide if the communications controller, on-board microprocessor or EISA bus controller has access to the on-board static RAM (SRAM). The on-board SRAM mainly acts as a high-speed data buffer for the communications controller to off-load the EISA bus by providing block size transfers. The on-board microprocessor initializes the EISA control logic and communications controller and provides handling of local interrupts/error conditions. A block diagram of the system and required logic are provided by Figures 21 and 22, respectively. The "communications controller" may be implementing an ISDN, high-speed serial, Ethernet, FDDI or other communications link. Often these devices can themselves control the local bus and provide DMA capabilities to move data to and from memory. Also, many of these controllers have on-board data FIFOs that may necessitate a need for bursting data to/from the local memory.

Each of the three bus control-capable devices is assumed to have "Bus Request" and "Bus Grant" signals that are routed to the arbitration logic. The iPLD610 provides 8 product terms (in addition to separate OE and RESET product terms) in each macrocell, which allows for increased flexibility in choosing an arbitration scheme. Common schemes include fixed priority, rotating (or last granted, lowest priority), or First-Come, First-Serve. In this example a rotating priority is implemented to assure a balance of accesses between the devices, and to decrease the worst-case service time to help prevent data underflow/overflow. Figure 23 shows the state diagram of the 3-way bus arbitration logic. This method is easily expandible if more bus masters were present, as would be the case for DRAM Refresh requests and/or multiple communications controllers or in a multiprocessing system.

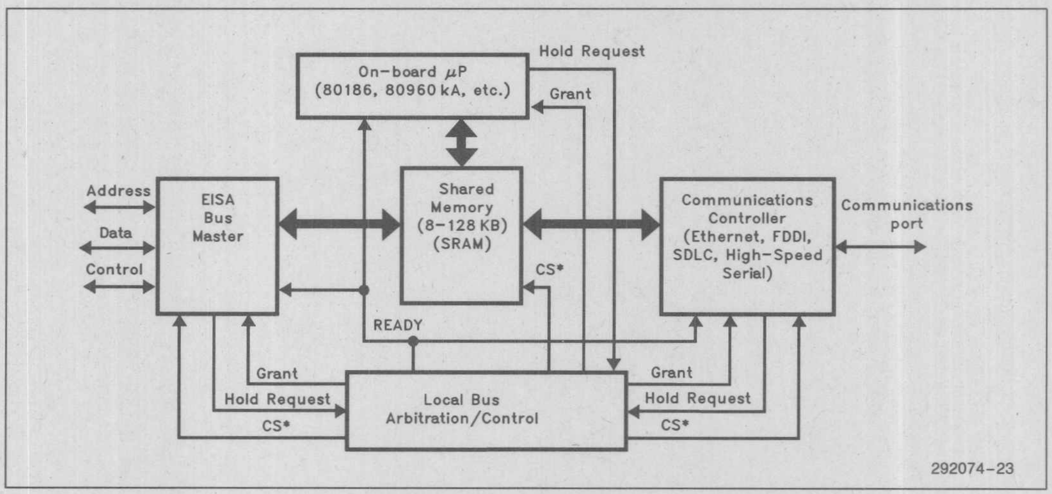

Figure 21. Intelligent EISA Communications Add-In Card

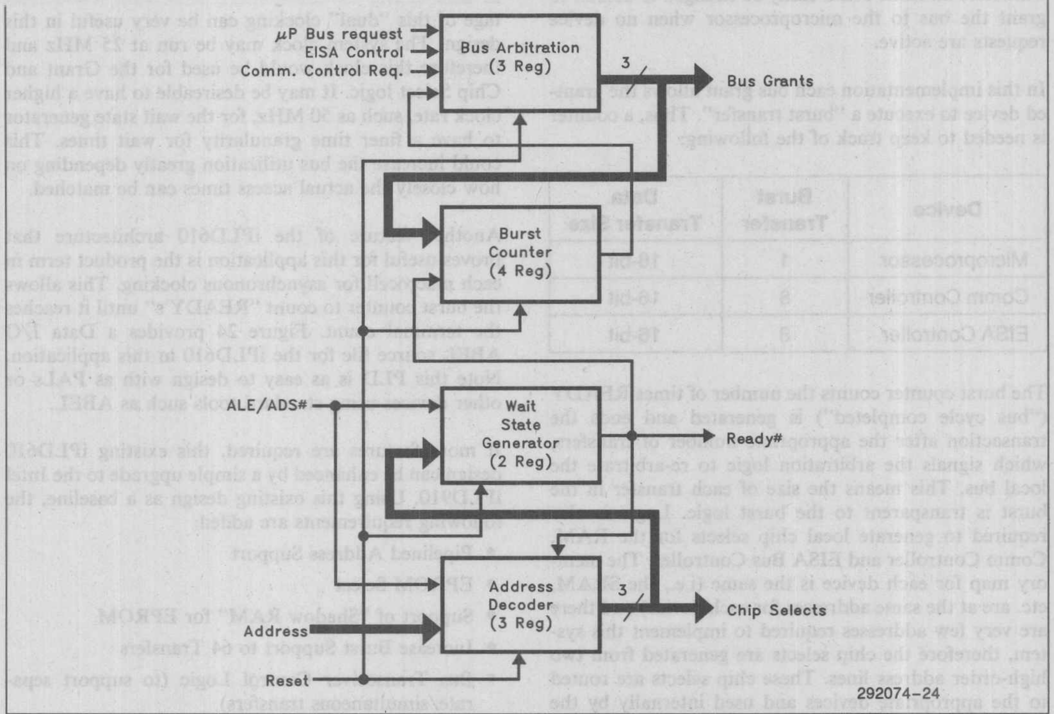

Figure 22. iPLD610 Shared Memory Arbitration/Bus Control Logic Implementation

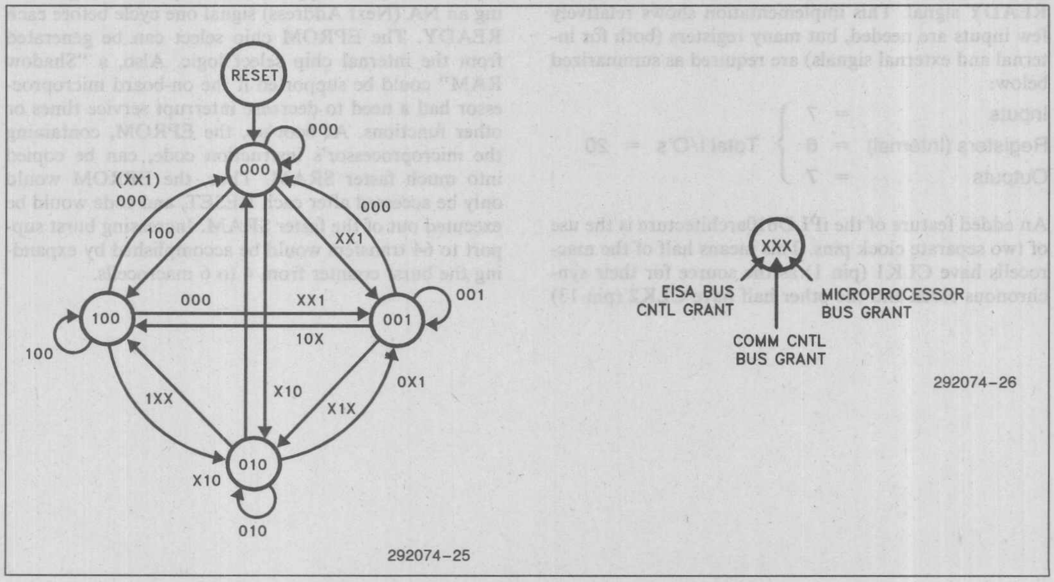

Figure 23. Bus Arbitration State Machine—Rotating Priority

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This state machine could easily be changed to default to grant the bus to the microprocessor when no device requests are active.

In this implementation each bus grant allows the granted device to execute a "burst transfer". Thus, a counter is needed to keep track of the following:

Device	Burst Transfer	Data Transfer Size
Microprocessor	1	16-bit
Comm Controller	8	16-bit
EISA Controller	8	16-bit

The burst counter counts the number of times READY ("bus cycle completed") is generated and ends the transaction after the appropriate number of transfers, which signals the arbitration logic to re-arbitrate the local bus. This means the size of each transfer in the burst is transparent to the burst logic. Logic is also required to generate local chip selects for the RAM, Comm Controller and EISA Bus Controller. The memory map for each device is the same (i.e., the SRAM, etc. are at the same addresses for each device) and there are very few addresses required to implement this system, therefore the chip selects are generated from two high-order address lines. These chip selects are routed to the appropriate devices and used internally by the wait-state generator, which counts the number of cycles programmed for each chip select before activating the READY signal. This implementation shows relatively few inputs are needed, but many registers (both for internal and external signals) are required as summarized below:

$$\left.\begin{array}{lcl} \text{Inputs} & = & 7 \\ \text{Registers (Internal)} & = & 6 \\ \text{Outputs} & = & 7 \end{array}\right\} \text{Total I/O's} = 20$$

An added feature of the iPLD610architecture is the use of two separate clock pins. This means half of the macrocells have CLK1 (pin 1) as the source for their synchronous clock and the other half have CLK2 (pin 13) as their source for the synchronous clock. The advantage of this "dual" clocking can be very useful in this design. The system clock may be run at 25 MHz and therefore this clock would be used for the Grant and Chip Select logic. It may be desireable to have a higher clock rate, such as 50 MHz, for the wait state generator to have a finer time granularity for wait times. This could increase the bus utilization greatly depending on how closely the actual access times can be matched.

Another feature of the iPLD610 architecture that proves useful for this application is the product term in each macrocell for asynchronous clocking. This allows the burst counter to count "READY's" until it reaches the terminal count. Figure 24 provides a Data I/O ABEL source file for the iPLD610 in this application. Note this PLD is as easy to design with as PALs or other devices using standard tools such as ABEL.

If more features are required, this existing iPLD610 design can be enhanced by a simple upgrade to the Intel iPLD910. Using this existing design as a baseline, the following requirements are added:

- Pipelined Address Support
- EPROM Select
- Support of "Shadow RAM" for EPROM
- Increase Burst Support to 64 Transfers
- Bus Transceiver Control Logic (to support separate/simultaneous transfers)

Pipelined address support is accomplished by generating an NA (Next Address) signal one cycle before each READY. The EPROM chip select can be generated from the internal chip select logic. Also, a "Shadow RAM" could be supported if the on-board microprocessor had a need to decrease interrupt service times or other functions. At boot-up, the EPROM, containing the microprocessor's instruction code, can be copied into much faster SRAM. Thus, the EPROM would only be accessed after each RESET, and code would be executed out of the faster SRAM. Increasing burst support to 64 transfers would be accomplished by expanding the burst counter from 4 to 6 macrocells.

```
module arb_cntl          flag '-UL', '-r3'
title 'Arbitration/Bus control logic
John Casey       Intel Corp.       July 1990'

"THIS IS A SAMPLE FILE ONLY.  THIS CIRCUIT PROVIDES A GENERAL SOLUTION !!!


arblogic          device   'E0600';


"inputs
clk1              pin 1;          "33 MHz clock input
clk2              pin 13;         "33 MHz clock input
procreq           pin 2;          "microprocessor local bus request
commreq           pin 23;         "comm controller local bus request
eisareq           pin 11;         "on-board eisa controller local bus req.
addr1             pin 14;         "address input - used for chip select dec.

addr2             pin 3;          "address input - used for chip select dec.
ale_              pin 5;          "ale (or ads/) - represents valid addr.
reset             pin 22;         "board reset - used to set initial state

"outputs
procgrant         pin 6;          "processor local bus grant
commgrant         pin 7;          "communications controller local bus grant
eisagrant         pin 8;          "on-board eisa controller local bus grant
ready_            pin 9;          "indicates end of current bus cycle
commcs            pin 10;         "comm controller chip select
eisacs            pin 15;         "local eisa bus controller chip select
sramcs            pin 21;         "sram chip select

"buried functions
burst0            pin 16;         "part of burst counter logic
burst1            pin 17;         "part of burst counter logic
burst2            pin 18;         "part of burst counter logic
burstdone         pin 19;         "active at end of current burst count
wait0             pin 20;         "lower bit of wait state count logic,
                                  "ready represents output of this logic
wait1             pin 4;          "upper bit of wait state count logic

"macrocell control
burst0, burst1, burst2, burstdone          istype 'feed_reg';
wait0, wait1                               istype 'feed_reg';

"busarb valid states (for the bus arbitration state machine)
s0 = ^b000;               "no grant active
s1 = ^b001;               "microprocessor grant active
s2 = ^b010;               "comm controller grant active
s3 = ^b100;               "eisa bus controller grant active

"wait state generator valid states
ws0 = ^b000;    ws1 = ^b010;    ws2 = ^b100;    ws3 = ^b111;

"burst state machine
bs0 = ^b000;    bs4 = ^b100;
bs1 = ^b001;    bs5 = ^b101;
bs2 = ^b010;    bs6 = ^b110;
bs3 = ^b011;    bs7 = ^b111;
```

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Figure 24. Sample iPLD610 ABEL Source File

```
equations

commcs := !addr1 & !addr2;                      "address mapping will vary
commcs.clk = !ale_;                             "ale is async clock

eisacs := !addr1 & addr2;
eisacs.clk = !ale_;

sramcs := addr1 & !addr2;
sramcs.clk = !ale_;

burstdone = burst0 & burst1 & burst2;           "terminal count completed

burst0.clk = ready_;                "burst counter async clocked w/ ready
burst1.clk = ready_;
burst2.clk = ready_;

"Reset signal sets all registers low
procgrant.re = reset;   commgrant.re = reset;   eisagrant.re = reset;
commcs.re = reset;      eisacs.re = reset;      sramcs.re = reset;
burst0.re = reset;      burst1.re = reset;      burst2.re = reset;
wait0.re = reset;       wait1.re = reset;

 "busarb state machine uses a rotating (last grant, lowest priority) scheme
 "which allows bus accesses to be balanced.  If no request then returns to
 "state 000 which allows microprocessor to be #1 priority (this is due to
 "requirement to quickly service interrupts.

state_diagram [procgrant, commgrant, eisagrant]
State s0:  if (burstdone & procreq) then s1 else s0;
           if (burstdone & commreq & !procreq) then s2 else s0;
           if (burstdone & eisareq & !commreq & !procreq) then s3 else s0;

State s1:  if (burstdone & commreq) then s2 else s0;
           if (burstdone & eisareq & !commreq) then s3 else s0;
           if (burstdone & procreq & !eisareq & !commreq) then s1 else s0;

State s2:  if (burstdone & eisareq) then s3 else s0;
           if (burstdone & procreq & !eisareq) then s1 else s0;
           if (burstdone & commreq & !procreq & !eisareq) then s3 else s0;

State s3:  if (burstdone & procreq) then s1 else s0;
           if (burstdone & commreq & !procreq) then s2 else s0;
           if (burstdone & eisareq & !commreq & !procreq) then s3 else s0;


"This wait state generator can support accesses up to 4 clocks long.
"The EISA controller and the comm controller each take 4 cycles (2 wait
"states) and the SRAM takes two cycles (zero wait states).

state_diagram [wait0, wait1, ready_]

State ws0:      if (sramcs) then ws3 else ws0;
                if (commcs # eisacs) then ws1 else ws0;

State ws1:      goto ws2;
```

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Figure 24. Sample iPLD610 ABEL Source File (Continued)

```
State ws2:         goto ws3;
State ws3:         goto ws0;

"the burst logic state machine has a programmed burst length for each bus
"grant.  These are 8 transfers for the comm controller (fifo) and EISA bus
"controller and one transfer for the microprocessor.  When terminal count
"is reached BURSTDONE will go active, indicating to the bus arbitration logic
"that it should re-arbitrate the bus.  At each state the bus grant is checked
"to make sure it is still active (i.e. that a full FIFO transfer is necessary).

state_diagram [burst0, burst1, burst2]
state bs0:  if (procgrant) then bs7 else bs0;
            if (commgrant # eisagrant) then bs1 else bs0;

state bs1: if (!commgrant & !eisagrant) then bs7 else bs2;

state bs2: if (!commgrant & !eisagrant) then bs7 else bs3;

state bs3: if (!commgrant & !eisagrant) then bs7 else bs4;

state bs4: if (!commgrant & !eisagrant) then bs7 else bs5;

state bs5: if (!commgrant & !eisagrant) then bs7 else bs6;

state bs6: goto bs7;

state bs7: goto bs0;


"       test_vectors
"            .
"            .
"            .

end arb_cntl;
```

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Figure 24. Sample iPLD610 ABEL Source File (Continued)

5.3 High-Speed Custom Control/ Status Register

In many applications there exists a need for a high-speed dedicated control and/or status register. In multiprocessing systems there may be a need for a system control register; in a communications controller there may be a requirement for a system configuration control register. Figure 25 shows this general application idea. There is a frequent requirement in system add-on card and adapter designs for a Read/Write register that also provides discrete status inputs and control outputs.

The destinations of these discrete signals can include a wide variety of functions that need to be under software control. The functions provided by this register can include enable signals, transceiver/mux control and it can also include status indications such as a communications error. The design, configuration and purpose of each bit of this register is individually selectable, which leads into a wide variety of applications.

The iPLD610 is useful in this application due to these key architectural features:

— 16 macrocells (8 for data bus, 8 for control outputs/ inputs)

— separate product term for RESET (to set known power up state)

— four dedicated inputs (necessary for register control)

— pin/register feedback capabilities and OE control (allows specialized I/O capabilities to be implemented)

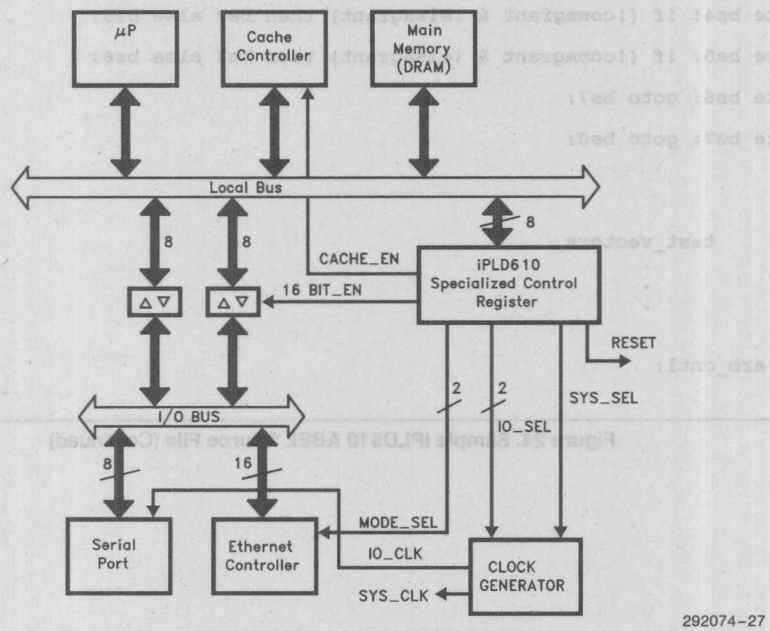

Figure 25. Typical System Requiring Specialized Register for Configuration Control

As shown in Figures 26 and 27, the iPLD610 uses these features to implement each bit of this control register. Not only is the architecture of the iPLD610 a perfect match for this application, but the performance level is so high (83.3 MHz register speed) that it can meet the zero-wait state requirements for most microprocessors. This provides very high-speed register access via Read-Modify-Write operations.

Some applications may benefit from the power-down mode of the iPLD610. If the register implemented is required only periodically, such as at power-on or after system resets, the power-down feature of the iPLD610 can be programmed to allow power consumption to be in the 20 μA (typical) range. Decreasing power consumption can have a positive impact on system reliability in addition to decreasing power supply and cooling requirements.

A sample design file is included in Figure 28. This demonstrates the ease of using the advanced architectural capabilities of the iPLD610. This design file is written in the Intel ADF (Advanced Design File) format and is compiled by the iPLS II Development Tools. Since the creation of this example, Intel has updated its tools support. Intel's newest tool, PLDshell Plus, is a free tool that supports Intel's entire PLD and FPGA product lines. (See the PLD Handbook or call the PLD hotline, 1 800-628-8686, for more information on Intel development tools.) Figure 27 provides details on the actual logic implementation of each of the eight register/control output cells. Each of these cells requires two macrocells of the iPLD610. One macrocell forms the register portion and provides the control signal and the other provides the data bus interface (with output enable controlled).

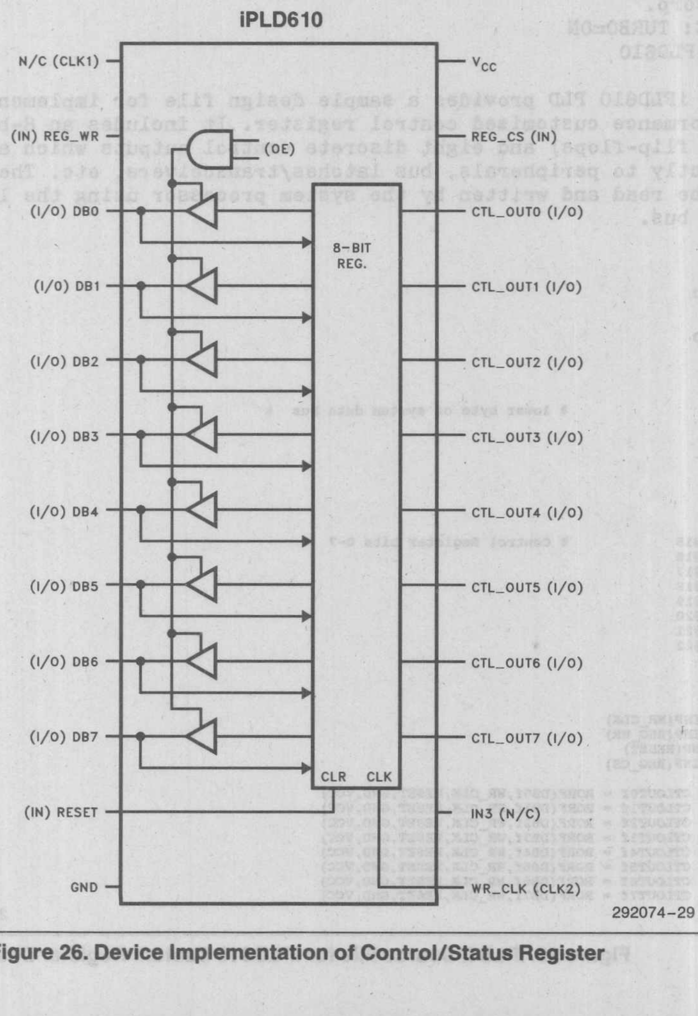

Figure 26. Device Implementation of Control/Status Register

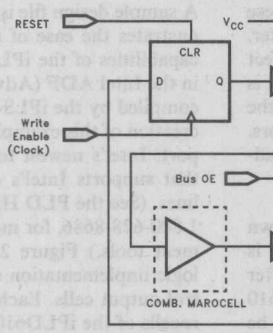

Figure 27. iPLD610 Control Register Implementation (1-Bit)

```
J. Casey
Intel Corp.
OPTIONS: TURBO=ON
PART: iPLD610

% This iPLD610 PLD provides a sample design file for implementing a high
  performance customized control register. It includes an 8-bit register (D-
  type flip-flops) and eight discrete control outputs which are routed
  directly to peripherals, bus latches/transceivers, etc. The 8-bit register
  can be read and written by the system processor using the lower byte of the
  data bus.

INPUTS:

WR_CLK @13
REG_WR @2
RESET @11
REG_CS @23

OUTPUTS:

DB0 @3                          % lower byte of system data bus  %
DB1 @4
DB2 @5
DB3 @6
DB4 @7
DB5 @8
DB6 @9
DB7 @10

CTL_OUT7 @15                    % Control Register bits 0-7  %
CTL_OUT6 @16
CTL_OUT5 @17
CTL_OUT4 @18
CTL_OUT3 @19
CTL_OUT2 @20
CTL_OUT1 @21
CTL_OUT0 @22

NETWORK:

WR_CLK = INP(WR_CLK)
REG_WR = INP(REG_WR)
RESET = INP(RESET)
REG_CS = INP(REG_CS)

CTL_OUT0, CTLOUT0f = RORF(DB0f,WR_CLK,RESET,GND,VCC)
CTL_OUT1, CTLOUT1f = RORF(DB1f,WR_CLK,RESET,GND,VCC)
CTL_OUT2, CTLOUT2f = RORF(DB2f,WR_CLK,RESET,GND,VCC)
CTL_OUT3, CTLOUT3f = RORF(DB3f,WR_CLK,RESET,GND,VCC)
CTL_OUT4, CTLOUT4f = RORF(DB4f,WR_CLK,RESET,GND,VCC)
CTL_OUT5, CTLOUT5f = RORF(DB5f,WR_CLK,RESET,GND,VCC)
CTL_OUT6, CTLOUT6f = RORF(DB6f,WR_CLK,RESET,GND,VCC)
CTL_OUT7, CTLOUT7f = RORF(DB7f,WR_CLK,RESET,GND,VCC)
```

292074-41

Figure 28. iPLS II Source File for iPLD610 Custom Register Design

```
DB1, DB1f = COIF(iDB1,REG_OE)
DB2, DB2f = COIF(iDB2,REG_OE)
DB3, DB3f = COIF(iDB3,REG_OE)
DB4, DB4f = COIF(iDB4,REG_OE)
DB5, DB5f = COIF(iDB5,REG_OE)
DB6, DB6f = COIF(iDB6,REG_OE)
DB7, DB7f = COIF(iDB7,REG_OE)


EQUATIONS:

iDB0 = CTLOUT0f;
iDB1 = CTLOUT1f;
iDB2 = CTLOUT2f;
iDB3 = CTLOUT3f;
iDB4 = CTLOUT4f;
iDB5 = CTLOUT5f;
iDB6 = CTLOUT6f;
iDB7 = CTLOUT7f;

REG_OE = REG_CS * !REG_WR;

END$
```

292074-42

Figure 28. iPLS II Source File for iPLD610 Custom Register Design (Continued)

A .RPT (Report) file was generated by the Intel iPLS logic compiler. A JEDEC for the iPLD610 was also generated by the software. This .RPT file, included in Figure 29, shows the macrocell/p-term usage and device pin-out as the device was implemented.

This application demonstrates the effective combination of architecture and performance provided by the Intel iPLD610 μPLD. In essence, the performance increase over existing devices with identical architecture has opened more doors for additional uses. It is now clear how this device can be used in high-speed applications—even when closely coupled to the microprocessor.

```
INTEL Logic Optimizing Compiler Utilization Report          a:CONTROL.rpt
IPLS II FIT Version 2.2 Beta3 Level 4.0i 9/7/88

***** Design implemented successfully

J. Casey
Intel Corp.
OPTIONS:  TURBO=ON

                         iPLD610
                     _ _ _ _ _
              Gnd -| 1        24|- Vcc
           REG_WR -| 2        23|- REG_CS
              DB0 -| 3        22|- CTL_OUT0
              DB1 -| 4        21|- CTL_OUT1
              DB2 -| 5        20|- CTL_OUT2
              DB3 -| 6        19|- CTL_OUT3
              DB4 -| 7        18|- CTL_OUT4
              DB5 -| 8        17|- CTL_OUT5
              DB6 -| 9        16|- CTL_OUT6
              DB7 -| 10       15|- CTL_OUT7
            RESET -| 11       14|- Gnd
              Gnd -| 12       13|- WR_CLK
                     _ _ _ _ _
```

292074-30

Figure 29. iPLS II Report File For The iPLD610 Custom Register Design

```
**OUTPUTS**

      Name         Pin        Resource       MCell      PTerms   | Sync Clock

       DB0           3          COIF            9         1/ 8   |      -
       DB1           4          COIF           10         1/ 8   |      -
       DB2           5          COIF           11         1/ 8   |      -
       DB3           6          COIF           12         1/ 8   |      -
       DB4           7          COIF           13         1/ 8   |      -
       DB5           8          COIF           14         1/ 8   |      -
       DB6           9          COIF           15         1/ 8   |      -
       DB7          10          COIF           16         1/ 8   |      -
  CTL_OUT7          15          RORF            8         1/ 8   |   WR_CLK
  CTL_OUT6          16          RORF            7         1/ 8   |   WR_CLK
  CTL_OUT5          17          RORF            6         1/ 8   |   WR_CLK
  CTL_OUT4          18          RORF            5         1/ 8   |   WR_CLK
  CTL_OUT3          19          RORF            4         1/ 8   |   WR_CLK
  CTL_OUT2          20          RORF            3         1/ 8   |   WR_CLK
  CTL_OUT1          21          RORF            2         1/ 8   |   WR_CLK
  CTL_OUT0          22          RORF            1         1/ 8   |   WR_CLK

**INPUTS**

      Name         Pin        Resource       MCell      PTerms   | Sync Clock

    WR_CLK          13          CKR             -           -    |      -
    REG_WR           2          INP             -           -    |      -
     RESET          11          INP             -           -    |      -
    REG_CS          23          INP             -           -    |      -

**UNUSED RESOURCES**

      Name         Pin        Resource       MCell      PTerms

         -          14          INPUT           -           -

**PART UTILIZATION**

16/16             Macrocells (100%), 12% of used Pterms Filled
3/ 4              Input Pins (75%)
                  PTerms Used 12%
```

Figure 29. iPLS II Report File For The iPLD610 Custom Register Design (Continued)

```
Macrocell Interconnection Cross Reference

FEEDBACKS:                       M M M M M M M M   M M M M M M M M
                                 0 0 0 0 0 0 0 0   0 1 1 1 1 1 1 1
                                 1 2 3 4 5 6 7 8   9 0 1 2 3 4 5 6
CTL_OUT0 . RORF @M1 -> . . . . . . . .   * . . . . . . . @22
CTL_OUT1 . RORF @M2 -> . . . . . . . .   . * . . . . . . @21
CTL_OUT2 . RORF @M3 -> . . . . . . . .   . . * . . . . . @20
CTL_OUT3 . RORF @M4 -> . . . . . . . .   . . . * . . . . @19
CTL_OUT4 . RORF @M5 -> . . . . . . . .   . . . . * . . . @18
CTL_OUT5 . RORF @M6 -> . . . . . . . .   . . . . . * . . @17
CTL_OUT6 . RORF @M7 -> . . . . . . . .   . . . . . . * . @16
CTL_OUT7 . RORF @M8 -> . . . . . . . .   . . . . . . . * @15

DB0 ...... COIF @M9 -> * . . . . . . .   . . . . . . . . @3
DB1 ...... COIF @M10-> . * . . . . . .   . . . . . . . . @4
DB2 ...... COIF @M11-> . . * . . . . .   . . . . . . . . @5
DB3 ...... COIF @M12-> . . . * . . . .   . . . . . . . . @6
DB4 ...... COIF @M13-> . . . . * . . .   . . . . . . . . @7
DB5 ...... COIF @M14-> . . . . . * . .   . . . . . . . . @8
DB6 ...... COIF @M15-> . . . . . . * .   . . . . . . . . @9
DB7 ...... COIF @M16-> . . . . . . . *   . . . . . . . . @10

INPUTS:

REG_WR ... INP  @2  -> . . . . . . . .   * * * * * * * *
RESET .... INP  @11 -> * * * * * * * *   . . . . . . . .
WR_CLK ... CKR  @13 -> * * * * * * * *   . . . . . . . .
REG_CS ... INP  @23 -> . . . . . . . .   * * * * * * * *
                       C C C C C C C C   D D D D D D D D
                       T T T T T T T T   B B B B B B B B
                       L L L L L L L L   0 1 2 3 4 5 6 7
                       _ _ _ _ _ _ _ _
                       O O O O O O O O
                       U U U U U U U U
                       T T T T T T T T
                       0 1 2 3 4 5 6 7

 . = not connected         x = no connection possible
 * = signal feeds cell     ? = error, unable to fit
```

292074-43

Figure 29. iPLS II Report File For The iPLD610 Custom Register Design (Continued)

6.0 iPLD610 PROGRAMMING/ DEVELOPMENT SUPPORT

Design development and device programming support are important issues for PLDs because the silicon is useless without them. Design development tools such as Intel's PLDshell Plus and Data I/O's ABEL are required to convert state machine/boolean equation entries into the required device JEDEC file. The device programmer is then required to program each cell/fuse to configure the device to the user's needs.

Since devices with architectures identical to the iPLD610 have been available for a number of years, there is an existing level of support for this PLD already in existence. As mentioned earlier, the architecture, pin-out, and JEDEC map for the iPLD610 is identical to the Intel 85C060, 5C060, Altera EP600, EP610, and EP630, AMD PALCE630, and TI EP610 and EP630. Therefore, performance of existing designs using these devices can be improved by replacing these parts using the existing design/JEDEC files.

Full logic compilation and functional simulation for the iPLD610 is supported by PLDshell Plus software.

PLDshell Plus design software is Intel's user-friendly design tool for μPLD design. PLDshell Plus allows users to incorporate their prefered text editor, programming software, and additional design tools into a easy-to-use, menued design environment that includes Intel's PLDasm logic compiler and simulation software along with disassembly, conversion, and translation utilities. The PLDasm compiler and simulator software accepts industry stanard PDS source files that express designs as Boolean equations, truth tables, or state machines. On-line help, datasheet briefs, technical notes and error message information, along with waveform viewing/printing capability make the design task as easy as possible. PLDshell Plus software is available from Intel Literature channels or from your local Intel sales representative.

Tools that support schematic capture and timing simulation of the iPLD610 are available. Please refer to the "Development Tools" section of the Programmable Logic handbook.

The iPLD610 is supported by third-party logic compilers such as ABEL*, CUPL*, PLDesigner*, Log/IC, etc. Programming support is provided by third-party programmer companies such as Data I/O, Logical Devices, STAG, etc. Please refer to the "Third-Party Support" lists in the *Programmable Logic* handbook for complete information and vendor contacts.

The support summary shows an emphasis by Intel to provide timing/simulation models from Viewlogic and Quadtree for customers performing device/board simulations. The models are provided on most popular design platforms. The support summary reflects Intel's close relationship with key support tool vendors (which includes others not shown here) to provide iPLD610 customers design support with the format and package with which they are most familiar. These support tool vendors, such as Data I/O and Logical Devices, provide products in addition to the Intel development products. Intel provides complete design development support as detailed in Figure 5.2. Designs can be entered in several ways:

1. Schematic Capture using IPLDview-286—this Viewlogic Workview derivative allows gate/74xx macro level entry and supports design simulation (functional or timing).
2. State Machine entry using iSTATE—this Intel tool translates SMF (State Machine Format) designs into an ADF file.
3. Boolean Equation entry using PLDshell Plus—this logic compiler/minimizer generates device JEDEC/Report files from an ADF source file.

Based on the variety of offerings, users can pick the tool(s) that best fits their development environment. Also, programming support is available with Intel's GUPI adapters, which provide a quick and efficient method of device programming.

7.0 UPGRADING TO THE iPLD610

Because of the performance/architecture combination provided by the iPLD610 it may be desirable to upgrade an existing design for many reasons. Upgrading from 5C060 or EP6x0 devices can provide quick performance increases. Upgrading from 22V10 or 20RA10 devices may be done for performance, architecture, heat or power consumption reasons and may include the need for the standby power mode. Conversion of each of the devices mentioned here follows.

UPGRADE FROM 5C060

The Intel 5C060 PLD is pin- and JEDEC-compatible with the iPLD610. This allows existing 5C060 JEDEC files to be programmed directly into iPLD610. Therefore, designs running on 45 ns–55 ns t_{PD} performance levels can instantly be upgraded to 10 ns–25 ns t_{PD} performance levels provided by the iPLD610. The Intel development tool PLDshell Plus supports both Intel PLDs. Most non-Intel design development tools and device programmers also support both Intel devices.

UPGRADE FROM ALTERA/TI/AMD EP6x0

As discussed in Section 3, the A.C. and D.C. specifications of the iPLD610 meet or exceed those of competitive devices from Altera, TI and AMD. The list of devices which can be upgraded to the Intel iPLD610 includes:

- Altera EP600
- Altera EP610
- Altera EP610A
- Altera EP630
- TI EP610
- TI EP630
- AMD PALCE 610
- AMD PALCE 630
- Cypress EP610

Just as with the Intel 5C060, an upgrade of one of these devices can be accomplished by using existing JEDEC files from one of these devices to program directly onto an iPLD610. Also, Data I/O ABEL, Logical Devices CUPL and other design tools support the iPLD610. The only difference of note is the lack of a programmable standby current mode in the AMD device. Again, due to complete architecture compatibility the iPLD610 provides a quick and easy performance increase to any design using any of the above devices.

Due to differences in device programming parameters (such as programming voltages and pulse width requirements) all device programmers may not support the iPLD610 unless explicitly stated. Also, device simulation models are not interchangeable between devices due to timing differences.

UPGRADE FROM 22V10

Many designers requiring more architectural features than standard PAL devices offer have turned to the 22V10. Compared to standard PALs, the 22V10 offers additional outputs and product terms. However, the iPLD610 also has features not found in PAL devices. Since there are many differences between the iPLD610 and 22V10, the analysis will revolve first around device pin-out and then, cover performance, architecture, clocking options and D.C. specification issues.

Device Pinout

Table 9 shows the device pinouts of the iPLD610 and the 22V10 and highlights the differences. The iPLD610 has dedicated clock inputs at pins 1 and 13 while both of these can be inputs on the 22V10. The iPLD610 also has dedicated inputs at pins 14 and 23, while these are

Table 9. iPLD610/22V10 Pin-Out Comparison

DIP Pin #	iPLD610	22V10	Notes
1	CLK1	CLK/INPUT	Clock only on iPLD610
2	INPUT	INPUT	
3	I/O	INPUT	Input only on 22V10
4	I/O	INPUT	Input only on 22V10
5	I/O	INPUT	Input only on 22V10
6	I/O	INPUT	Input only on 22V10
7	I/O	INPUT	Input only on 22V10
8	I/O	INPUT	Input only on 22V10
9	I/O	INPUT	Input only on 22V10
10	I/O	INPUT	Input only on 22V10
11	INPUT	INPUT	
12	GND	GND	
13	CLK2	INPUT	Clock only on iPLD610
14	INPUT	I/O	Input only on iPLD610
15	I/O	I/O	
16	I/O	I/O	
17	I/O	I/O	
18	I/O	I/O	
19	I/O	I/O	
20	I/O	I/O	
21	I/O	I/O	
22	I/O	I/O	
23	INPUT	I/O	Input only on iPLD610
24	V_{CC}	V_{CC}	

I/O pins on the 22V10. However, there are 8 input-only pins (3–10) on the 22V10 that are I/O pins on the iPLD610. This is the main architectural advantage provided by the iPLD610. Table 10 shows a summary of performance (A.C. specifications of the iPLD610) compared to the 22V10–15. This includes combinational logic speed (t_{PD}), register performance (t_{CO_1} and t_{SU}), and maximum register speed (F_{MAX}).

ARCHITECTURE

A comparison of architectures shows that the iPLD610 has 6 more I/O pins (macrocells) than the 22V10, even though both are 24-pin devices. The main advantages of the 22V10 architecture are higher number of p-terms/macrocell (up to 16 for some macrocells) and capability of up to 22 inputs (compared to 20 for the iPLD610).

The number of p-terms (product terms or AND terms) required by any design is often greatly affected by the register type used. The 22V10 offers only D-type flip-flops, while the iPLD610 offers D, T, JK or RS register types. Register type selection is done on a macrocell-by-macrocell basis, so each specific function with the iPLD610 can be better optimized. Figure 30 shows an example of how register type selection can affect the number of p-terms required. The example shown is an MSB of a 4-bit counter which requires 5 p-terms using a D-type flip-flop, but only one p-term if a T-type flip-flop is used. By using the register type selection capability of the iPLD610 the designer can further minimize logic requirements.

Table 10. iPLD610/22V10 Specification Comparison

Area of Comparison	Feature	iPLD610-15	AMD 22V10-15	Lattice GAL 22V10-15
Performance	t_{PD}	15 ns	15 ns	15 ns
	F_{CNT}	50 MHz	50 MHz	50 MHz
	F_{MAX}	83 MHz	50 MHz	62.5 MHz
	t_{CO1}	8 ns	10	8 ns
	t_{SU}	12 ns	10	12 ns
Architecture	Macrocells	16	10	10
	Outputs	16	10	10
	Max Inputs	20	22	22
	Prog. Security Cell	Yes	Yes	Yes
	Ave P-Terms/Macrocell	8	12	12
	Individual Macrocell OE	Yes	Yes	Yes
	Reg Clock Options	3	1	1
	Indiv. Macrocell Clear	Yes	Yes	No
	Invert Control	Yes	Yes	Yes
	Reg. Power Up State	Low	High	High
	Register Types	D/T/RS/JK	D	D
D.C. Specifications	I_{CC}(max)	105 mA	180 mA	130*
	Power-Down Mode	Yes	No	No
	Standby Current	<150 μA	N/A	N/A
	I_{OL} (max)	12 mA	16 mA	16 mA

*F_{TOGGLE} = 15 MHz

Clocking Options

One other major architectural improvement provided by the iPLD610 is in the area of logic clocking options. Not only does the iPLD610 have two dedicated clock inputs (allowing separate synchronous clocking of macrocells), but each macrocell has a p-term dedicated as an asynchronous clock option.

D.C. Specifications

The final area of comparison between these two devices is D.C. specifications. The advantage in maximum supply current (I_{CC}) has benefits in many areas including power supply selection, cooling requirements and system reliability. The iPLD610 also offers a programmable standby current option which allows I_{CC} values to drop to 20 μA (typical) when in the standby mode. This can be useful if working with a "power budget" such as in laptop PC or Microchannel add-in card design. The difference in I_{OL} capabilities is very small (16 mA for the 22V10 versus 12 mA for the iPLD610).

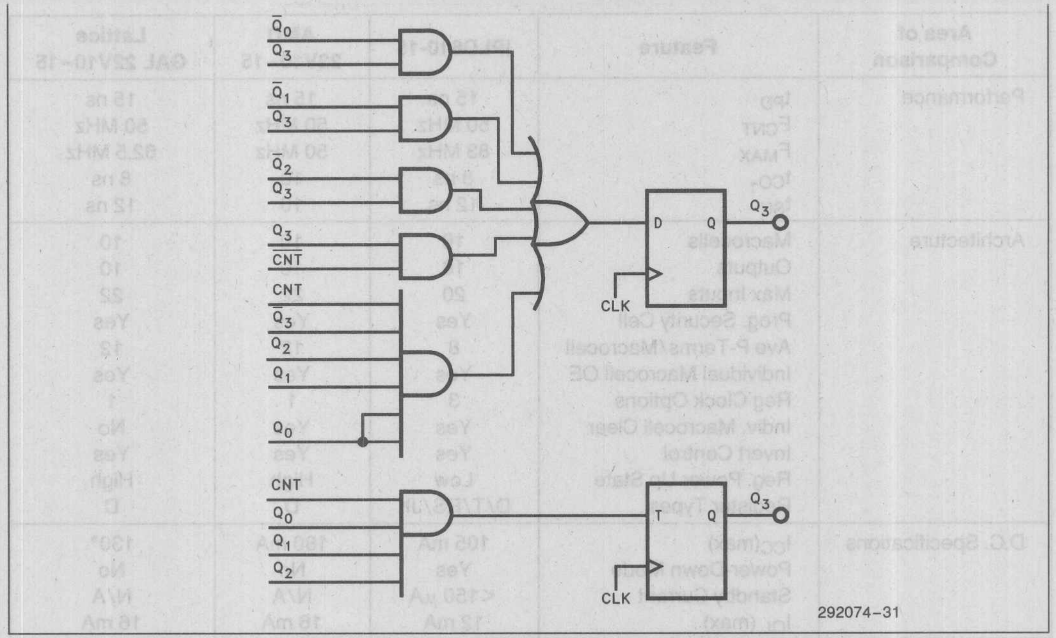

Figure 30. Product Term Requirements for D-Type and T-Type Flip-Flops (MSB of 4-Bit Counter)

22V10 to iPLD610 Conversion

NOTE:

There are NO performance related issues for this comparison due to design of iPLD610. No issues with registered operation (F_{MAX}, t_{CO}); no issues with combinatorial logic (t_{PD}).

There are several ways to replace a 22V10. A "pin-for-pin" replacement means the iPLD610 that is upgrading the 22V10 can be placed into an existing 22V10 socket and provide complete compatibility. A "functional" replacement is one in which the iPLD610 can replace the 22V10, but one or more of the pin numbers need to be changed. A functional replacement will only be an issue if the board is already made; if the upgrade is made at the design phase there is very little impact.

1. Determine if a pin for pin replacement can be made:
   a) Are there 8 or less p-terms used for each 22V10 output?
   b) Is pin 1 used as a Clock (rather than an Input)?
   c) Is pin 13 unused (i.e., is this input pin unused on the 22V10)?
   d) Is the global register preset feature unused?
   e) Is the output drive (I_{OL}) requirement for each output 12 mA or less?

NOTE:

Check for need of clock input at Pin 13 of the iPLD610.

If YES to all above, then pin-for-pin replacement looks good!

2. Determine if functional replacement can be made:
   a) Is the total number of inputs and outputs 20 or less?
   b) Are there 8 or less p-terms for each output?
      — If NO, can the number be reduced via iPLD610 register type selection, inversion control (DeMorgan's logic implementation) and/or use of async clock capabilities?
   c) Is the output drive (I_{OL}) requirement for each output 12 mA or less?
      — If NO, is there a spare iPLD610 output which can be utilized to duplicate this output and double the output drive capability?

If YES to questions above, then a functional replacement looks good!

3. In some cases the 5AC312 can also upgrade 22V10 sockets due to it's pin-for-pin compatibility, and superset architecture, although it's performance is not equal to that of the faster 22V10s.

4. In other cases the 22V10 and surrounding PLDs and/or 74xxx logic can be integrated into one of Intel's larger high-performance PLDs (such as the iPLD910). This is always an option if there are power, heat, or board space concerns.

Call The Intel Applications Hotline for Conversion Assistance
1-800-628-8686

UPGRADE FROM 20RA10

The 20RA10 presents designers requiring implementation of an asynchronous state machine or other asynchronous registered logic with a viable solution. The Intel iPLD610 provides these designers with another alternative. In many cases, a pin-compatible upgrade can be made due to architecture and performance features of the Intel iPLD610.

Device Pin-Out

Table 11 compares the device pinouts of the iPLD610 and the Lattice 20RA10. Both have up to 20 inputs, both are 24 pin devices (DIP package), and both have dedicated functions implemented at pins 1 and 13. The advantage provided by the iPLD610 are the 16 I/Os (macrocells), compared to only 10 for the 20RA10. This allows designers the flexibility to implement larger asynchronous state machines and/or additional synchronous or combinatorial logic.

Spec Comparison

A data sheet comparison of the Intel iPLD610 and Lattice 20RA10-15 is summarized in Table 12. The performance of the iPLD610is superior for both combinatorial logic (t_{PD}) and asynchronous register performance (F_{ACNT}, F_{AMAX}, t_{ACO_1}, t_{ASU}) as well as synchronous logic (which is not supported by the 20RA10). There are significant differences in register setup time that could be critical to a designer required to meet specifications of microprocessors or other system peripherals (such as an output valid delay spec).

Table 11. iPLD610/20RA10 Pin-Out Comparison

DIP Pin #	iPLD610	22V10	Notes
1	CLK1	PRELOAD	Dedicated on Each
2	INPUT	INPUT	
3	I/O	INPUT	Input only on 20RA10
4	I/O	INPUT	Input only on 20RA10
5	I/O	INPUT	Input only on 20RA10
6	I/O	INPUT	Input only on 20RA10
7	I/O	INPUT	Input only on 20RA10
8	I/O	INPUT	Input only on 20RA10
9	I/O	INPUT	Input only on 20RA10
10	I/O	INPUT	Input only on 20RA10
11	INPUT	INPUT	
12	GND	GND	
13	CLK2	OE	Dedicated on Each
14	INPUT	I/O	Input only on iPLD610
15	I/O	I/O	
16	I/O	I/O	
17	I/O	I/O	
18	I/O	I/O	
19	I/O	I/O	
20	I/O	I/O	
21	I/O	I/O	
22	I/O	I/O	
23	INPUT	I/O	Input only on iPLD610
24	V_{CC}	V_{CC}	

Table 12. iPLD610/20RA10 Specification Comparison Summary

Area of Comparison	Feature	iPLD610-10	Lattice 20RA10-15
Performance	t_{PD}	10 ns	12 ns
	F_{ACNT_1}	71.4 MHz	62.5 MHz
	F_{AMAX}	100 MHz	71.4 MHz
	t_{ACO_1}	12 ns	12 ns
	t_{ASU}	2 ns	7 ns
Architecture	DIP Pin Count	24	24
	Macrocells	16	10
	Outputs (I/Os)	16	10
	Inputs (max)	20	20
	Prog. Security Cell	Yes	No
	Total P-Terms/ Macrocell	10	8
	Indiv. Macrocell OE	Yes	No
	Reg. Preload	No	Yes
	Invert Control	Yes	Yes
	Reg. Types	D/T/JK/RS	D
	Clock Options	Sync/Async	Async Only
	Async Preset	No	Yes
	Async Clear	Yes	Yes
D.C. Specs	I_{CC} (max)	105 mA@1 MHz	100 mA@15 MHz
	Power Down Mode	Yes	No
	Standby I_{CC}	150 μA (max)	N/A
	I_{OL} (max)	12 mA	8 mA

Architecture

Comparing architectures, the iPLD610 offers more flexibility than the 20RA10. This is based on macrocell count, total p-terms/macrocell, register type selections, and clock options. The iPLD610 offers 6 more macrocells than the 20RA10. It also has 8 dedicated sum-of-product p-terms in addition to asynchronous register reset (clear) and async clock/OE p-terms. The 20RA10 has a total of eight p-terms for each macrocell, only four of which are dedicated to performing standard sum-of-products logic. Register type selections offered by the iPLD610 include D, T, RS and JK, while the 20RA10 implements only a D-type register. As mentioned in the section on upgrading from the 22V10, register type selection can have a significant impact on the number of p-terms required to implement a logic function and may allow a design to "fit" with one type, but not with another. Also, of note is the fact that the iPLD610 can implement synchronous (via 2 clock inputs) or asynchronous (via individual macrocell p-terms) registered logic. The designer using the 20RA10 can only implement asynchronous registered logic (using clock p-term) only. As mentioned earlier the synchronous register specifications of the iPLD610 (t_{SU}, t_H and t_{CO_1}) are slightly skewed from the asynchronous register specifications (t_{ASU}, t_{AH} and t_{ACO_1}). A designer using the iPLD610 can select clocking options on a macrocell-by-macrocell basis to best meet the needs of the system.

D.C. Specifications

Looking at D.C. specifications of these devices, the 20RA10 and the iPLD610 exhibit similar maximum supply current. But the iPLD610 offers a programmable power-down mode, which can put this device into a power saving mode useful in many applications. The I_{OL} of the iPLD610 is higher than the 8 mA maximum for the 20RA10.

8.0 SUMMARY

The iPLD610 represents the highest performer in one of the industry-standard PLD architectures. The advantages gained by using the iPLD610 extend past the

delay and counter capability. The iPLD610 provides the following capabilities:

- 12 mA I_{OL}
- Programmable Standby Mode
- 105 mA (max) I_{CC}
- 16 Macrocell Architecture
- 100% Testability due to EPROM Technology
- 111 MHz Register Operation

In addition, this device is offered with several speed and package options. The device is available in 10 ns, 15 ns and 25 ns t_{PD} speeds. The packages for the iPLD610 are Plastic DIP and PLCC.

Already highlighted were the architectural advantages of this device over standard programmable logic devices. These advantages include device level capabilities (16 macrocells, up to 20 inputs, dual clocking) and macrocell level capabilities (total of 10 p-terms per macrocell, register type selection, feedback control, async clocking). These capabilities of the iPLD610 device outperforms others at a data sheet level (A.C. and D.C. specifications). But, the iPLD610 was further highlighted by the characterization data presented, which demonstrates performance outside data sheet considerations. The combination of data sheet and device characterization information provides designers an added level of confidence in actual device behavior, and knowledge of actual in-system performance.

The iPLD610 device is well supported by PLD design and development tools from major third party vendors as well as Intel's own PLDshell Plus software.

One other advantage of the iPLD610 is the ease of upgrade it provides to systems using the 5C060, EP610/630, 22V10 or 20RA10. These devices can be quickly upgraded to the iPLD610 μPLD to gain performance, architectural, and power dissipation advantages.

The iPLD610 takes this standard architecture to a higher level. Its high performance in all areas open new applications to Intel μPLDs. Designers can now have both integration and performance!

APPLICATION NOTE

Designing with the 5AC312/5AC324 PLDs

DAVID BICKEL
PROGRAMMABLE LOGIC APPLICATIONS
INTEL CORPORATION

October 1993

Order Number: 292049-001

Designing with the 5AC312/5AC324 PLDs

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3

INTRODUCTION

The Intel 5AC312 PLD (Programmable Logic Device) was developed to break down certain existing PLD architectural barriers and meet increased performance needs. The Intel 5AC312 PLD was designed by PLD users with direct input from system designers. In the design process, emphasis was placed first on gate utilization, and then on density.

This application note highlights the advanced architecture and features of the 5AC312 PLD and shows the benefits of designing with this new device over more traditional PLD architectures. These features include enhanced input structure with register/latch option on all input pins (synchronous or asynchronous operation); user-controllable, software-supported p-term allocation scheme in all macrocells; and multiple p-terms on control functions (asynchronous CLK, SET, RESET, OE).

It should also be noted that the features and information described here also apply to the new 5AC324 PLD. The 5AC324 is basically a 24 macrocell version of the 5AC312.

PROGRAMMABLE INPUTS

The 5AC312 was designed with a highly flexible macrocell and I/O structure allowing the device to implement both combinational and sequential logic functions. The enhanced input structure not only allows the device to latch and hold incoming data, but also to implement register-combinational-register logic to easily accommodate state machine designs. Figure 1 shows a global view of the 5AC312 architecture.

The 5AC312 is equipped with 8 user-programmable input structures that can each be configured to work in one of five modes: 1) synchronous D-type register, 2) asynchronous D-type register, 3) synchronous D-type latch, 4) asynchronous D-type latch, and 5) flow-through input. Each input can be configured independently of the others. The desired configuration is implemented through the programming of EPROM architecture control bits by the logic compiler under user-control.

MACROCELL STRUCTURE

The 5AC312 also has a unique macrocell array structure that allows for user-controllable, software-supported product term allocation in each of its 12 macrocells. Each of the 12 macrocells also has a dual feedback option with independent feedback and I/O paths. Each macrocell has 16 product terms, 8 of which control the OE, PRESET, ASYNCHRONOUS CLOCK, and CLEAR signals (2 p-terms per signal). The other 8 feed the data input to the macrocell and are split into two groups of four (upper half and lower half). See Figure 2. Each group of four can be allocated to an adjacent macrocell if needed.

As shown in Figure 1, the 12 macrocells of the 5AC312 are further divided into two "rings" with 6 macrocells per ring. Allocation of p-terms to adjacent macrocells can occur with a given ring. See Figure 3 for p-term allocation scheme.

Each macrocell register in the 5AC312 is also equipped with an asynchronous PRESET signal. The PRESET function can be constructed in more traditional architectural devices such as the 5C060 and 5C090 using combinational logic and feedback, however two macrocells are consumed in the process. To illustrate this difference, compare Figure 2 to the implementation shown in Figure 4. The PRESET function would require additional macrocells in traditional architectures if it were expanded beyond a single p-term.

MULTIPLE P-TERMS

Multiple p-terms on the control functions (asynchronous CLOCK, PRESET, RESET, and OE) increases the efficiency of the device. Multiplexed I/O is accomplished by controlling the output buffer associated with each macrocell using the 2 p-terms set aside for implementing an OE function. Multiple p-terms create a means to avoid using macrocells for control logic. For example, it would take two macrocells in the iPLD610 and iPLD910 PLD to drive the OE line by a 2 p-term signal. To illustrate, compare Figure 2, the 5AC312 macrocell structure, to Figure 5, a diagram of how a two p-term OE signal can be implemented in a iPLD610 or iPLD910 PLD.

P-TERM ALLOCATION

P-term allocation allows for more efficient use of p-terms and thus increased device utilization by raising the number of p-terms per macrocell to 16. P-term allocation, where p-terms are dedicated to certain macrocells, should not be confused with p-term sharing, where several macrocells can actually use the same p-terms. The p-term allocation scheme in all macrocells is user-controllable and software supported, and provides the ability to satisfy designs with large p-term requirements. P-term allocation is ideal for p-term intensive applications such as complex counters or comparators.

P-term allocation in the 5AC312 is used when a design requires one of the 12 macrocells to employ more than 8 p-terms. P-term allocation is simply the transfer

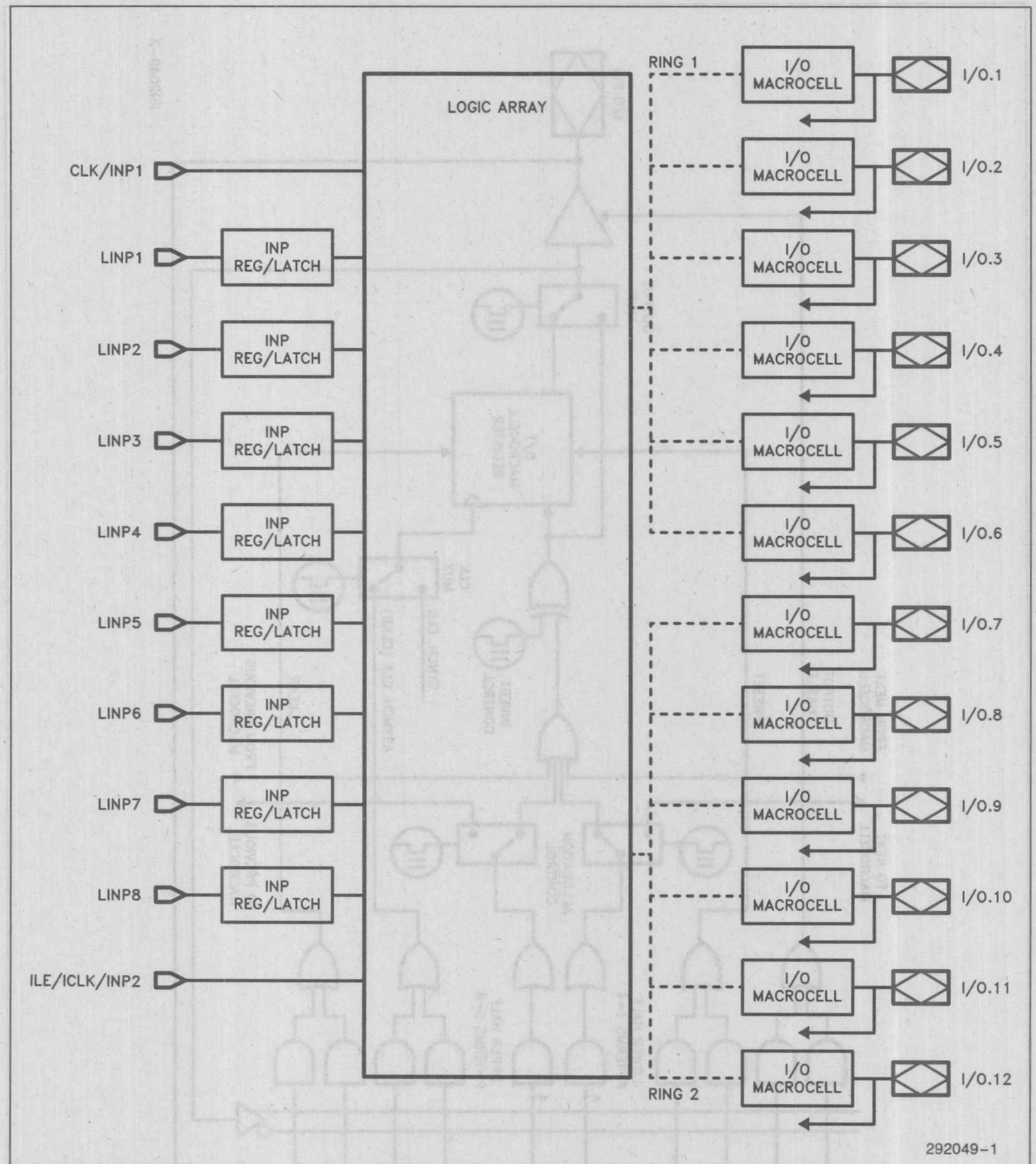

Figure 1. 5AC312 Architecture

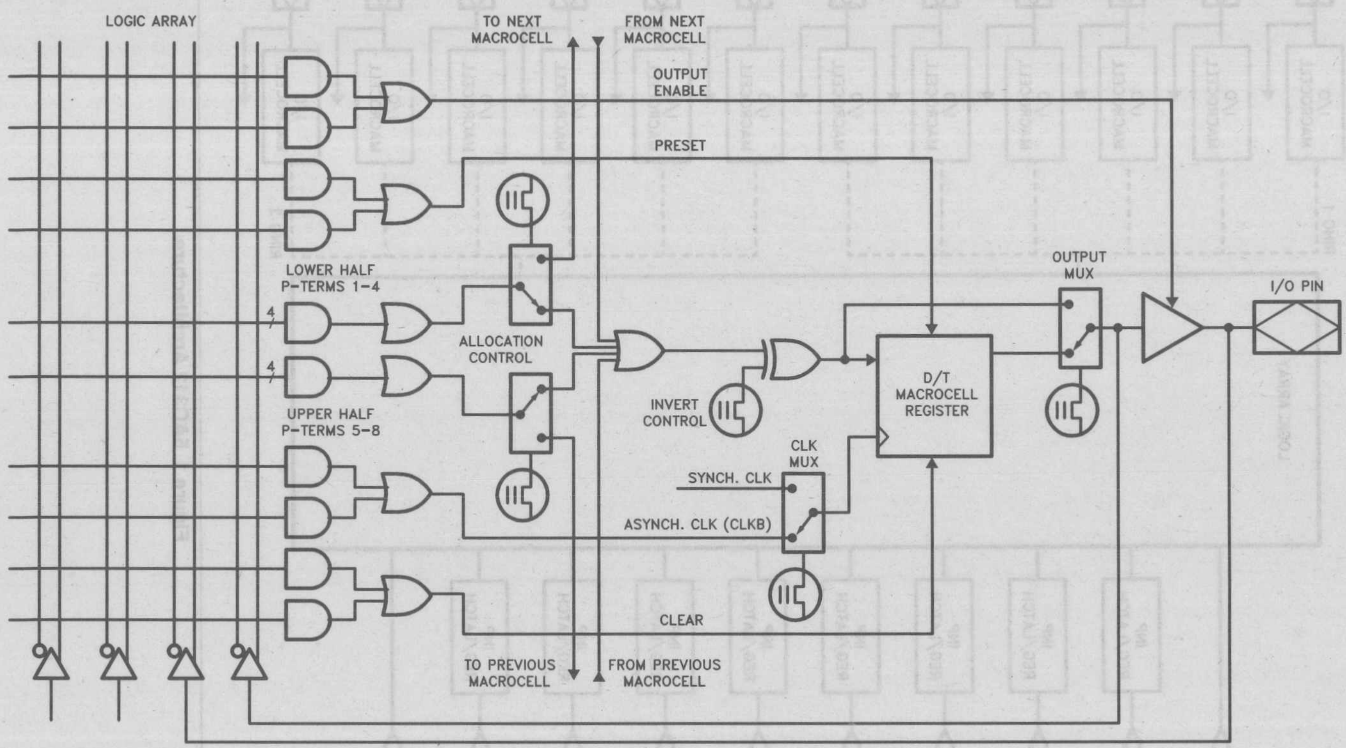

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Figure 2. 5AC312 Basic Macrocell Structure

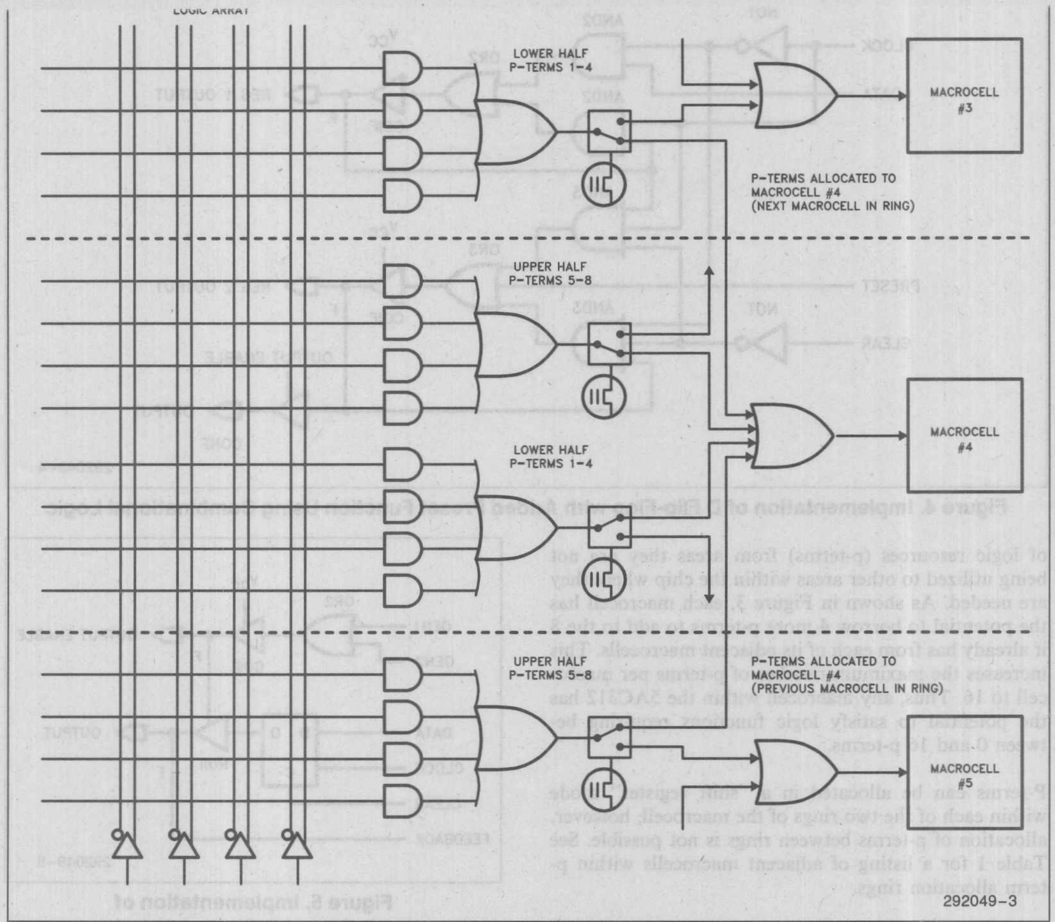

Figure 3. Product Term Allocation (8 + 4 + 4)

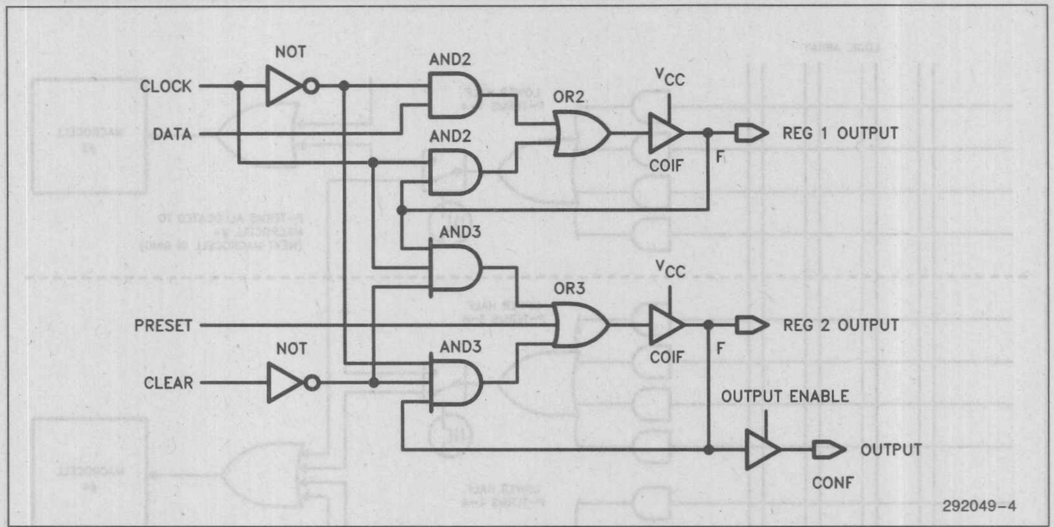

Figure 4. Implementation of D Flip-Flop with Added Preset Function Using Combinational Logic

of logic resources (p-terms) from areas they are not being utilized to other areas within the chip where they are needed. As shown in Figure 3, each macrocell has the potential to borrow 4 more p-terms to add to the 8 it already has from each of its adjacent macrocells. This increases the maximum number of p-terms per macrocell to 16. Thus, any macrocell within the 5AC312 has the potential to satisfy logic functions requiring between 0 and 16 p-terms.

P-terms can be allocated in a "shift register" mode within each of the two rings of the macrocell; however, allocation of p-terms between rings is not possible. See Table 1 for a listing of adjacent macrocells within p-term allocation rings.

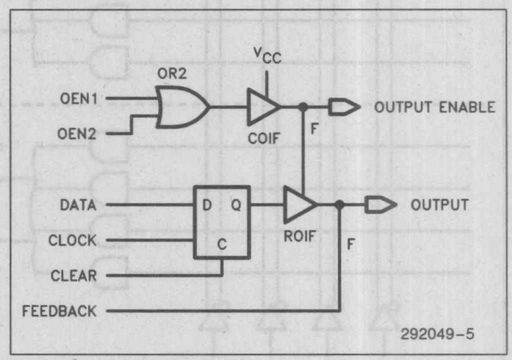

Figure 5. Implementation of 2 P-Term OE Control Signal

Table 1. 5AC312 Product Term Allocation Rings

Ring 1			Ring 2		
Current Macrocell	**Next Macrocell**	**Previous Macrocell**	**Current Macrocell**	**Next Macrocell**	**Previous Macrocell**
1	2	8	7	8	12
2	3	1	8	9	7
3	4	2	9	10	8
4	5	3	10	11	9
5	6	4	11	12	10
6	1	5	12	7	11

A given macrocell's output structure is still available for use when some or all of its p-terms are allocated away. If all of the p-terms of one macrocell are allocated away to its respective adjacent macrocells, the data input to that macrocell defaults to GND. This polarity can be changed through programming of the invert select EPROM bit. The I/O register as well as all secondary controls to this I/O control block are still available and can be used as needed for design purposes.

DUAL FEEDBACK

The 5AC312 contains separate input and feedback paths (dual feedback) on each of the macrocell I/O control blocks. This allows designs to utilize input pins when the associated macrocells have been assigned a no output with buried feedback primitive. Multiplexed I/O is accomplished by controlling the output buffer associated with each macrocell using the 2 p-terms that implement the OE function. Registered outputs may be clocked from the synchronous CLK/INP1 pin or asynchronously clocked by the 2 p-terms available for ASYNCH_CLK.

POWER ON CHARACTERISTICS

Another feature of the 5AC312 is its power-on characteristics. The I/O registers of the 5AC312 experience a reset to their inactive state upon Vcc power-up. Using the PRESET function available for each macrocell allows any particular register preset to be achieved after power-up. The inputs and outputs of the 5AC312 begin responding approximately 10 μs (6 μs typical) after Vcc power-up or after a power-loss/power-up sequence.

POWER DOWN MODE

A trade-off between power consumption and speed is possible when using the 5AC312 by programming the "Turbo Bit". Left unprogrammed and with no transition occurring at the device inputs for a period of approximately 100 ns, the device powers-down the internal array while holding the outputs at their previous levels. At the next input transition occurrence, the 5AC312 powers-up the array and reacts to the change in input conditions. If the "Turbo Bit" is programmed, the power-down circuitry is disabled and the device will not power-down even if there are no more transitions. The array power-up sequence requires an additional 20 ns of propagation delay. Power supply current during power-down is no more than 120 μA. See Figure 6.

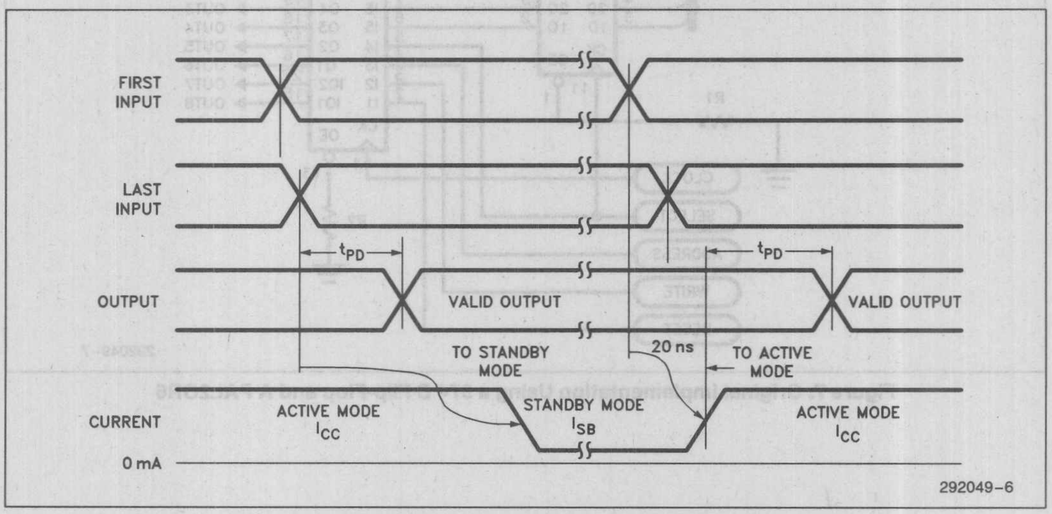

Figure 6. 5AC312 Standby and Active Mode Transitions

EXAMPLE

An example application for the 5AC312 can be shown by replacing a PAL* 20R6 and a 374 D type flip-flop in a design due to a power constraint. The same implementation can be achieved consuming less power using one 5AC312 PLD. Compare Figures 7 and 8. Straight jumpers can be substituted in the PC board where the 374 sits, and since the clock signal is already available on the PAL socket, it can be internally routed to clock the input registers of the 5AC312. The 5AC312 can then be programmed to match the existing pin assignments and therefore require no PC board re-layout. The internal circuitry of the 5AC312 allows the PLD to act as both a D type flip-flop and a PAL.

SUMMARY

The 5AC312 PLD, which uses advanced CHMOS EPROM cells as logic control elements instead of polysilicon fuses, represents an innovative device to help overcome the primary limitations of standard PLDs. With its advanced features, proprietary architecture and macrocell structure, the 5AC312 is capable of implementing high performance logic functions more effectively than was previously possible. The p-term allocation scheme is a unique feature, increasing the efficiency of the device immensely. The PRESET signal and 2 p-term control lines are also features giving the 5AC312 added efficiency in many designs.

These same architectural features have been included in the 5AC324 PLD, making that device ideal for even higher integration applications. Refer to the 5AC324 Data Sheet for details on that device.

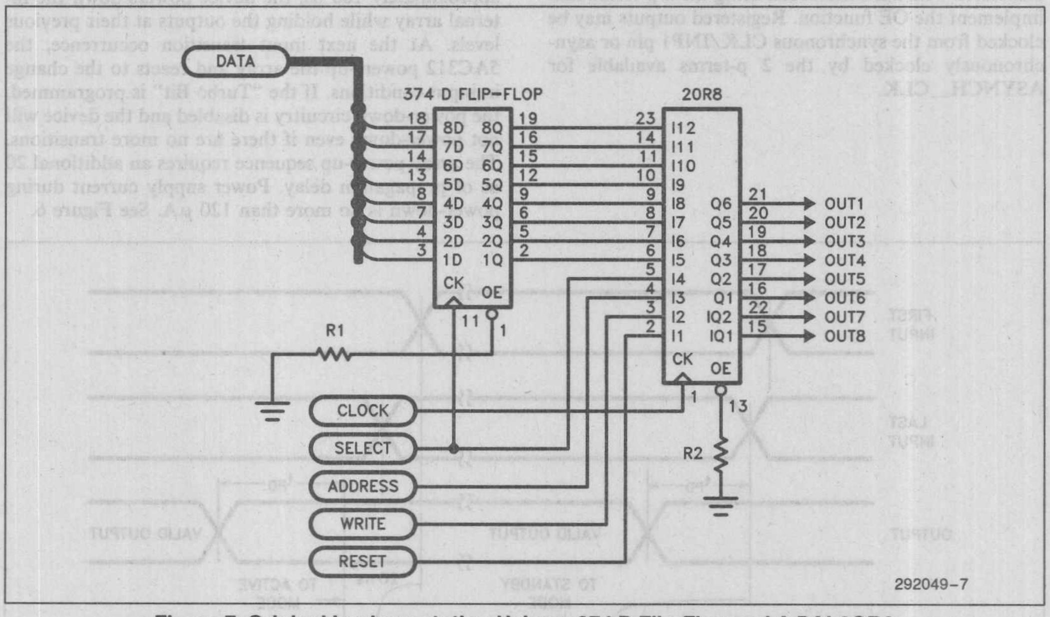

Figure 7. Original Implementation Using a 374 D Flip-Flop and A PAL2OR6

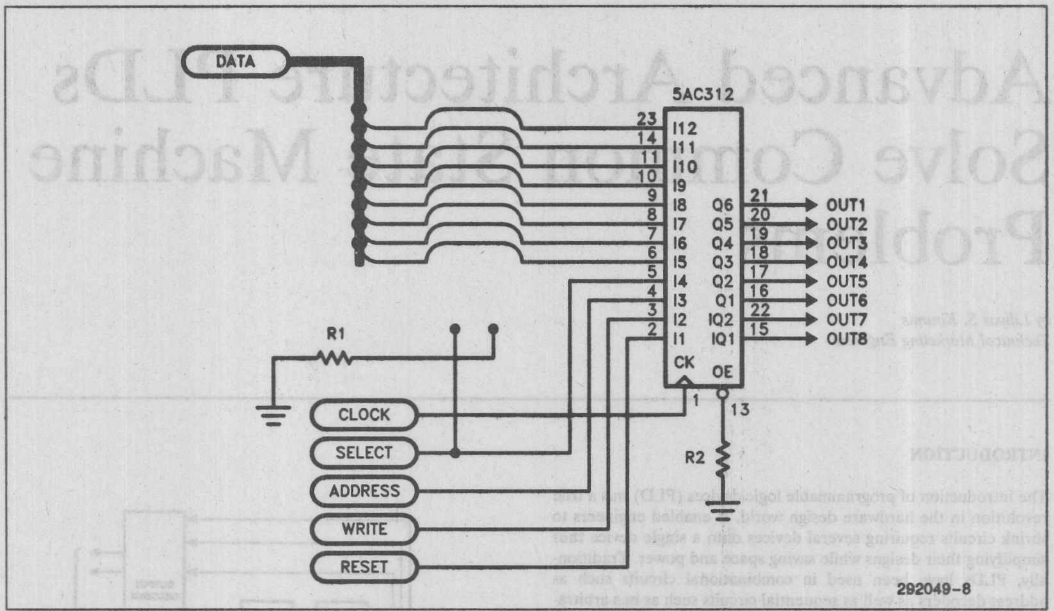

Figure 8. Example Implementation Using the 5AC312

3

Advanced Architecture PLDs Solve Common State Machine Problems

by Liliyas S. Koumis
Technical Marketing Engineer

INTRODUCTION

The introduction of programmable logic devices (PLD) was a true revolution in the hardware design world. It enabled engineers to shrink circuits requiring several devices onto a single device thus simplifying their designs while saving space and power. Traditionally, PLDs have been used in combinational circuits such as address decoders as well as sequential circuits such as bus arbitration schemes. During the last few years, advances and improvements in PLD architectures enabled the devices to grow more complex while addressing the never-ending quest for higher density and faster speeds. Despite these improvements, engineers still face certain problems and limitations when implementing state machine designs with PLDs. The Intel 5AC312 and 5AC324, multipurpose generic erasable PLDs, offer a solution to these problems that gives engineers a better device to implement their designs.

A typical programmable logic device is composed of a user-programmable AND array, a fixed OR gate, followed by an output register which includes a feedback path from the output to the programmable AND array. Combination of these elements is commonly referred to as a 'macrocell.' The existence of a feedback path from the output registers to the AND array makes PLDs ideal candidates for state machine implementations.

TYPES OF STATE MACHINES POSSIBLE IN PLDs

The three basic categories of state machines are Class A, Class B and Class C, better known as MEALY, MOORE TYPE A and MOORE TYPE B respectively. It is possible to implement any of the classes of state machines in a PLD, however the efficiencies vary with state machine class. The main characteristic of the Class A machine is that its outputs to the external world are a function of both the input and the present state of the machine as shown in Figure 1. Mathematically, this can be expressed as:

$$z^{n+1} = f(x^n, y^n)$$

Class A Machine
(Mealy Machine)

where 'z' is the decoded output, 'x' is the input, 'y' is output of the next state decoder and 'n' is the present state.

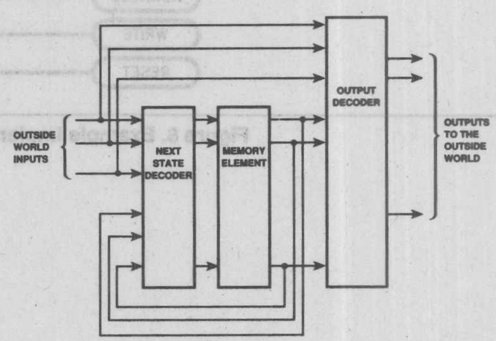

Figure 1. Class A State Machine

The Class B machine differs from Class A in that its output is only dependent on the present state of the machine through output decoding, or better expressed as:

$$z^{n+1} = f(y^n)$$

Class B Machine
(Moore Type A Machine)

Finally, the Class C macine is essentially the same as the Class B but requires no output decoding: the outputs *are* the next state of the machine:

$$z^{n+1} = y^{n+1}$$

Class C Machine
(Moore type B Machine)

If a Class A or a Class B machine is implemented in a standard PLD, two macrocells would be required per state; one macrocell

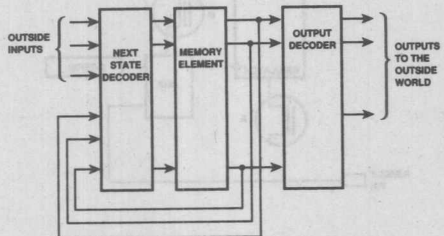

Figure 2. Class B State Machine

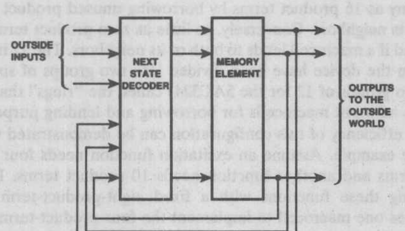

Figure 3. Class C Machine

has to be used for the input decoding and the other for the output decoding. The use of an extra macrocell for output decoding is not an efficient use of the device resources. For example, the largest state machine that can be implemented in an eight-register PLD is one with only four states variables. On the other hand, since a Class C machine does not perform output decoding, only one macrocell per state is required. As a result, that a machine with eight state variables could easily fit in the same eight-register PLD.

PROBLEMS WITH STATE MACHINE DESIGNS IN PLDs

Despite the architectural advantages of implementing a Class C machine, traditional PLDs still inherit serious timing problems and structural shortcomings.

The first problem is violation of setup and hold times of the output registers. This is encountered commonly in environments where the inputs are asynchronously changing with the device clock. Sources for these problems may be different data paths for each input or origination of these input signals from circuits that use a different clock than that used for the output registers. This kind of problem causes the output to glitch and may cause the machine to enter an invalid or incorrect state. The problem traditionally has been solved by adding external metastable-hardened registers to synchronize the inputs with the outputs. This solution, tion. In some cases, an eight-register IC is added even when only a few inputs must be synchronized.

The second most common problem is missed input pulses of short duration. In modern and complex circuits, short pulses may arrive at the inputs and disappear at a faster rate than the PLD clock. This causes these inputs to be missed by the PLD, which in turn causes erroneous operation of the state machine. Traditional PLDs offer no solution to this problem. Engineers have had to resort to adding circuitry to ensure that the inputs are present long enough to be seen by the PLD clock. This additional circuitry further complicates designs, adds delays, increases power consumption and adds an unnecessary burden to the engineers.

Finally, the most frustrating problem for engineers is that the number of product terms available per macrocell is fixed. Engineers usually assign the states to the output pins randomly, write the equations and allow the software to determine whether the equations fit their chosen device. If the number of product terms required to implement the given equations is greater than the fixed number of available product terms, the designer devotes additional time and resorts to more 'innovative' approaches, such as breaking down the state machine into smaller parts to fit the device. This not only introduces additional time delays and reduces the effective use of the device, but it also increases development time and board cost.

SOLUTIONS TO THESE COMMON PROBLEMS

The above discussion illustrates the need for a more sophisticated generation of Programmable Logic Devices that address these problems. Two new Intel PLDs, the 5AC312 and 5AC324, are specifically targeted at fulfilling the requirements of better set-up and hold timing, faster input clock rate and flexible product terms. The AC in the part name stands for "Advanced CMOS," the 3 stands for third generation and 12/24 is the number of macrocells in each device. This family of Intel Erasable Programmable Logic Devices uses advanced CHMOS* EPROM cells instead of polysilicon fuses as a logic control element. This process enhances the testability and reliability of the devices while significantly reducing power consumption. For the remaining portions of this paper, the 5AC312 will be referred for ease of reference, but for all practical purposes, the 5AC324 is functionally identical to the 5AC312 but contains twice the number of macrocells and ten register/latched inputs instead of eight.

As it can be seen in Figure 4, the 5AC312 has the architectural features of a Class C machine but also offers additional features address the issues discussed earlier. The input structure of the 5AC312 offers several programmable options, each addressing a particular need or problem.

To address the first problem-violation of setup and hold times of the output registers—the 5AC312 offers an additional register/latch input with a programmable clock. The clock can be the same as the output register clock shifted by 180°, a separate high frequency clock, or be generated by a product term from the logic array.

By using the first clock option, synchronization is achieved, and thus the risk of output glitches is minimized. By cascading the input and output registers and shifting the input clock 180° from the output register clock, an additional advantage is gained by

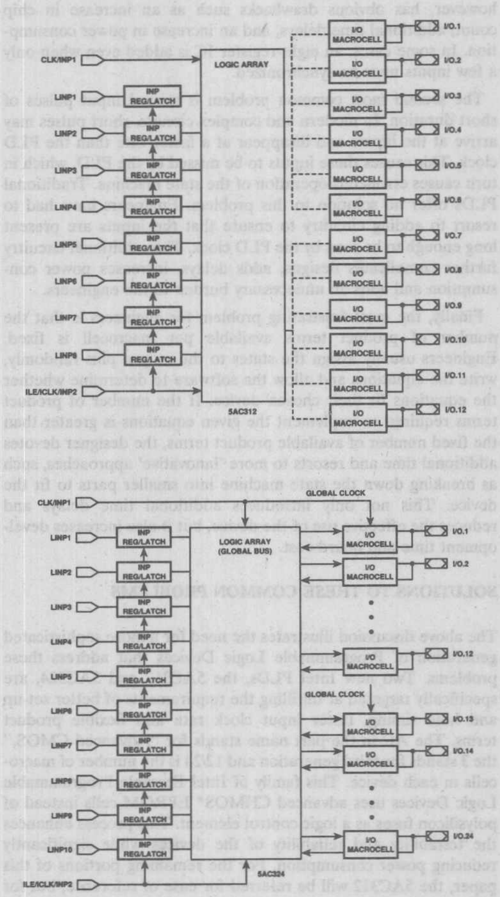

Figure 4. Architecturally Advanced 5AC312 and 5AC324 Global Block Diagrams

allowing enough time to satisfy the setup and hold time requirements of the output registers. Metastability characteristics of the device is of particular concern and are discussed later in this paper.

The second option, a separate high frequency clock, enables the device to sample inputs of very short time duration. This clock operates up to 50 MHz, with an input register setup of only 5 ns. If the latch feature is selected, the setup time is reduced to 0 ns. Of course, a mode can be selected where the input data flows through, bypassing the register/latch combination. The third clock option, clocking the input registers with the output of a product term from the logic array, is ideal for applications where registers are to be clocked only when a certain input condition is met.

To address the fixed product term problem, the 5AC312 implements an innovative solution called 'product term allocation.' In

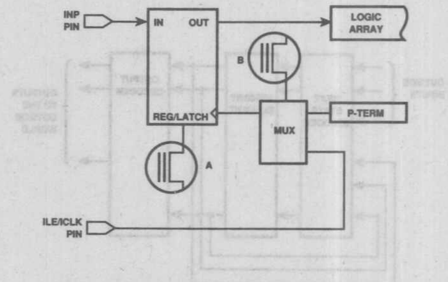

Figure 5. 5AC312/5AC324 Input Structure

each individual macrocell, the eight product terms are sub-divided into two groups of four. The product term allocation is achieved by allowing each of these four product term groups to be borrowed from or lent to adjacent macrocells. By 'allocating' product terms between adjacent macrocells, any register can be driven by as many as 16 product terms by borrowing unused product terms from its neighbors. Conversely, as little as zero product terms can be used if a macrocell lends to both of its neighbors. The 12 macrocells in the device have been divided into two groups of six each (or two groups of 12 for the 5AC324) called the "rings" that help define adjacent macrocells for borrowing and lending purposes.

The efficiency of this configuration can be demonstrated with a simple example. Assume an excitation function needs four product terms and another function needs 10 product terms. Implementing these functions with a fixed eight-product-term PLD requires one macrocell to implement the four-product-term function, and two macrocells to implement the 10 product terms function. To fit the 10 product term function, the equation needs to be broken into two parts, thereby increasing the delay. Therefore, out of 24 available product terms (three groups of eight), 14 are used (14/24 = 58% efficiency). Using the 5AC312 to implement the same functions yields the following: the four-product-term function is implemented with half of a macrocell, allowing the other half to be allocated to the adjacent macrocell for implementing the 10-product-term function. No design-splitting is required. Therefore, out of 16 product terms, 14 are used. This translates to 88% product term utilization. The product term allocation is completely transparent to the user since it is achieved through software. When the compiler determines that an additional number of product terms is required, it automatically allocates resources to fit the required excitation function.

METASTABILITY CHARACTERISTICS

Although metastability is a relatively rare event, ignoring it can cause serious timing problems. The input registers found in the 5AC312 offer excellent recovery time where metastability is of concern. Metastability can be simply described as the inability of a register to decide the state of its output within a fixed amount of time. This event usually occurs when synchronizing an external event with a periodic clock. If a flip flop is clocked nearly at the same time as changing data, there is a small window of time where the output of the register is unknown. This window of time is the recovery time (t_{re}) of the flip-flop and is typically in the order of nano-seconds. Designers at Intel have performed tests to obtain the recovery time for the 5AC3xx family of devices and have concluded that the Intel devices have better recovery times

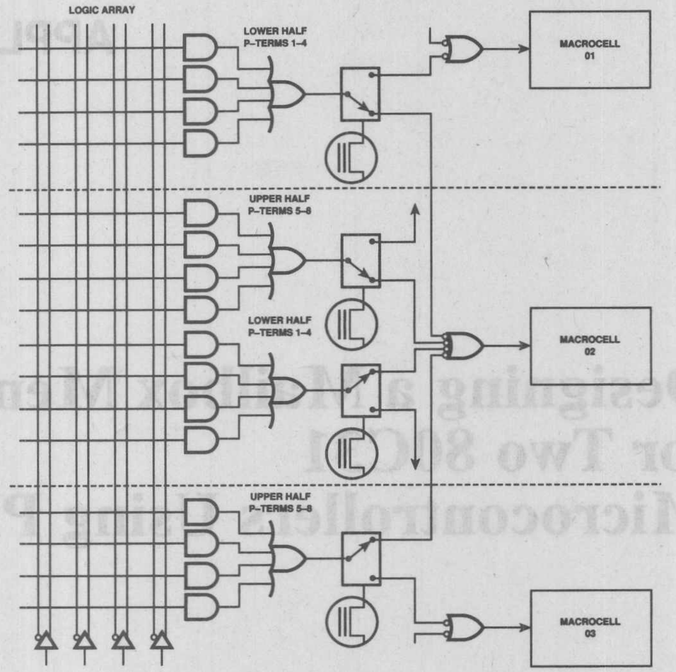

Figure 6. Product Term Allocation

than familiar TTL devices such as 74F74. Table 1 shows sample data taken at a clock frequency of 2 MHz and data frequency of 1 MHz.

Additional information on the procedure used to obtain this data and its use can be found in references one and three.

CONCLUSION

Because of their internal architectural characteristics Programmable Logic Devices have become the ideal method to implement state machine designs. This is evident by the wide variety of applicatons where programmable logic devices are found today. The latest generation of PLDs, with the advantages of programmable I/O pins and expanded number affixed product terms, are certain to replace traditional off-the-shelf logic as designers discover their usefulness in modern applications. However, to overcome the problems associated with setup and hold time violations, missed inputs and fixed number of product terms, a new generation of PLDs was needed. The Intel 5AC312 and 5AC324 overcome these problems by providing selectable input register/latch option with excellent metastability characteristics and allocatable product terms.

Table 1

Device	Recovery Time (ns)
7474	1.6
74LS74	1.5
74S374	0.91
74F373	0.70
74F74	0.40
5AC312/5AC324	0.35

*CHMOS is a patented process of Intel Corporation.

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APPLICATION BRIEF

Designing a Mailbox Memory for Two 80C31 Microcontrollers Using PLDs

K. WEIGL & J. STAHL
INTEL CORPORATION
MUNICH, GERMANY

September 1993

Order Number: 292016-004

DESIGNING A MAILBOX MEMORY FOR TWO 80C31 MICROCONTROLLERS USING PLDs

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INTRODUCTION

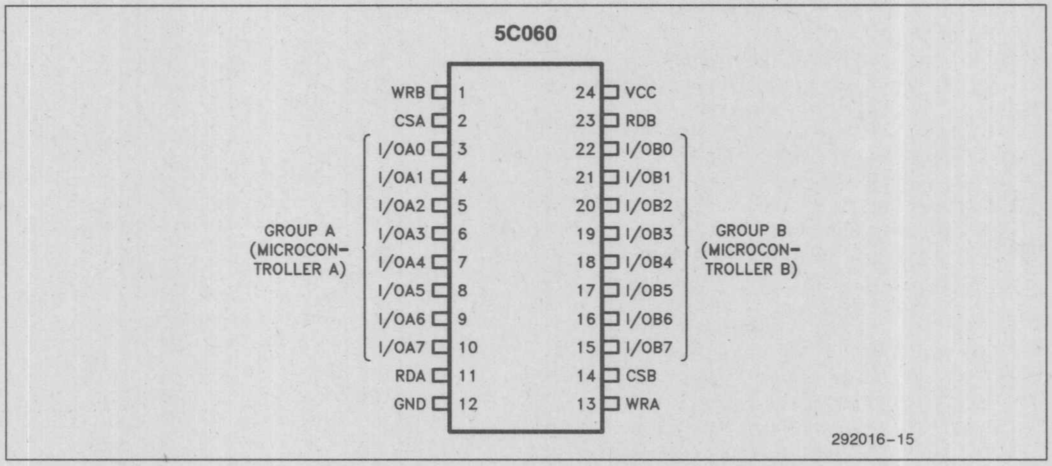
Very often, complex systems involve two or more microcontrollers to fulfill the requirements defined by a given objective. Since the nature of microcontrollers does not allow for easy dual-port memory design (no "READY" input; no "HOLD/HLDA" interface; port-oriented I/O etc.), design engineers are faced with the problem of interchanging information (data and status) between those microcontrollers. This application brief describes the design of a mailbox for exchanging information between two 80C31s, using a 5C060 PLD as a "back-to-back" register, and a 5C032 PLD as an arbitration vehicle to control the actions of the CPUs.

THE 5C060 MAILBOX

In this application, the 16 macrocells of the 5C060 are grouped into two sets of 8 so called "ROIF" (register output with input feedback) primitives to implement the two 8 bit bus interfaces needed. The grouping is done according to the following picture.

The 5C060 allows for independent clocking of 8 macrocells on each side of the chip, the two clock inputs are used to clock data from the microcontroller bus into the chip. To read the data written into the mailbox by one of the controllers, the RDA- (controller A is reading) or RDB- (controller B is reading) line must be pulled low by activating the read command (/RD). In order to avoid spurious read-cycles, the /RD commands from both microcontrollers are logically "ORed" together with an active high CS-signal (Chip Select) inside the 5C060. The CS-signal for both ports is derived from address line A15. Therefore, whenever A15 becomes a logic "1" (true), the mailbox is activated and ready to take or submit data.

Address range for the mailbox: F000 Hex to FFFF Hex (Upper 12 kbyte)



THE 5C032 "MAILBOX CONTROLLER"

To keep the two microcontrollers informed about the status of their mailbox, the 5C032 is programmed to supply the following signals to both controllers:

```
/OBFA: "OUTPUT BUFFER FULL" FOR MC A

/OBFB: "OUTPUT BUFFER FULL" FOR MC B

/IBEA: "INPUT BUFFER EMPTY" FOR MC A

/IBEB: "INPUT BUFFER EMPTY" FOR MC B

/INTA: INTERRUPT TO MC A

/INTB: INTERRUPT TO MC B
```

The next section will discuss the meanings of these signals in more detail.

Output Buffer Full: This flag is set whenever the controller writes into its own output buffer. The flag remains valid, until the second controller has read the data. The flag is automatically reset to its inactive state when this read cycle is accomplished.

NOTE:
Both controllers can access (read or write) the mailbox simultaneously.

Input Buffer Empty: This flag indicates that there is no message in the mailbox. The flag will become inactive as soon as one microcontroller places a message for the other one (or vice versa).

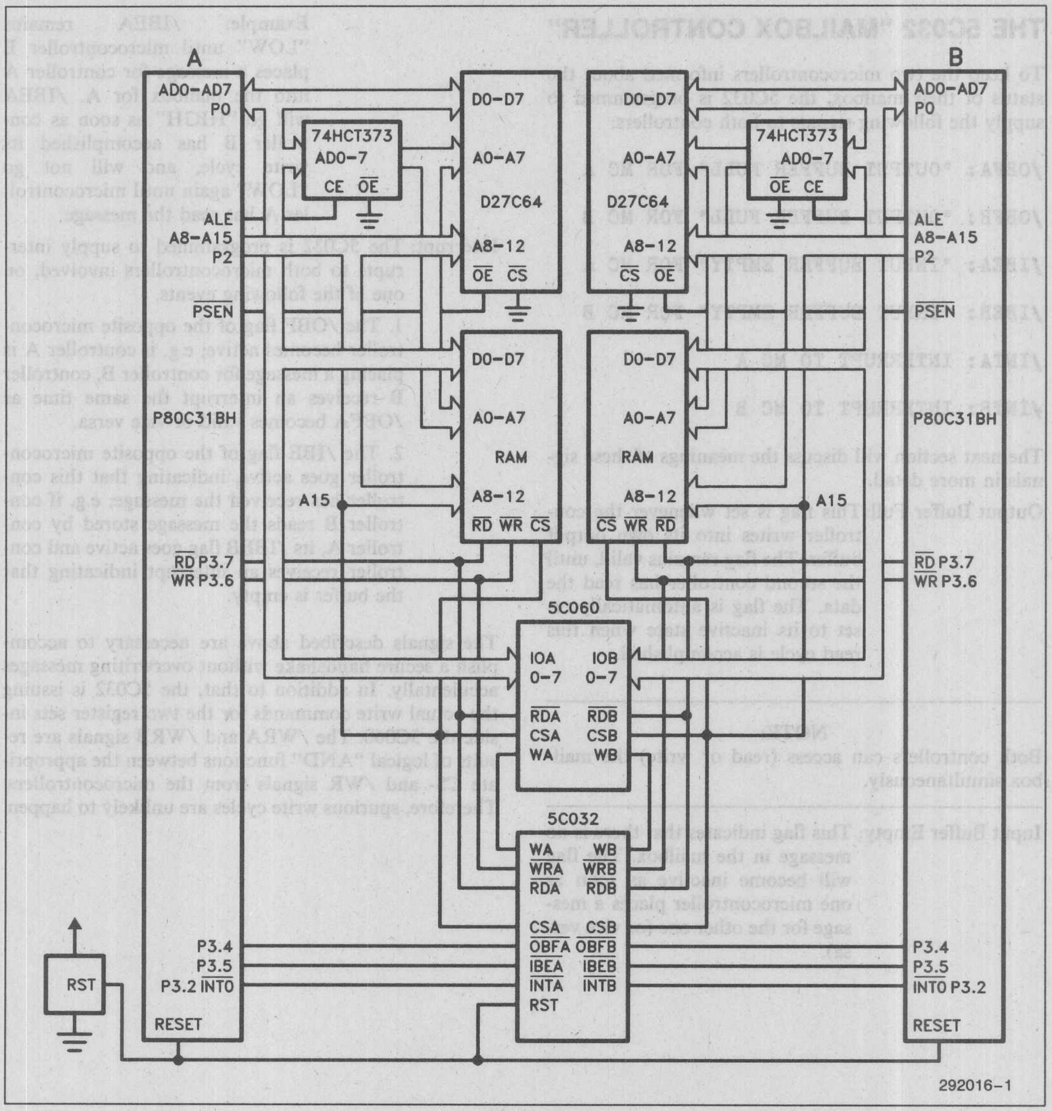
Example: /IBEA remains "LOW" until microcontroller B places a message for controller A into the mailbox for A. /IBEA will go "HIGH" as soon as controller B has accomplished its write cycle, and will not go "LOW" again until microcontroller A has read the message.

Interrupt: The 5C032 is programmed to supply interrupts to both microcontrollers involved, on one of the following events.

1. The /OBF flag of the opposite microcontroller becomes active; e.g. if controller A is placing a message for controller B, controller B receives an interrupt the same time as /OBFA becomes valid or vice versa.

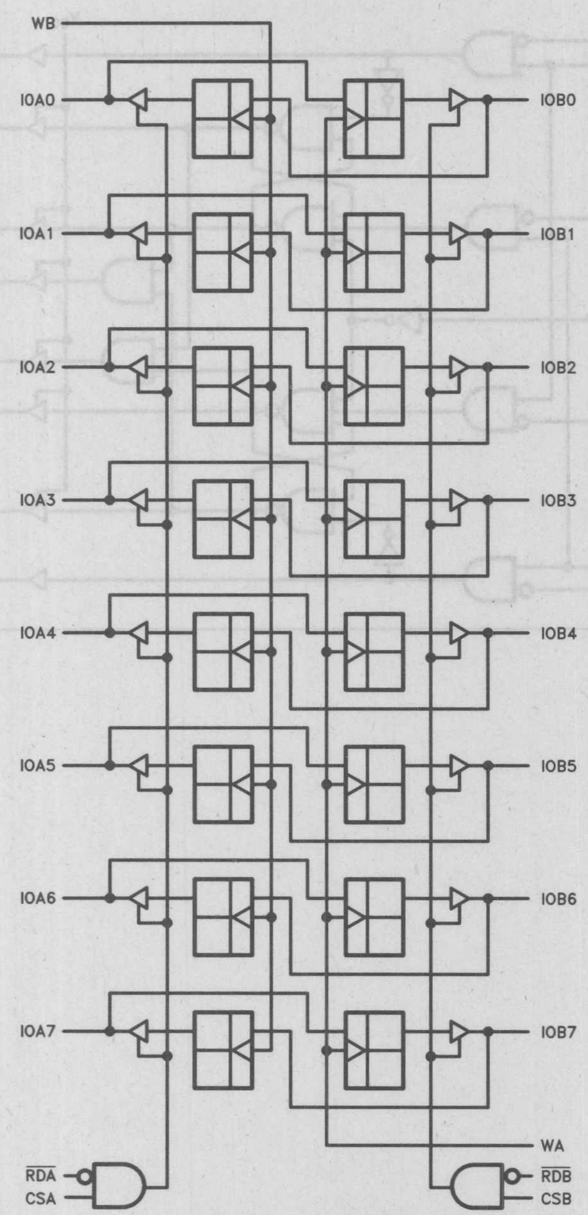
2. The /IBE flag of the opposite microcontroller goes active, indicating that this controller has received the message; e.g. if controller B reads the message stored by controller A, its /IBEB flag goes active and controller receives an interrupt indicating that the buffer is empty.

The signals described above are necessary to accomplish a secure handshake without overwriting messages accidentally. In addition to that, the 5C032 is issuing the actual write commands for the two register sets inside the 5C060. The /WRA and /WRB signals are results of logical "AND" functions between the appropriate CS- and /WR signals from the microcontrollers. Therefore, spurious write cycles are unlikely to happen.



Block Diagram

5C060 "BACK TO BACK REGISTER"



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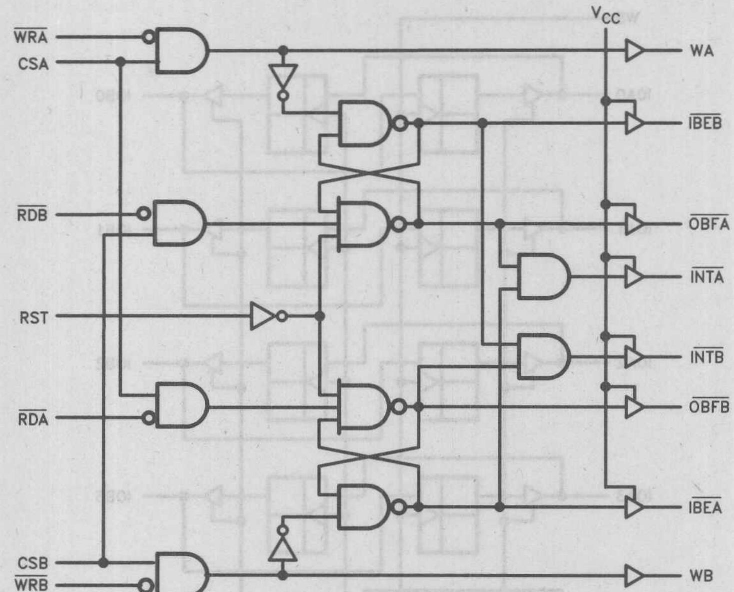
5C032 "MAILBOX CONTROLLER"



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JUERG STAHL
INTEL ZUERICH
August 28, 1989
80C31 MAILBOX MEMORY USING 5C060 / 5C032
REV 5
5C060

PART: 5C060
INPUTS: WB@1, CSA@2, CSB@14, nRDA@11, nRDB@23, WA@13
OUTPUTS: IOB7@15, IOA7@10, IOB6@16, IOA6@9,
         IOB5@17, IOA5@8, IOB4@18, IOA4@7,
         IOB3@19, IOA3@6, IOB2@20, IOA2@5,
         IOB1@21, IOA1@4, IOB0@22, IOA0@3

NETWORK:
        IOB7,DB7 = ROIF(DA7,WAC,GND,GND,RDBC)
        IOB6,DB6 = ROIF(DA6,WAC,GND,GND,RDBC)
        IOB5,DB5 = ROIF(DA5,WAC,GND,GND,RDBC)
        IOB4,DB4 = ROIF(DA4,WAC,GND,GND,RDBC)
        IOB3,DB3 = ROIF(DA3,WAC,GND,GND,RDBC)
        IOB2,DB2 = ROIF(DA2,WAC,GND,GND,RDBC)
        IOB1,DB1 = ROIF(DA1,WAC,GND,GND,RDBC)
        IOB0,DB0 = ROIF(DA0,WAC,GND,GND,RDBC)
        IOA7,DA7 = ROIF(DB7,WBC,GND,GND,RDAC)
        IOA6,DA6 = ROIF(DB6,WBC,GND,GND,RDAC)
        IOA5,DA5 = ROIF(DB5,WBC,GND,GND,RDAC)
        IOA4,DA4 = ROIF(DB4,WBC,GND,GND,RDAC)
        IOA3,DA3 = ROIF(DB3,WBC,GND,GND,RDAC)
        IOA2,DA2 = ROIF(DB2,WBC,GND,GND,RDAC)
        IOA1,DA1 = ROIF(DB1,WBC,GND,GND,RDAC)
        IOA0,DA0 = ROIF(DB0,WBC,GND,GND,RDAC)
        WAC = INP(WA)
        WBC = INP(WB)
        CSB = INP(CSB)
        CSA = INP(CSA)
        nRDB = INP(nRDB)
        nRDA = INP(nRDA)

EQUATIONS:

        RDBC = CSB * !nRDB;

        RDAC = CSA * !nRDA;


END$
```

292016–4

```
JUERG STAHL
INTEL ZUERICH
August 28, 1989
80C31 MAILBOX MEMORY USING 5C060 / 5C032
REV 5
5C032

PART: 5C032
INPUTS: RST, nWRA, nRDB, CSA, nRDA, nWRB, CSB
OUTPUTS: WA, nOBFA, nIBEB, nINTA, nINTB, nOBFB, nIBEA, WB

NETWORK:
     nWRA = INP(nWRA)
     nRDA = INP(nRDA)
     CSA = INP(CSA)
     nWRB = INP(nWRB)
     nRDB = INP(nRDB)
     CSB = INP(CSB)
     RST = INP(RST)
     WA = CONF(WAd,VCC)
     WB = CONF(WBd,VCC)
     nOBFA,nOBFA = COIF(nOBFAd,VCC)
     nOBFB,nOBFB = COIF(nOBFBd,VCC)
     nIBEA,nIBEA = COIF(nIBEAd,VCC)
     nIBEB,nIBEB = COIF(nIBEBd,VCC)
     nINTA = CONF(nINTAd,VCC)
     nINTB = CONF(nINTBd,VCC)

EQUATIONS:

        nINTBd = nOBFB * nIBEB;
        nINTAd = nOBFA * nIBEA;
        nOBFBd = !(!(!nRDA * CSA) * nIBEA * !RST);
        nOBFAd = !(!(!nRDB * CSB) * nIBEB * !RST);
        nIBEBd = !(!(CSA * !nWRA) * nOBFA);
        nIBEAd = !(!(CSB * !nWRB) * nOBFB);
        WAd = CSA * !nWRA;
        WBd = CSB * !nWRB;

END$
```

292016–9

Metastability Characteristics of Intel PLDs

THOM BOWNS
PROGRAMMABLE LOGIC APPLICATIONS
INTEL CORPORATION

3

September 1993

Metastability Characteristics of Intel PLDs

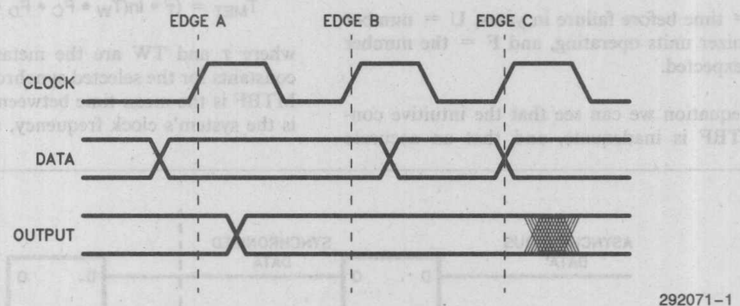
WHAT METASTABILITY IS

Edge triggered registers (otherwise known as "flip-flops") are designed to propagate and store data applied to their "D" inputs. If the data applied is HIGH just before the clock edge, the Q output transitions to HIGH. If the data applied is LOW just before the clock edge, the Q output transitions to LOW. These are the two normal states for a register. However, registers may be forced into a "metastable" state, in which the output either oscillates or simply remains in between a HIGH and a LOW for a prolonged period. This can occur when the register's setup or hold parameters are violated; that is, when data input to the register transitions too close to the clock edge. Figure 1 shows the three possibilities of when data may arrive with reference to the system clock, and when metastability may occur.

HOW METASTABILITY AFFECTS SYSTEM DESIGN

Most systems have the capability to read input data from an asynchronous source such as a keyboard or a modem. They are called asynchronous because the timing of the data from these sources is not in synchronization with the system clock. This type of data must first be synchronized before the system can use it; this usually means placing a synchronization register stage between the asynchronous data source and the rest of the system. Because the data is asynchronous, it inevitably zation register at some time during normal operation and drives the register into a metastable state. Once in the metastable state, the synchronization register eventually resolves to either a HIGH or LOW. How easy the register can be driven into, and how long it remains in the metastable state depends upon noise, ambient conditions, and the register's process technology. For example, FAST* TTL is more immune to and resolves more quickly from a metastable state than LS TTL.

In some older technologies, register outputs are fed directly to the device pin with no intermediate amplification stage. When one of these registers enters a metastable state, the voltage at the output pin can be seen to oscillate or hover in between HIGH and LOW. Intel CMOS PLDs have high gain buffers between the register circuitry and the output pin. The output pins will always be at one rail or the other, and therefore will never show an in-between or oscillatory state. Instead, they manifest metastability by a late transition: when metastable, the output transitions appreciably later than allowed by the normal clock to output delay (T_{CO}) specification of the device. To guard against the effects of metastability, one designs the system to wait a sufficient time after the register's specified T_{CO} to ensure valid data from the register. This additional wait time after T_{CO} is called T_{MET}. The designer uses the device's supplied metastability characteristics, chooses a Mean Time Between Failures (MTBF) value that meets the target system requirements, and then calculates a T_{MET} based upon that MTBF.



Edge A: Data changes before clock; normal output transition
Edge B: Data changes after clock; no output transition
Edge C: Data changes with clock; output goes metastable

Figure 1. Synchronization Data vs. Clock Timing

*FAST is a trademark of Fairchild Semiconductor Corporation.

Since metastability is a probabilistic quantity, one cannot simply say that after a given T_{MET} the register is absolutely guaranteed to have resolved, but rather we refer to the probability that the register will have resolved. Further, since MTBF is exponential in nature, the failure curve is greatly skewed toward early failures. For instance, say a given register claims an MTBF of 100 years for a given T_{MET}. Intuitively, we would expect a 50% probability of a failure in the first 100 years. However, the probability is actually 63.2% that the register will manifest a resolution failure in the first 100 years. Equation 1 gives a very close approximation of the probability of failure based on the MTBF of each synchronizer, the number of systems in use, the number of synchronizers on each system, the length of time in service, and the number of failures allowable in that time. As an example, given ten systems that each have five synchronizers with MTBFs of 1000 years, what is the possiblity of one failure in five years? Using equation 1 and solving for P (Probability):

Equation 1

$$P = 1 - (e^{(-T/MTBF)} ** (U/F))$$

$$P = 1 - (e^{(-5/1000)} ** (50/1))$$

$$P = 1 - (e^{(-0.005)} ** 50)$$

$$P = 1 - (0.995 ** 50)$$

$$P = 1 - (0.775)$$

$$P = 0.221 = 22.1\%$$

Where T = time before failure in years, U = number of synchronizer units operating, and F = the number of failures expected.

From this equation we can see that the intuitive concept of MTBF is inadequate, and that an accurate failure prediction algorithm is necessary. The concept of MTBF is very complicated and may seem unnecessarily technical, but it is essential to know what you're getting when a PLD manufacturer claims 100 years MTBF; that's for one synchronizer alone. Adding more synchronizers increases the probability of failure that much more.

Figure 2 shows the simplified diagram of a synchronization register feeding the rest of the system, which is shown here as simply another register. The minimum clock period for a single stage synchronization scheme such as this is given by equation 2. The clock period cannot be any shorter than the maximum TCO of the synchronization register plus the maximum TSU of the system plus TMET for the given system conditions.

Equation 2 solves for the margin afforded by a given clock frequency.

Equation 2

$$\text{Margin} = 1/F_C - (T_{SU} + T_{CO} + T_{MET})$$

where F_C is the system clock frequency, T_{SU} is the system's input data setup to clock edge minimum time, T_{CO} is the synchronization regsister's clock to output delay, and T_{MET} is the additional time after T_{CO} that the designer is willing to wait. Equation 3 allows the designer to determine what sort of T_{MET} he can expect for a chosen MTBF.

Equation 3

$$T_{MET} = (\tau \bullet \ln(T_W \bullet F_C \bullet F_D \bullet MTBF)) - T_{CO}$$

where τ and TW are the metastability characteristic constants for the selected synchronization register type, MTBF is the mean time between failures expected, F_C is the system's clock frequency, and F_D is the average

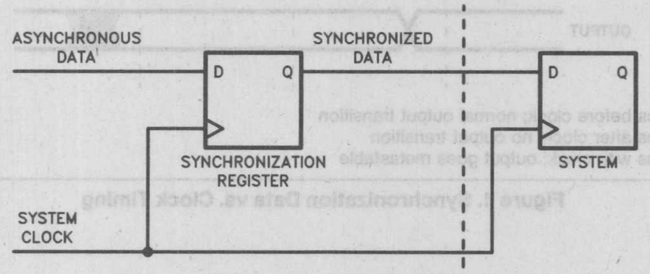


Figure 2. Single-Stage Synchronizer

data rate coming into the synchronization register. Equation 4 was derived from equation 3 to solve for MTBF when T_{MET} is chosen and the other factors are known.

Equation 4

$$\mathrm{MTBF} = \frac{e^{\left(\frac{T_{MET} + T_{CO}}{\tau}\right)}}{T_W \bullet F_C \bullet F_D}$$

It is important to note that each register within an Intel PLD is independent; if one register should go metastable, other registers within the device are not affected. Thus if several macrocell or input registers are used in parallel as a byte-wise synchronizer array, one need not be concerned about one register affecting the data in another register. The only problem that may arise would be if the incoming data bytes had some timing skew between the bits that make it up. If one input data bit transitioned later than the others, driving it's synchronizer into metastability, the worst case scenario would be that the system would sample the synchronizers before that register settled. That would mean that the data at that point would most likely be invalid, and the next sampled data byte might also be invalid. However, with a sufficient T_{MET} to allow for metastable settling, the probability of this occurrence can be reduced to a managable level.

HOW METASTABILITY IS QUANTIFIED

Each device has two metastability characteristic constants, τ (or "Tau") and T_W, which are used to determine the probability of metastable occurrences. As shown in Figure 3, this probability decreases at an exponential rate, according to the value of τ. T_W defines the likelihood that the register will enter the metastable state in the first place; it is also known as the "failure window". Given τ and T_W, T_{MET} can be calculated for a chosen MTBF, according to equation 3.

The metastability constants are determined by running the register under test through billions of clock cycles with randomly changing input data. For each increment of T_{MET}, the number of late transitions are counted within a given time period. A late transition is when the delay from the clock edge until when the register's output changes takes longer than it's observed T_{CO} allows; we interpret that as an occurrence of a metastable event. The number of failures recorded for each increment of T_{MET} is logged and then run through the following equations, producing τ and T_W.

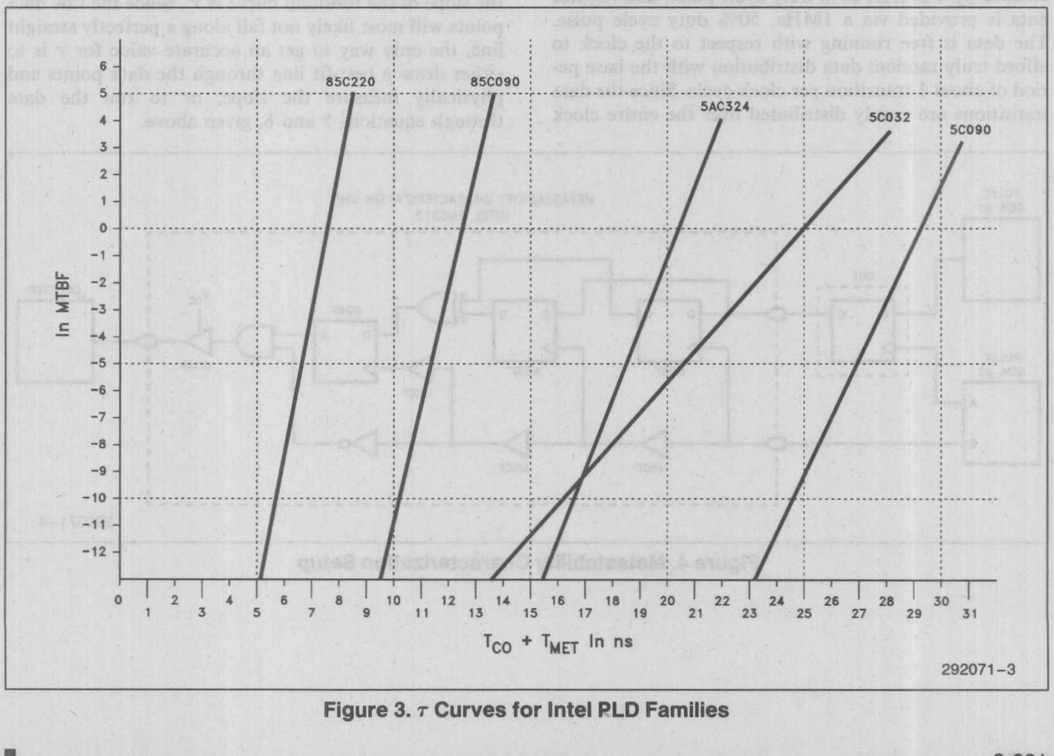


Figure 3. τ Curves for Intel PLD Families

Equation 5

$$\tau = \frac{n \sum_{i=1}^{n} Xi^2 - \left(\sum_{i=1}^{n} Xi\right)^2}{n \sum_{i=1}^{n} Xi\,Yi - \left(\sum_{i=1}^{n} Xi\right)\left(\sum_{i=1}^{n} Yi\right)}$$

Equation 6

$$T_W = \frac{\sum_{i=1}^{n} \left(\dfrac{N_i \bullet e^{\left(\frac{T_{CO} + T_{MET}}{\tau}\right)}}{Nc_i \bullet F_C} \right)}{n}$$

The X axis is scaled as the $T_{CO} + T_{MET}$ value in nanoseconds, and the Y axis is the Natural logarithm of the number of seconds between failures (actual number of failures recorded divided into the amount of time taken to accumulate those failures). X_i and Y_i are the delay value and log of the failures, respectively, at point i. N_i is the number of events recorded at point i, and N_{ci} is the number of clock pulses which occurred within that time.

When plotted on semi-log paper, the resulting line shows the τ slope. The Y-axis intercept point is related to T_W.

Metastable failure characteristics for each PLD are ascertained by using the setup in Figure 4. The register is clocked by a 2MHz, 25% duty cycle pulse, and register data is provided via a 1MHz, 50% duty cycle pulse. The data is free running with respect to the clock to afford truly random data distribution with the base period of about 1 transition per clock cycle. Since the data transitions are evenly distributed over the entire clock period, we may assume that the data transitions are also evenly distributed within the failure window (violating setup and hold). The register under test or DUT (device under test) clock is provided by the first output of a dual pulse generator. The second output is delayed by $T_{CO} + T_{MET}$ and fed into the metastable characterization unit. The output of the DUT is thus sampled at $T_{CO} + T_{MET}$, and it is sampled again aproximately 100 ns later. If the two samples disagree, the DUT must have transitioned after $T_{CO} + T_{MET}$, and therefore must have been metastable. For each metastable event detected, a pulse is generated to increment the event counter. In about half of the cases, the DUT may enter the metastable state and resolve to the same logic level as before, and so not give an external indication of metastability. However, since cases like this will not affect system performance, they are not figured into the MTBF equations.

To run the test, T_{CO} is characterized for ambient conditions and used as a base delay. The first test begins, and the counter catches X metastable failure events for 60 seconds. The number of metastable failures is recorded for that particular T_{MET}. T_{MET} is increased by .2 nS and another X events are counted for 60 seconds. This is continued until the events get spaced out to where less than 100 events occur in 60 seconds, and the remaining data points are arrived at by counting 100 events for X seconds and recording the results appropriately. The results are plotted on semi-log paper, and the slope of the resultant curve is τ . Since the raw data points will most likely not fall along a perfectly straight line, the only way to get an accurate value for τ is to either draw a best-fit line through the data points and physically measure the slope, or to run the data through equations 5 and 6, given above.

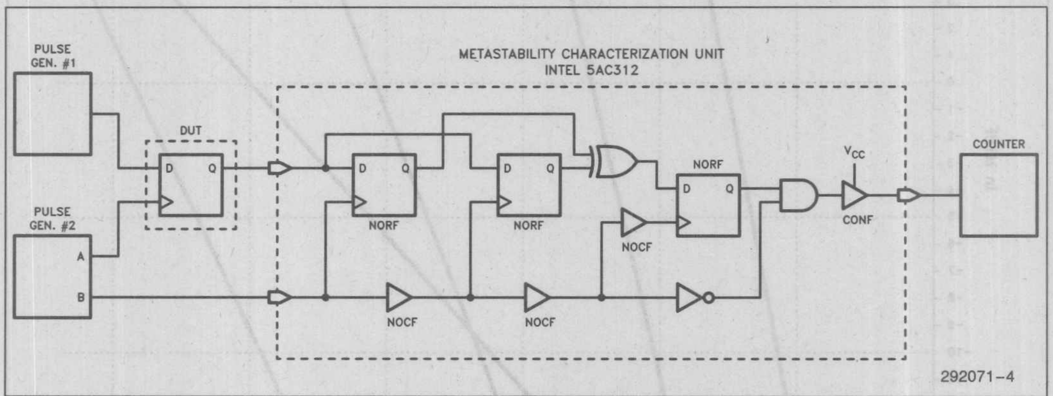


Figure 4. Metastability Characterization Setup

METASTABILITY DATA FOR INTEL PLDs

Intel PLDs are based upon fast, CMOS EPROM process technologies which make them inherently resilient against metastability. The metastability characteristics for each device are dependent upon its design and process technology, thus all Intel PLDs within a given family have similar metastable characteristics.

The metastability characteristic constants for each Intel PLD are shown in Table 1. Corresponding metastability characteristic curves for each family are shown in Figure 3.

HOW INTEL PLDs COMPARE AGAINST OTHER PLDS

The first half of Table 2 lists maximum allowable clock frequencies for a single-stage synchronization scheme for various PLDs. This determination comes from a derivation of equations 2 and 3, with the margin set for 0 nanosecond. The other factors are calculated to give a resulting maximum clock frequency. The second half of Table 2 shows the T_{MET} values that achieve different MTBF levels for several PLD technologies. The metastability characteristics of the other PLDs were determined empirically using the same bench testing method as the Intel PLDs. It is easy to see that Intel PLDs have very good metastable resolution characteristics when compared against other technologies.

Table 1. Intel PLD Metastability Characteristic Constants

Device	τ	T_W
5C031	0.82 ns	5.8×10^{2}
5C032	0.86 ns	2.4×10^{-2}
5C060	0.90 ns	4.0×10^{0}
5C090	0.44 ns	2.0×10^{14}
5AC312	0.42 ns	1.4×10^{4}
5AC324	0.35 ns	8.6×10^{10}
5AC324 (Input Registers)	0.39 ns	3.0×10^{19}
85C220	0.22 ns	5.2×10^{1}
85C224	0.24 ns	4.4×10^{1}
iPLD610	0.39 ns	1.1×10^{-1}
iPLD910	0.28 ns	1.5×10^{6}
iPLD22V10/85C22V10	0.43 ns	3.24×10^{10}

Table 2. Maximum Clock Frequencies for Sampled PLDs

Margin = 0 ns, FD = 4 MHz — **Maximum Clock Frequency for a Chosen MTBF** (Based on Equations 2 and 3)

MTBF	Device: 5C032-30	5AC312-25	85C220-80	16V8A-10	16R6-7	iPLD910-15
1 Yr	16 MHz	22 MHz	53 MHz	46 MHz	26 MHz	34 MHz
10 Yrs	15 MHz	22 MHz	51 MHz	45 MHz	24 MHz	34 MHz
100 Yrs	15 MHz	21 MHz	50 MHz	44 MHz	23 MHz	33 MHz
1000 Yrs	15 MHz	21 MHz	49 MHz	43 MHz	21 MHz	32 MHz

FC = 33 MHz, FD = 4 MHz — **MTBFs for a Given T_{MET}** (Based on Equation 3)

MTBF	Device: 5C032-30	85C220-80	16V8A-10	16R6-7	iPLD910-15
1 Yr	22.1 ns	6.3 ns	3.9 ns	25.1 ns	8.9 ns
10 Yrs	24.1 ns	6.8 ns	4.3 ns	27.7 ns	9.6 ns
100 Yrs	26.1 ns	7.3 ns	4.6 ns	30.2 ns	10.2 ns
1000 Yrs	28.0 ns	7.8 ns	5.0 ns	32.7 ns	10.8 ns

3

Every dynamic system which has two stable states can enter a metastable state. Each PLD technology has a metastable characteristic associated with it, and some are less susceptible to metastability than others. By using Intel CMOS PLDs and knowing how to effectively guard against the effects of metastability, systems may be designed to be virtually trouble-free.

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uary 1989

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ACKNOWLEDGEMENTS

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PLD Quality and Reliability Data Summary

November 1992

Order Number: 293003-004

PLD QUALITY AND RELIABILITY DATA SUMMARY

CONTENTS PAGE

CONTENTS PAGE

THE IMPORTANCE OF RELIABILITY

Reliabilty of the erasable programmable logic devices (EPLDs) in your end product is critical to your total system reliability. The use of Intel EPLDs can make a difference. Intel EPLDs are manufactured on patented EPROM processes with proven reliability.

Quality ≠ Reliability

A quality component is one that meets your specification when received and tested. A reliable component continues to meet your specification even years after you have shipped your product. While Intel is a quality leader, we also adhere to stringent reliability standards which we have established for ourselves.

Consider Quality vs Reliability

The true cost of any component involves more than just the purchase price. The true component cost encompasses the initial purchase price, cost of rework during system production, and the cost of field repairs due to component failures. "Rework" costs during system production are incurred prior to shipment of your end product, and are a function of the quality of the component you purchase.

Repair costs incurred in the field after end product shipments, are a function of the reliability of the components. In addition to the increasing real cost of a system field service call, there is the intangible cost of a poor reliability reputation to the end user of your product. These costs depend upon the reliability of the components you purchase. Thus, reliability may impact costs during the system lifetime more than the initial quality of the components!

The Roots of Reliability

The manufacture of a reliable semiconductor device using a modern technology is a dynamic and evolutionary process. Success of this process is highly dependent upon the interplay between knowledgable and experienced manufacturing engineers, materials physicists, and responsible/responsive management. Only the correct combination can consistantly deliver high volumes of a reliable product. In this model, the experienced process engineer selects and defines the stresses to be performed and the performance criteria to be met, utilizing appropriate statistical tools and limits. The materials physicist then determines the root cause of the failure, if and when failure occurs, and provides effective solutions and/or containment recommendations. Finally, management provides the resources for the entire process from initial monitor to root cause corrective action.

Monitor Program

Reliability is designed into each component Intel manufactures. From the moment the design is put to paper, stringent reliability standards must be met at each step for a product to bear the Intel name.

Designing-in reliability, however, is only the beginning. Ongoing tests must be conducted to ensure that the original reliability specifications remain as valid in volume production as they were when the device was first qualified.

Intel's Reliability Monitor Program, devised to measure and control device reliability in production, is a proven tool that Intel has used for seven years and is now available to its customers. The Monitor Program subjects all of Intel's technologies to a 48 hour dynamic burn-in at 125°C (with a portion of these devices continued for a 1000 hour lifetest) and provides answers about device reliability that are not generally available from limited testing programs. But it's much more than burn-in and device testing. When test rejects are encountered, failure analysis is performed on each failed part. Isolating the fault and determining the failure mechanism is a critical part of the Monitor Program. It is the most comprehensive reliability program anywhere.

The paramount objective is to deliver reliable, quality devices. Actions that Intel takes to meet this objective may include a process or design change, or added reliability screen. Each decision is made with our customers in mind so that they receive the parts–and the performance–that they ordered by specifying Intel. Reliability qualification assures that all new production meets Intel's reliability standards. The Reliability Monitor Program ensures that these high standards are continually maintained, day in, day out, over the duration of a device's life. This reliability improves the life-time reputation of your product, reducing the required number of field service calls.

EPLD RELIABILITY DATA SUMMARY

Intel routinely publishes this "EPLD Reliability Data Summary", a continuing update of reliability information covering Intel's EPLD product line. This document includes a discussion on EPLD reliability testing methodology and the most current failure rate calculations, failure analysis and lifetest results. The "EPROM Reliability Data Summary" (order number: 210473 and 293004) should be used as a supplement to monitor EPROM process reliability.

Intel's commitment to the reliability of our products is clearly reflected in the information we make available to customers. We believe that supplying detailed reliability information to our customers is part of the total solution Intel offers, and is an important part of Intel's leadership in microelectronics technology.

EPLD Reliability Testing

Intel EPLDs undergo comprehensive testing to insure electrical reliability. This testing is done at qualification and/or during ongoing monitor checks. Testing differences between plastic and ceramic packaged EPLDs are noted.

Intel continually reviews its testing procedures and makes improvements to its methodology whenever overall reliability can be enhanced. Our goal is to be the industry leader in delivering high-quality, reliable parts.

Information on Intel's reliability testing procedures follows.

High Temperature 5.25V Dynamic Lifetest—This test is used to accelerate failure mechanisms by operating the devices at an elevated temperature of 125°C and nominal V_{CC}. During the test the device is programmed as a counter, with the inputs and outputs exercised, but not monitored or loaded. A pattern with greater than 90% of the EPROM cells programmed is used to simulate random customer patterns expected during actual use. Results of the lifetest have been summarized along with the failure analysis. Table 1 lists the activation energies for various failure mechanisms. These activation energies are used to calculate the amount of acceleration due to increased stress temperature or voltage (see Appendix A for failure rate calculations).

In order to best determine long-term failure rate, all devices used for lifetesting are first subjected to standard INTEL testing. The 48 hour burn-in results are an indication of infant mortality. These results are not included in the failure rate calculation. (See Figure 1 for typical lifetest bias and time diagrams.)

Table 1. Failure Mechanism Activation Energies

Failure Mechanism	E_a (ev)
Oxide	0.3
Fab/Assembly Defect	0.5
SBCL/SBCG/MBCL/MBCG	0.6
Contamination	1.0
Speed Degradation	0.3–1.0
Intrinsic Charge Loss	1.4

Failure Definitions

Oxide—An Oxide Failure Related Fault
SBCL—Single Bit Charge Loss
SBCG—Single Bit Charge Gain
MBCL—Multiple Bit Charge Loss
MBCG—Multiple Bit Charge Gain
Contamination—Ionic Contamination Failure
Speed Degradation—Device Speed Degraded Over Test

Failure Rate Calculations—Failure rate calculations are given for each relevant activation energy. Failure rate calculations are made using the appropriate energy (1, 2, 3, 4) and the Arrhenius Plot as shown in Figure 2. The total equivalent device hours at a given temperature can be determined. The failure rate is then calculated by dividing the number of failures by the equivalent device hours and is expressed as a %/1000 hours. To arrive at a confidence level associated failure rate, the failure rate is adjusted by a factor related to the number of device hours using a chi-square distribution. A conservative estimate of the failure rate is obtained by including zero failures at 0.3 eV. Appendix A provides example failure rate calculations.

High Temperature, High Voltage Dynamic Lifetest—This test is used to accelerate oxide breakdown failures. The test setup is identical to the one used for the dynamic lifetest except V_{CC} is an elevated voltage. The acceleration factor due to this test can be found in Appendix A. This data plus the standard dynamic lifetest data are used to calculate the 0.3 eV failure rate.

High Temperature Storage—This test is used to accelerate charge loss/gain from the EPROM floating gate. The test is performed by subjecting devices containing a 90%+ programmed pattern to a 250°C bake (140°C for plastic) with no applied bias. In addition to EPROM cell integrity, this test is used to detect mechanical reliability problems (e.g., bond strength) and process stability. This test is sometimes referred to as Data Retention Bake Test.

Temperature Cycle—This test consists of cycling the temperature of the chamber housing the subject devices from −65°C to +150°C and back. The device is functionally tested before and after the stress. In addition, hermetic packages have fine/gross leak readouts. This test is to detect mechanical reliability problems and microcracks.

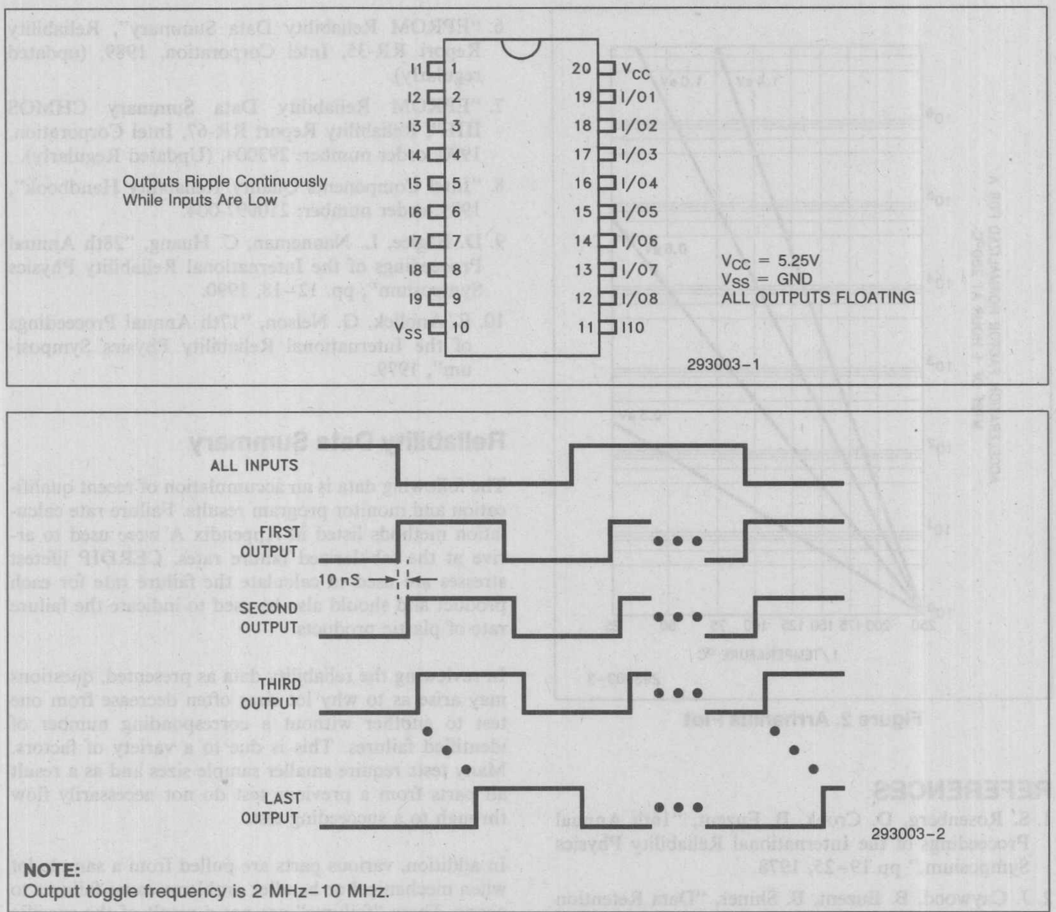

Figure 1. EPLD Lifetest/Burn-In Bias and Timing Diagram (85C220 Used as Example)

85/85 Humidity—High temperature/humidity testing is performed to evaluate moisture resistance characteristics of plastic-encapsulated components. A 2000-hour test is performed under static bias conditions at 85°C/85 percent relative humidity with nominal voltages. To maximum metal corrosion conditions, the biasing configuration is either under low power or no power, with alternate pins biased at +5V or 0V.

Steam—This test consists of exposing parts to water vapor at 121°C and at 2 atmospheres. The devices are functionally tested before and after the test. This test is used to highly accelerate failure mechanisms effecting the bonds, bond pads, and passivation.

ESD Testing—This test is performed to validate the products tolerance to Electro Static Discharge damage. All products incorporate ESD protection networks where needed to ensure the Intel corporate goals of military and charged device ESD testing are met. The military test uses the MIL STD 883 test criteria, while the charged device testing is performed to further validate protection occurring during mechanical handling.

Programmability—Device programmability is routinely monitored through the process of programming the devices for product monitors and qualifications Programmability is a distinct part of a product qualification. All voltage combinations are verified. Program margin is measured and tested on ≥90% of Intel EPLD EPROM cells.

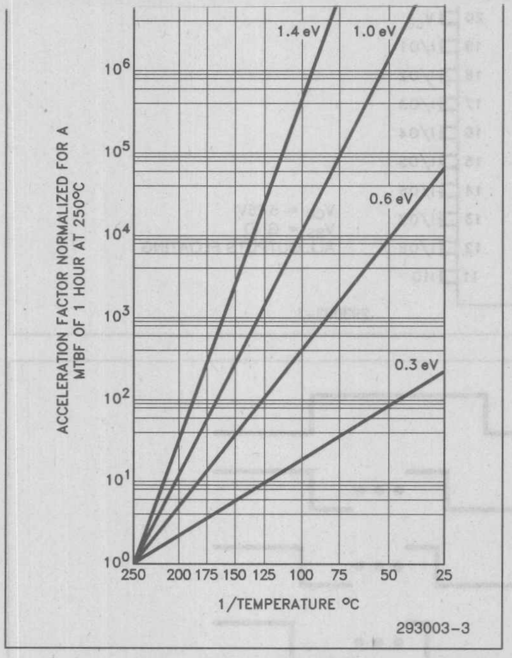

Figure 2. Arrhenius Plot

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Reliability Data Summary

The following data is an accumulation of recent qualification and monitor program results. Failure rate calculation methods listed in Appendix A were used to arrive at the tabularized failure rates. CERDIP lifetest stresses are used to calculate the failure rate for each product and should also be used to indicate the failure rate of plastic products.

In reviewing the reliability data as presented, questions may arise as to why lot sizes often decrease from one test to another without a corresponding number of identified failures. This is due to a variety of factors. Many tests require smaller sample sizes and as a result all parts from a previous test do not necessarily flow through to a succeeding test.

In addition, various parts are pulled from a sample lot when mechanical or handler problems cause failures to occur. These "failures" are not a result of the specific test just completed. They are removed from the sample lot size and are not included in any failure rate calculation. It can also happen that a particular test is done incorrectly through human error or faulty test equipment and these suspected "invalid" failures are put aside for retesting at a later date, decreasing the lot size for a succeeding test. If these parts are found to be truly defective, they are treated as failures and listed. If they test out properly, they are removed from any calculation data base.

Organization:	10 Macrocells
Pinout:	24 Lead, 300 mil CERDIP and PDIP; 28 Lead PLCC
Die Size:	108 x 123 mils
Transistor Count:	~ 13K
Process:	CHMOS IIIE, P629.5
Programming Voltage:	12.5V
Technology:	CMOS

Table 1. Reliability Data

Package	Burn-In 48 Hours	125°C Dynamic Lifetest		
		168 Hours	500 Hours	1K Hours
CERDIP	1/334	0/333	0/170	
PLCC	0/504	0/504		
TOTALS	1/838 A	0/837	0/170	

Package	125°C High Voltage Dynamic Lifetest (6.5V)		
	48 Hours	168 Hours	500 Hours
CERDIP	0/1819	0/1818	0/168
PDIP	0/336	0/336	
PLCC	0/814	0/814	
TOTALS	0/2969	0/2968	0/168

Package	Data Retention Bake (CERDIP @ 250°C, PDIP @ 140°C)		
	168 Hours	500 Hours	1K Hours
CERDIP	0/62		
PLCC	0/62		
TOTALS	0/124		

Table 2. Additional Qualification Stress Information

Package	Temperature Cycling (Condition "C"—150°C to −65°C)		
	200 Cycles	500 Cycles	1K Cycles
CERDIP	0/62		
PDIP	0/62		
PLCC	0/62		
TOTALS	0/186		

Package	85°C/85% Relative Humidity		
	168 Hours	500 Hours	1K Hours
PDIP	0/124		
PLCC	0/126		
TOTALS	0/250		

Package	Steam (121°C, 2 ATM)	
	96 Hours	168 Hours
PDIP	0/62	0/62
PLCC	0/62	0/62
TOTALS	0/124	0/124

Table 3. Failure Rate Predictions (CERDIP 85C22V10)

Actual Device Hrs	Ea (eV)	Equivalent Device Hrs 55°C	Equivalent Device Hrs 70°C	# Fail	Fail Rate in FITs (60% UCL) 55°C	Fail Rate in FITs (60% UCL) 70°C
9.54E + 4	0.3 LT	5.0E + 5	3.3E + 5			
2.66E + 5	0.3 HVLT * VAF	3.7E + 7	2.5E + 7			
		Total 0.3 eV Failures =		0	0	0
9.54E + 4	0.5 LT	1.5E + 6	7.6E + 5			
2.66E + 5	0.5 HVLT	4.6E + 6	2.2E + 6			
		Total 0.5 eV Failures =		0	158	312
9.54E + 4	0.6 LT	2.6E + 6	1.2E + 6			
2.66E + 5	0.6 HVLT	7.5E + 6	3.3E + 6			
		Total 0.6 eV Failures =		0	0	0
9.54E + 4	1.0 LT	2.4E + 7	6.1E + 6			
2.66E + 5	1.0 HVLT	6.8E + 7	1.8E + 7			
		Total 1.0 eV Failures =		0	0	0
		Combined Failure Rate (FITs) =			158	312
		48 Hour BI Infant Mortality = 1/2153 = 0.046%				

Table 4. Failure Rate Predictions (PDIP 85C22V10)

Actual Device Hrs	Ea (eV)	Equivalent Device Hrs		# Fail	Fail Rate in FITs (60% UCL)	
		55°C	70°C		55°C	70°C
6.0E + 4 1.4E + 5	0.3 LT 0.3 HVLT * VAF	3.0E + 5 1.9E + 7	2.0E + 5 1.2E + 7			
		Total 0.3 eV Failures =		0	0	0
6.0E + 4 1.4E + 5	0.5 LT 0.5 HVLT	9.0E + 5 2.1E + 6	4.6E + 5 1.1E + 6			
		Total 0.5 eV Failures =		0	306	595
6.0E + 4 1.4E + 5	0.6 LT 0.6 HVLT	1.5E + 6 3.6E + 6	6.9E + 5 1.6E + 6			
		Total 0.6 eV Failures =		0	0	0
6.0E + 4 1.4E + 5	1.0 LT 1.0 HVLT	1.3E + 7 3.1E + 7	3.5E + 6 8.3E + 6			
		Total 1.0 eV Failures =		0	0	0
		Combined Failure Rate (FITs) =			306	595
48 Hour BI Infant Mortality = 0/1654 = 0.00%						

Table 5. Failure Rate Predictions (CERDIP and PDIP Combined Data 85C22V10)

Actual Device Hrs	Ea (eV)	Equivalent Device Hrs		# Fail	Fail Rate in FITs (60% UCL)	
		55°C	70°C		55°C	70°C
1.6E + 5 4.0E + 5	0.3 LT 0.3 HVLT * VAF	8.1E + 5 5.3E + 7	5.4E + 5 3.5E + 7			
		Total 0.3 eV Failures =		0	0	0
1.6E + 5 4.0E + 5	0.5 LT 0.5 HVLT	2.4E + 6 6.0E + 6	1.2E + 6 3.1E + 6			
		Total 0.5 eV Failures =		0	109	213
1.6E + 5 4.0E + 5	0.6 LT 0.6 HVLT	4.1E + 6 1.0E + 7	1.9E + 6 4.6E + 6			
		Total 0.6 eV Failures =		0	0	0
1.6E + 5 4.0E + 5	1.0 LT 1.0 HVLT	3.6E + 7 9.0E + 7	9.5E + 6 2.4E + 7			
		Total 1.0 eV Failures =		0	0	0
		Combined Failure Rate (FITs) =			109	213
48 Hour BI Infant Mortality = 1/3807 = 0.026% = 532 DPM @ 60% Confidence						

Theta Ja =	50°C/W	**Temp with Theta Ja Degree Kelvin**	
Theta Jc =	19°C/W		
V_{CC} =	5.25V	T(55°C) =	349.5 K
I_{CC} @ 55°C =	75 mA	T(70°C) =	364.5 K
I_{CC} @ 70°C =	75 mA	T(125°C) =	419.5 K
I_{CC} @ 125°C =	75 mA	T(250°C) =	544.5 K

Boltzman's Constant = K = 8.62×10^{-5} eV/K

Thermal Acceleration Factors—

Lifetest (LT) and High Voltage Lifetest (HVLT)			Bake (250°C)		
Activation Energy	**55°C**	**70°C**	**Activation Energy**	**55°C**	**70°C**
0.3	5.26	3.49	0.3	n/a	n/a
0.5	15.9	8.04	0.5	730	337
0.6	27.7	12.2	0.6	2730	1080
1.0	253	64.7	1.0	n/a	n/a

Other Data (PDIP)

Theta Ja =	66°C/W	**Temp with Theta Ja Degree Kelvin**	
Theta Jc =	21°C/W		
V_{CC} =	5.25V	T(55°C) =	354 K
I_{CC} @ 55°C =	75 mA	T(70°C) =	369 K
I_{CC} @ 70°C =	75 mA	T(125°C) =	424 K
I_{CC} @ 125°C =	75 mA	T(250°C) =	549 K

Boltzman's Constant = K = 8.62×10^{-5} eV/K

Thermal Acceleration Factors—

Lifetest (LT) and High Voltage Lifetest (HVLT)			Bake (140°C)		
Activation Energy	**55°C**	**70°C**	**Activation Energy**	**55°C**	**70°C**
0.3	5.07	3.40	0.3	n/a	n/a
0.5	15.0	7.68	0.5	730	337
0.6	25.7	11.6	0.6	2730	1080
1.0	224	59.1	1.0	n/a	n/a

Other Data (PLCC)

Theta Ja =	65°C/W	**Temp with Theta Ja Degree Kelvin**	
Theta Jc =	21°C/W		
V_{CC} =	5.25V	T(55°C) =	354 K
I_{CC} @ 55°C =	75 mA	T(70°C) =	369 K
I_{CC} @ 70°C =	75 mA	T(125°C) =	424 K
I_{CC} @ 125°C =	75 mA	T(250°C) =	549 K

Boltzman's Constant = K = 8.62×10^{-5} eV/K

Thermal Acceleration Factors—

Lifetest (LT) and High Voltage Lifetest (HVLT)			Bake (140°C)		
Activation Energy	**55°C**	**70°C**	**Activation Energy**	**55°C**	**70°C**
0.3	5.07	3.40	0.3	n/a	n/a
0.5	15.0	7.68	0.5	730	337
0.6	25.7	11.6	0.6	2730	1080
1.0	224	59.1	1.0	n/a	n/a

Failure Analysis

A. ISB failure, destroyed in analysis.

85C220

Device:	85C220
Organization:	8 Macrocells
Pinout:	24 Lead, 300 mil CERDIP and PDIP; 20 Lead PLCC
Die Size:	89 x 90 mils
Transistor Count:	~7K
Process:	CHMOS IIIE, P629.5
Programming Voltage:	12.5V
Technology:	CMOS

Table 1. Reliability Data

Package	Burn-In 48 Hours	125°C Dynamic Lifetest		
		168 Hours	500 Hours	1K Hours
CERDIP PDIP	0/2050 0/1995	0/2050 0/1995	0/270 0/485	0/270 0/270
TOTALS	0/4045	0/4045	0/755	0/540

Additional Readouts:
- CERDIP 0/90 @ 2K Hours Lifetest
- PDIP 0/180 @ 2K Hours Lifetest

Package	125°C High Voltage Dynamic Lifetest (6.5V)			
	48 Hours	168 Hours	500 Hours	1K Hours
CERDIP PDIP	0/2048 0/400	0/2048 0/399	0/270 0/299	0/90 0/199
TOTALS	0/2448	0/2447	0/569	0/289

Additional Readouts:
- CERDIP 0/90 @ 2K Hours Lifetest
- PDIP 0/199 @ 2K Hours Lifetest

Package	Data Retention Bake (CERDIP @ 250°C, PDIP @ 140°C)		
	168 Hours	500 Hours	1K Hours
CERDIP PDIP	0/300 0/300	0/300 0/300	
TOTALS	0/600	0/600	

Table 2. Additional Qualification Stress Information

Package	Temperature Cycling (Condition "C"—150°C to −65°C)		
	500 Cycles	**1K Cycles**	**2K Cycles**
CERDIP	0/90	0/89	0/89
PDIP	0/150	0/150	0/150
PLCC	0/78	0/78	
TOTALS	0/318	0/317	0/239

Package	85°C/85% Relative Humidity		
	500 Hours	**1K Hours**	**2K Hours**
PDIP	0/98	0/98	0/48
PLCC	0/30	0/30	
TOTALS	0/128	0/128	0/48

Package	Steam (121°C, 2 ATM)		
	168 Hours	**336 Hours**	**500 Hours**
PDIP	0/300	0/300	0/300
PLCC	0/100	0/100	
TOTALS	0/400	0/400	0/300

3

Table 3. Failure Rate Predictions (CERDIP 85C220)

Actual Device Hrs	Ea (eV)	Equivalent Device Hrs		# Fail	Fail Rate in FITs (60% UCL)	
		55°C	**70°C**		**55°C**	**70°C**
5.6E + 5	0.3 LT	3.2E + 6	2.1E + 6			
5.6E + 5	0.3 HVLT * VAF	8.3E + 7	5.4E + 7			
		Total 0.3 eV Failures =		0	0	0
5.6E + 5	0.5 LT	1.0E + 7	4.98E + 6			
5.6E + 5	0.5 HVLT	1.0E + 7	4.98E + 6			
		Total 0.5 eV Failures =		0	44	91
5.6E + 5	0.6 LT	1.8E + 7	7.7E + 6			
5.6E + 5	0.6 HVLT	1.8E + 7	7.7E + 6			
		Total 0.6 eV Failures =		0	0	0
5.6E + 5	1.0 LT	1.9E + 8	4.4E + 7			
5.6E + 5	1.0 HVLT	1.9E + 8	4.4E + 7			
		Total 1.0 eV Failures =		0	0	0
		Combined Failure Rate (FITs) =			44	91
		48 Hour BI Infant Mortality = 0/4098 = 0.00%				

Table 4. Failure Rate Predictions (PDIP 85C220)

Actual Device Hrs	Ea (eV)	Equivalent Device Hrs		# Fail	Fail Rate in FITs (60% UCL)	
		55°C	70°C		55°C	70°C
7.20E + 5 5.0E + 5	0.3 LT 0.3 HVLT * VAF	4.0E + 6 7.2E + 7	2.6E + 6 4.7E + 7			
		Total 0.3 eV Failures =		0	0	0
7.20E + 5 5.0E + 5	0.5 LT 0.5 HVLT	1.2E + 7 8.6E + 6	6.1E + 6 4.25E + 6			
		Total 0.5 eV Failures =		0	44	88
7.20E + 5 5.0E + 5	0.6 LT 0.6 HVLT	2.2E + 7 1.5E + 7	9.4E + 6 6.5E + 6			
		Total 0.6 eV Failures =		0	0	0
7.20E + 5 5.0E + 5	1.0 LT 1.0 HVLT	2.1E + 8 1.5E + 8	5.2E + 7 3.6E + 7			
		Total 1.0 eV Failures =		0	0	0
		Combined Failure Rate (FITs) =			44	88
			48 Hour BI Infant Mortality = 0/2395 = 0.00%			

Table 5. Failure Rate Predictions (CERDIP and PDIP Combined Data)

Actual Device Hrs	Ea (eV)	Equivalent Device Hrs		# Fail	Fail Rate in FITs (60% UCL)	
		55°C	70°C		55°C	70°C
1.3E + 6 1.1E + 6	0.3 LT 0.3 HVLT * VAF	7.0E + 6 1.5E + 8	4.6E + 6 1.0E + 8			
		Total 0.3 eV Failures =		0	0	0
1.3E + 6 1.1E + 6	0.5 LT 0.5 HVLT	2.2E + 7 1.8E + 7	1.1E + 7 9.0E + 6			
		Total 0.5 eV Failures =		0	23	46
1.3E + 6 1.1E + 6	0.6 LT 0.6 HVLT	3.9E + 7 3.2E + 7	1.7E + 7 1.4E + 7			
		Total 0.6 eV Failures =		0	0	0
1.3E + 6 1.1E + 6	1.0 LT 1.0 HVLT	3.7E + 8 3.1E + 8	9.2E + 7 7.7E + 7			
		Total 1.0 eV Failures =		0	0	0
		Combined Failure Rate (FITs) =			23	46
		48 Hour BI Infant Mortality = 0/2225 = 0.00% = 142 DPM @ 60% Confidence				

Other Data (CERDIP)

		Temp with Theta Ja Degree Kelvin	
Theta Ja =	68°C/W		
Theta Jc =	30°C/W		
V_{CC} =	5.25V	T(55°C) =	340.5 K
I_{CC} @ 55°C =	35 mA	T(70°C) =	355.5 K
I_{CC} @ 70°C =	35 mA	T(125°C) =	410.5 K
I_{CC} @ 125°C =	35 mA	T(250°C) =	535.5 K

Boltzman's Constant = K = 8.62×10^{-5} eV/K

Thermal Acceleration Factors—

Lifetest (LT) and High Voltage Lifetest (HVLT)			Bake		
Activation Energy	55°C	70°C	Activation Energy	55°C	70°C
0.3	5.71	3.71	0.3	n/a	n/a
0.5	18.3	8.90	0.5	730	337
0.6	32.7	13.8	0.6	2730	1080
1.0	334	79.2	1.0	n/a	n/a

Other Data (PDIP and PLCC)

		Temp with Theta Ja Degree Kelvin	
Theta Ja =	90°C/W		
Theta Jc =	25°C/W		
V_{CC} =	5.25V	T(55°C) =	344.5 K
I_{CC} @ 55°C =	35 mA	T(70°C) =	359.5 K
I_{CC} @ 70°C =	35 mA	T(125°C) =	414.5 K
I_{CC} @ 125°C =	35 mA	T(250°C) =	539.5 K

Boltzman's Constant = K = 8.62×10^{-5} eV/K

Thermal Acceleration Factors—

Lifetest (LT) and High Voltage Lifetest (HVLT)			Bake		
Activation Energy	55°C	70°C	Activation Energy	55°C	70°C
0.3	5.51	3.61	0.3	n/a	n/a
0.5	17.2	8.50	0.5	730	337
0.6	30.3	13.1	0.6	2730	1080
1.0	295	72.3	1.0	n/a	n/a

Failure Analysis

N/A

85C224

Device:	85C224
Organization:	8 Macrocells
Pinout:	24 Lead, 300 mil CERDIP and PDIP; 28 Lead PLCC
Die Size:	99 x 94 mils
Transistor Count:	~ 7K
Process:	CHMOS IIIE, P629.5
Programming Voltage:	12.5V
Technology:	CMOS

Table 1. Reliability Data

Package	Burn-In 48 Hours	125°C Dynamic Lifetest		
		168 Hours	500 Hours	1K Hours
CERDIP	0/897	0/897	0/255	0/255
PDIP	0/300	0/300	0/170	0/170
TOTALS	0/1197	0/1197	0/425	0/425

Package	125°C High Voltage Dynamic Lifetest (6.5V)			
	48 Hours	168 Hours	500 Hours	1K Hours
CERDIP	0/728	1/450	0/449	0/449
PDIP	0/300	0/297	0/297	0/297
TOTALS	0/1028	1/747 (A)	0/746	0/746

Package	Data Retention Bake (CERDIP @ 250°C, PDIP @ 140°C)		
	168 Hours	500 Hours	1K Hours
CERDIP	0/300	0/300	0/300
PDIP	0/200	0/200	
TOTALS	0/500	0/500	0/300

Table 2. Additional Qualification Stress Information

Package	Temperature Cycling (Condition "C"—150°C to −65°C)		
	500 Cycles	1K Cycles	2K Cycles
CERDIP	0/90	0/90	
PDIP	0/60	0/60	
PLCC	0/60	0/60	
TOTALS	0/210	0/210	

Package	Steam (121°C, 2 ATM)		
	168 Hours	336 Hours	500 Hours
PDIP	0/200	0/200	
PLCC	0/100	0/100	
TOTALS	0/300	0/300	

Table 3. Failure Rate Predictions (CERDIP 85C224)

Actual Device Hrs	Ea (eV)	Equivalent Device Hrs		# Fail	Fail Rate in FITs (60% UCL)	
		55°C	70°C		55°C	70°C
3.2E + 5 4.3E + 5	0.3 LT 0.3 HVLT * VAF	1.9E + 6 6.5E + 7	1.2E + 6 4.2E + 7			
		Total 0.3 eV Failures =		0	30	46
3.2E + 5 4.3E + 5	0.5 LT 0.5 HVLT	6.1E + 6 8.2E + 6	2.9E + 6 3.9E + 6			
		Total 0.5 eV Failures =		1	142	294
3.2E + 5 4.3E + 5	0.6 LT 0.6 HVLT	1.1E + 7 1.5E + 7	4.6E + 6 6.1E + 6			
		Total 0.6 eV Failures =		0	0	0
3.2E + 5 4.3E + 5	1.0 LT 1.0 HVLT	1.2E + 8 1.6E + 8	2.7E + 7 3.6E + 7			
		Total 1.0 eV Failures =		0	0	0
		Combined Failure Rate (FITs) =			172	330
			48 Hour BI Infant Mortality = 0/1625 = 0.00%			

Table 4. Failure Rate Predictions (PDIP 85C224)

Actual Device Hrs	Ea (eV)	Equivalent Device Hrs		# Fail	Fail Rate in FITs (60% UCL)	
		55°C	70°C		55°C	70°C
1.8E + 5 2.8E + 5	0.3 LT 0.3 HVLT * VAF	1.0E + 6 4.1E + 7	6.6E + 5 2.7E + 7			
		Total 0.3 eV Failures =		0	0	0
1.8E + 5 2.8E + 5	0.5 LT 0.5 HVLT	3.2E + 6 5.0E + 6	1.6E + 6 2.5E + 6			
		Total 0.5 eV Failures =		0	111	227
1.8E + 5 2.8E + 5	0.6 LT 0.6 HVLT	5.7E + 6 8.9E + 6	2.4E + 6 3.8E + 6			
		Total 0.6 eV Failures =		0	0	0
1.8E + 5 2.8E + 5	1.0 LT 1.0 HVLT	5.8E + 7 9.0E + 7	1.4E + 7 2.2E + 7			
		Total 1.0 eV Failures =		0	0	0
		Combined Failure Rate (FITs) =			111	227
			48 Hour BI Infant Mortality = 0/600 = 0.00%			

3

Actual Device Hrs	Ea (eV)	Equivalent Device Hrs		# Fail	Fail Rate in FITs (60% UCL)	
		55°C	70°C		55°C	70°C
5.0E + 5 7.1E + 5	0.3 LT 0.3 HVLT * VAF	2.8E + 6 1.0E + 8	1.8E + 6 6.8E + 7			
	Total 0.3 eV Failures =			0	19	29
5.0E + 5 7.1E + 5	0.5 LT 0.5 HVLT	9.0E + 6 1.3E + 7	4.4E + 6 6.2E + 6			
	Total 0.5 eV Failures =			1	93	190
5.0E + 5 7.1E + 5	0.6 LT 0.6 HVLT	1.6E + 7 2.3E + 7	6.8E + 6 9.6E + 6			
	Total 0.6 eV Failures =			0	0	0
5.0E + 5 7.1E + 5	1.0 LT 1.0 HVLT	1.6E + 8 2.3E + 8	3.9E + 7 5.5E + 7			
	Total 1.0 eV Failures =			0	0	0
	Combined Failure Rate (FITs) =				112	219
48 Hour BI Infant Mortality = 0/2225 = 0.00% = 412 DPM @ 60% Confidence						

Other Data (CERDIP)

		Temp with Theta Ja Degree Kelvin	
Theta Ja =	55°C/W		
Theta Jc =	20°C/W		
V_{CC} =	5.25V	T(55°C) =	338.1 K
I_{CC} @ 55°C =	35 mA	T(70°C) =	353.1 K
I_{CC} @ 70°C =	35 mA	T(125°C) =	408.1 K
I_{CC} @ 125°C =	35 mA	T(250°C) =	533.1 K

Boltzman's Constant = K = 8.62×10^{-5} eV/K

Thermal Acceleration Factors—

Lifetest (LT) and High Voltage Lifetest (HVLT) Activation Energy	55°C	70°C	Bake Activation Energy	55°C	70°C
0.3	5.84	3.77	0.3	n/a	n/a
0.5	19.0	9.15	0.5	730	337
0.6	34.2	14.2	0.6	2730	1080
1.0	360	83.7	1.0	n/a	n/a

Other Data (PDIP)

Theta Ja =	75°C/W	**Temp with Theta Ja Degree Kelvin**	
Theta Jc =	22°C/W		
V_{CC} =	5.25V	T(55°C) =	341.8 K
I_{CC} @ 55°C =	35 mA	T(70°C) =	356.8 K
I_{CC} @ 70°C =	35 mA	T(125°C) =	411.8 K
I_{CC} @ 125°C =	35 mA	T(250°C) =	536.8 K

Boltzman's Constant = K = 8.62×10^{-5} eV/K

Thermal Acceleration Factors—

Lifetest (LT) and High Voltage Lifetest (HVLT)			Bake		
Activation Energy	55°C	70°C	Activation Energy	55°C	70°C
0.3	5.65	3.68	0.3	n/a	n/a
0.5	17.9	8.77	0.5	730	337
0.6	31.9	13.5	0.6	2730	1080
1.0	321	76.9	1.0	n/a	n/a

Other Data (PLCC)

Theta Ja =	75°C/W	**Temp with Theta Ja Degree Kelvin**	
Theta Jc =	22°C/W		
V_{CC} =	5.25V	T(55°C) =	341.8 K
I_{CC} @ 55°C =	35 mA	T(70°C) =	356.8 K
I_{CC} @ 70°C =	35 mA	T(125°C) =	411.8 K
I_{CC} @ 125°C =	35 mA	T(250°C) =	536.8 K

Boltzman's Constant = K = 8.62×10^{-5} eV/K

Thermal Acceleration Factors—

Lifetest (LT) and High Voltage Lifetest (HVLT)			Bake		
Activation Energy	55°C	70°C	Activation Energy	55°C	70°C
0.3	5.65	3.68	0.3	n/a	n/a
0.5	17.9	8.77	0.5	730	337
0.6	31.9	13.5	0.6	2730	1080
1.0	321	76.9	1.0	n/a	n/a

Failure Analysis

A. Leakage failure, 0.5 eV

3

85C060

Device:	85C060
Organization:	16 B Macrocells
Pinout:	24 Lead, 300 mil CERDIP and PDIP; 28 Lead PLCC
Die Size:	112 x 136 mils
Transistor Count:	~ 14K
Process:	CHMOS IIIE, P629.5
Programming Voltage:	12.5V
Technology:	CMOS

Table 1. Reliability Data

Package	Burn-In 48 Hours	125°C Dynamic Lifetest		
		168 Hours	500 Hours	1K Hours
CERDIP	1/900	0/899	0/270	0/270
PDIP	0/600	0/600	0/180	0/180
TOTALS	1/1500 A	0/1499	0/450	0/450

Package	125°C High Voltage Dynamic Lifetest (6.5V)		
	48 Hours	168 Hours	500 Hours
CERDIP	0/450	0/450	0/450
PDIP	0/300	0/300	0/300
TOTALS	0/750	0/750	0/750
Additional Readouts:			
CERDIP	0/450 @ 1K Hours HVLT		
PDIP	0/450 @ 1K Hours HVLT; 0/450 @ 2K Hours HVLT		

Package	Data Retention Bake (CERDIP @ 250°C, PDIP @ 140°C)		
	168 Hours	500 Hours	1K Hours
CERDIP	0/300	0/300	
PDIP	0/200	0/200	
TOTALS	0/500	0/500	

Table 2. Additional Qualification Stress Information

Package	Temperature Cycling (Condition "C"—150°C to −65°C)		
	500 Cycles	1K Cycles	2K Cycles
CERDIP	0/90	0/90	
PDIP	0/60	0/60	
PLCC	0/110	0/110	
TOTALS	0/260	0/260	

Package	Steam (121°C, 2 ATM)	
	96 Hours	168 Hours
PDIP	0/200	0/200
PLCC	0/100	1/100
TOTALS	0/300	1/300

Table 3. Failure Rate Predictions (CERDIP 85C060)

Actual Device Hrs	Ea (eV)	Equivalent Device Hrs		# Fail	Fail Rate in FITs (60% UCL)	
		55°C	70°C		55°C	70°C
3.3E + 5 4.3E + 5	0.3 LT 0.3 HVLT * VAF	1.8E + 6 6.0E + 7	1.2E + 6 4.0E + 7			
		Total 0.3 eV Failures =		0	0	0
3.3E + 5 4.3E + 5	0.5 LT 0.5 HVLT	5.5E + 6 7.1E + 6	2.8E + 6 3.6E + 6			
		Total 0.5 eV Failures =		0	72	145
3.3E + 5 4.3E + 5	0.6 LT 0.6 HVLT	9.7E + 6 1.3E + 7	4.2E + 6 5.4E + 6			
		Total 0.6 eV Failures =		0	0	0
3.3E + 5 4.3E + 5	1.0 LT 1.0 HVLT	9.2E + 7 1.2E + 8	2.3E + 7 3.0E + 7			
		Total 1.0 eV Failures =		0	0	0
		Combined Failure Rate (FITs) =			72	145
		48 Hour BI Infant Mortality = 1/2250 = 0.044%				

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Table 4. Failure Rate Predictions (PDIP 85C060)

Actual Device Hrs	Ea (eV)	Equivalent Device Hrs 55°C	Equivalent Device Hrs 70°C	# Fail	Fail Rate in FITs (60% UCL) 55°C	Fail Rate in FITs (60% UCL) 70°C
2.2E + 5 2.9E + 5	0.3 LT 0.3 HVLT * VAF	1.2E + 6 3.9E + 7	7.8E + 5 2.6E + 7			
		Total 0.3 eV Failures =		0	0	0
2.2E + 5 2.9E + 5	0.5 LT 0.5 HVLT	3.6E + 6 4.6E + 6	1.8E + 6 2.3E + 6			
		Total 0.5 eV Failures =		0	112	223
2.2E + 5 2.9E + 5	0.6 LT 0.6 HVLT	6.2E + 6 8.0E + 6	2.7E + 6 3.5E + 6			
		Total 0.6 eV Failures =		0	0	0
2.2E + 5 2.9E + 5	1.0 LT 1.0 HVLT	5.7E + 7 7.4E + 7	1.5E + 7 1.9E + 7			
		Total 1.0 eV Failures =		0	0	0
		Combined Failure Rate (FITs) =			112	223
		48 Hour BI Infant Mortality = 0/900 = 0.00%				

Table 5. Failure Rate Predictions (CERDIP and PDIP Combined Data 85C060)

Actual Device Hrs	Ea (eV)	Equivalent Device Hrs 55°C	Equivalent Device Hrs 70°C	# Fail	Fail Rate in FITs (60% UCL) 55°C	Fail Rate in FITs (60% UCL) 70°C
5.6E + 5 7.1E + 5	0.3 LT 0.3 HVLT * VAF	2.9E + 6 9.8E + 7	2.0E + 6 6.5E + 7			
		Total 0.3 eV Failures =		0	0	0
5.6E + 5 7.1E + 5	0.5 LT 0.5 HVLT	8.9E + 6 1.2E + 7	4.5E + 6 5.8E + 6			
		Total 0.5 eV Failures =		0	45	89
5.6E + 5 7.1E + 5	0.6 LT 0.6 HVLT	1.6E + 7 2.0E + 7	6.8E + 6 8.8E + 6			
		Total 0.6 eV Failures =		0	0	0
5.6E + 5 7.1E + 5	1.0 LT 1.0 HVLT	1.4E + 8 1.8E + 8	3.6E + 7 4.7E + 7			
		Total 1.0 eV Failures =		0	0	0
		Combined Failure Rate (FITs) =			45	89
		48 Hour BI Infant Mortality = 1/2250 = 0.04% = 899 DPM @ 60% Confidence				

Other Data (CERDIP)

Theta Ja =	59°C/W	**Temp with Theta Ja**	
Theta Jc =	18°C/W	**Degree Kelvin**	
V_{CC} =	5.25V	T(55°C) =	346.6 K
I_{CC} @ 55°C =	60 mA	T(70°C) =	361.6 K
I_{CC} @ 70°C =	60 mA	T(125°C) =	416.6 K
I_{CC} @ 125°C =	60 mA	T(250°C) =	541.6 K

Boltzman's Constant = K = 8.62×10^{-5} eV/K

Thermal Acceleration Factors—

Lifetest (LT) and High Voltage Lifetest (HVLT)			Bake		
Activation Energy	**55°C**	**70°C**	**Activation Energy**	**55°C**	**70°C**
0.3	5.41	3.56	0.3	n/a	n/a
0.5	16.6	8.31	0.5	730	337
0.6	29.2	12.7	0.6	2730	1080
1.0	277	69.1	1.0	n/a	n/a

Other Data (PDIP)

Theta Ja =	67°C/W	**Temp with Theta Ja**	
Theta Jc =	45°C/W	**Degree Kelvin**	
V_{CC} =	5.25V	T(55°C) =	349.1 K
I_{CC} @ 55°C =	60 mA	T(70°C) =	364.1 K
I_{CC} @ 70°C =	60 mA	T(125°C) =	419.1 K
I_{CC} @ 125°C =	60 mA	T(250°C) =	544.1 K

Boltzman's Constant = K = 8.62×10^{-5} eV/K

Thermal Acceleration Factors—

Lifetest (LT) and High Voltage Lifetest (HVLT)			Bake		
Activation Energy	**55°C**	**70°C**	**Activation Energy**	**55°C**	**70°C**
0.3	5.29	3.51	0.3	n/a	n/a
0.5	16.0	8.09	0.5	730	337
0.6	27.9	12.3	0.6	2730	1080
1.0	257	65.4	1.0	n/a	n/a

Other Data (PLCC)

Theta Ja =	65°C/W	**Temp with Theta Ja**	
Theta Jc =	16°C/W	**Degree Kelvin**	
V_{CC} =	5.25V	T(55°C) =	349.1 K
I_{CC} @ 55°C =	60 mA	T(70°C) =	364.1 K
I_{CC} @ 70°C =	60 mA	T(125°C) =	419.1 K
I_{CC} @ 125°C =	60 mA	T(250°C) =	544.1 K

Boltzman's Constant = K = 8.62×10^{-5} eV/K

Thermal Acceleration Factors—

Lifetest (LT) and High Voltage Lifetest (HVLT)			Bake		
Activation Energy	**55°C**	**70°C**	**Activation Energy**	**55°C**	**70°C**
0.3	5.29	3.51	0.3	n/a	n/a
0.5	16.0	8.09	0.5	730	337
0.6	27.9	12.3	0.6	2730	1080
1.0	257	65.4	1.0	n/a	n/a

Failure Analysis

A. Charge Loss due to Passivation Damage.

85C090

Device:	85C090
Organization:	24 Macrocells
Pinout:	40 Lead, 600 mil CERDIP and PDIP; 44 Lead PLCC
Die Size:	136 x 152 mils
Transistor Count:	~30K
Process:	CHMOS IIIE, P629.5
Programming Voltage:	12.5V
Technology:	CMOS

Table 1. Reliability Data

Package	Burn-In 48 Hours	125°C Dynamic Lifetest		
		168 Hours	500 Hours	1K Hours
CERDIP	0/900	0/900	0/90	0/90
PDIP	0/600	0/600		
TOTALS	0/1500	0/1500	0/90	0/90

Package	125°C High Voltage Dynamic Lifetest (6.5V)		
	48 Hours	168 Hours	500 Hours
CERDIP	0/450	0/450	0/270
PDIP	0/300	0/300	0/240
TOTALS	0/750	0/750	0/510

Additional Readouts:
- CERDIP 0/270 @ 1K Hours HVLT
- PDIP 0/240 @ 1K Hours HVLT

Package	Data Retention Bake (CERDIP @ 250°C, PDIP @ 140°C)		
	168 Hours	500 Hours	1K Hours
CERDIP	0/300	0/300	
PDIP	0/200	0/200	
TOTALS	0/500	0/500	

Table 2. Additional Qualification Stress Information

Package	Temperature Cycling (Condition "C"—150°C to −65°C)		
	500 Cycles	1K Cycles	2K Cycles
CERDIP	0/90	0/90	
PDIP	0/60	0/60	
PLCC	0/149	0/149	
TOTALS	0/299	0/299	

Package	Steam (121°C, 2 ATM)	
	96 Hours	168 Hours
PDIP	0/200	0/200
PLCC	0/100	0/100
TOTALS	0/300	0/300

Table 3. Failure Rate Predictions (CERDIP 85C090)

Actual Device Hrs	Ea (eV)	Equivalent Device Hrs		# Fail	Fail Rate in FITs (60% UCL)	
		55°C	70°C		55°C	70°C
9.0E + 4 2.7E + 5	0.3 LT 0.3 HVLT * VAF	4.6E + 5 3.6E + 7	3.1E + 5 2.4E + 7			
		Total 0.3 eV Failures =		0	0	0
9.0E + 4 2.7E + 5	0.5 LT 0.5 HVLT	1.4E + 6 4.1E + 6	7.0E + 5 2.1E + 6			
		Total 0.5 eV Failures =		0	166	326
9.0E + 4 2.7E + 5	0.6 LT 0.6 HVLT	2.4E + 6 7.1E + 6	1.1E + 6 3.2E + 6			
		Total 0.6 eV Failures =		0	0	0
9.0E + 4 2.7E + 5	1.0 LT 1.0 HVLT	2.1E + 7 6.3E + 7	5.5E + 6 1.6E + 7			
		Total 1.0 eV Failures =		0	0	0
		Combined Failure Rate (FITs) =			166	326
		48 Hour BI Infant Mortality = 0/1350 = 0.00%				

Table 4. Failure Rate Predictions (PDIP 85C090)

Actual Device Hrs	Ea (eV)	Equivalent Device Hrs 55°C	Equivalent Device Hrs 70°C	# Fail	Fail Rate in FITs (60% UCL) 55°C	Fail Rate in FITs (60% UCL) 70°C
7.2E + 4 2.4E + 5	0.3 LT 0.3 HVLT * VAF	3.6E + 5 3.1E + 7	2.4E + 5 2.1E + 7			
		Total 0.3 eV Failures =		0	0	0
7.2E + 4 2.4E + 5	0.5 LT 0.5 HVLT	1.1E + 6 3.5E + 6	5.4E + 5 1.8E + 6			
		Total 0.5 eV Failures =		0	202	390
7.2E + 4 2.4E + 5	0.6 LT 0.6 HVLT	1.8E + 6 6.0E + 6	8.1E + 5 2.7E + 6			
		Total 0.6 eV Failures =		0	0	0
7.2E + 4 2.4E + 5	1.0 LT 1.0 HVLT	1.5E + 7 5.1E + 7	4.1E + 6 1.4E + 7			
		Total 1.0 eV Failures =		0	0	0
		Combined Failure Rate (FITs) =			202	390
		48 Hour BI Infant Mortality = 0/900 = 0.00%				

Table 5. Failure Rate Predictions (CERDIP and PDIP Combined Data 85C090)

Actual Device Hrs	Ea (eV)	Equivalent Device Hrs 55°C	Equivalent Device Hrs 70°C	# Fail	Fail Rate in FITs (60% UCL) 55°C	Fail Rate in FITs (60% UCL) 70°C
1.6E + 5 5.1E + 5	0.3 LT 0.3 HVLT * VAF	8.0E + 5 6.6E + 7	5.4E + 5 4.5E + 7			
		Total 0.3 eV Failures =		0	0	0
1.6E + 5 5.1E + 5	0.5 LT 0.5 HVLT	2.3E + 6 7.4E + 6	1.2E + 6 3.8E + 6			
		Total 0.5 eV Failures =		0	94	182
1.6E + 5 5.1E + 5	0.6 LT 0.6 HVLT	4.0E + 6 1.3E + 7	1.8E + 6 5.7E + 6			
		Total 0.6 eV Failures =		0	0	0
1.6E + 5 5.1E + 5	1.0 LT 1.0 HVLT	3.4E + 7 1.1E + 8	9.1E + 6 2.9E + 7			
		Total 1.0 eV Failures =		0	0	0
		Combined Failure Rate (FITs) =			94	182
		48 Hour BI Infant Mortality = 0/2250 = 0.00% = 408 DPM @ 60% Confidence				

Other Data (CERDIP)

Theta Ja =	44.5°C/W	**Temp with Theta Ja**	
Theta Jc =	17°C/W	**Degree Kelvin**	
V_{CC} =	5.25V	T(55°C) =	353.5 K
I_{CC} @ 55°C =	105 mA	T(70°C) =	368.5 K
I_{CC} @ 70°C =	105 mA	T(125°C) =	423.5 K
I_{CC} @ 125°C =	105 mA	T(250°C) =	548.5 K

Boltzman's Constant = K = 8.62×10^{-5} eV/K

Thermal Acceleration Factors—

Lifetest (LT) and High Voltage Lifetest (HVLT)			Bake (250°C)		
Activation Energy	**55°C**	**70°C**	**Activation Energy**	**55°C**	**70°C**
0.3	5.13	3.43	0.3	n/a	n/a
0.5	15.3	7.8	0.5	730	337
0.6	26.3	11.8	0.6	2730	1080
1.0	233	60.9	1.0	n/a	n/a

Other Data (PDIP)

Theta Ja =	51°C/W	**Temp with Theta Ja**	
Theta Jc =	29°C/W	**Degree Kelvin**	
V_{CC} =	5.25V	T(55°C) =	356.1 K
I_{CC} @ 55°C =	105 mA	T(70°C) =	371.1 K
I_{CC} @ 70°C =	105 mA	T(125°C) =	426.1 K
I_{CC} @ 125°C =	105 mA	T(250°C) =	551.1 K

Boltzman's Constant = K = 8.62×10^{-5} eV/K

Thermal Acceleration Factors—

Lifetest (LT) and High Voltage Lifetest (HVLT)			Bake (140°C)		
Activation Energy	**55°C**	**70°C**	**Activation Energy**	**55°C**	**70°C**
0.3	4.98	3.35	0.3	n/a	n/a
0.5	14.5	7.52	0.5	730	337
0.6	24.8	11.3	0.6	2730	1080
1.0	211	56.5	1.0	n/a	n/a

Other Data (PLCC)

Theta Ja =	55°C/W	**Temp with Theta Ja**	
Theta Jc =	16°C/W	**Degree Kelvin**	
V_{CC} =	5.25V	T(55°C) =	356.1 K
I_{CC} @ 55°C =	105 mA	T(70°C) =	371.1 K
I_{CC} @ 70°C =	105 mA	T(125°C) =	426.1 K
I_{CC} @ 125°C =	105 mA	T(250°C) =	551.1 K

Boltzman's Constant = K = 8.62×10^{-5} eV/K

Thermal Acceleration Factors—

Lifetest (LT) and High Voltage Lifetest (HVLT)			**Bake (140°C)**		
Activation Energy	**55°C**	**70°C**	**Activation Energy**	**55°C**	**70°C**
0.3	4.98	3.35	0.3	n/a	n/a
0.5	14.5	7.52	0.5	730	337
0.6	24.8	11.3	0.6	2730	1080
1.0	211	56.5	1.0	n/a	n/a

Failure Analysis

N/A

85C508

Device:	85C508
Organization:	Decoder/Latch PLD
Pinout:	28 Lead, 300 mil CERDIP and PDIP; 28 Lead PLCC
Die Size:	65 x 98 mils
Transistor Count:	~10K
Process:	CHMOS IIIE, P629.5
Programming Voltage:	12.5V
Technology:	CMOS

Table 1. Reliability Data

Package	Burn-In 48 Hours	125°C Dynamic Lifetest		
		168 Hours	1K Hours	2K Hours
CERDIP PDIP	0/1200 1/800	0/1195 0/799	0/270 0/180	
TOTALS	1/2000 A	0/1994	0/450	

Package	125°C High Voltage Dynamic Lifetest (6.5V)		
	48 Hours	168 Hours	1K Hours
CERDIP PDIP	1/599 0/399	0/599 0/399	0/270 0/180
TOTALS	1/998	0/998	0/450

Package	Data Retention Bake (CERDIP @ 250°C, PDIP @ 140°C)		
	168 Hours	500 Hours	1K Hours
CERDIP PDIP	0/300 0/200	0/300 0/200	
TOTALS	0/500	0/500	

Table 2. Additional Qualification Stress Information

Package	Temperature Cycling (Condition "C"—150°C to −65°C)		
	500 Cycles	1K Cycles	2K Cycles
CERDIP	0/150	0/150	
PDIP	0/100	0/100	
PLCC	0/60	0/60	
TOTALS	0/310	0/310	

Package	Steam (121°C, 2 ATM)		
	168 Hours	336 Hours	500 Hours
PDIP	0/200	0/200	0/200
PLCC	1/600	0/60	
TOTALS	0/260	0/260	0/200

Table 3. Failure Rate Predictions (CERDIP 85C508)

Actual Device Hrs	Ea (eV)	Equivalent Device Hrs		# Fail	Fail Rate in FITs (60% UCL)	
		55°C	70°C		55°C	70°C
3.7E + 5 3.0E + 5	0.3 LT 0.3 HVLT * VAF	2.2E + 6 4.5E + 7	1.4E + 6 2.9E + 7			
		Total 0.3 eV Failures =		0	0	0
3.7E + 5 3.0E + 5	0.5 LT 0.5 HVLT	7.1E + 6 5.7E + 6	3.4E + 6 2.7E + 6			
		Total 0.5 eV Failures =		0	71	151
3.7E + 5 3.0E + 5	0.6 LT 0.6 HVLT	1.3E + 7 1.0E + 7	5.2E + 6 4.2E + 6			
		Total 0.6 eV Failures =		0	0	0
3.7E + 5 3.0E + 5	1.0 LT 1.0 HVLT	1.4E + 8 1.1E + 8	3.1E + 7 2.5E + 7			
		Total 1.0 eV Failures =		0	0	0
		Combined Failure Rate (FITs) =			71	151
		48 Hour BI Infant Mortality = 0/1799 = 0.00%				

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Table 4. Failure Rate Predictions (PDIP 85C508)

Actual Device Hrs	Ea (eV)	Equivalent Device Hrs		# Fail	Fail Rate in FITs (60% UCL)	
		55°C	70°C		55°C	70°C
2.5E + 5 2.0E + 5	0.3 LT 0.3 HVLT * VAF	1.4E + 6 3.0E + 7	9.1E + 5 1.9E + 7			
		Total 0.3 eV Failures =		0	0	0
2.5E + 5 2.0E + 5	0.5 LT 0.5 HVLT	4.6E + 6 3.7E + 6	2.2E + 6 1.8E + 6			
		Total 0.5 eV Failures =		0	111	232
2.5E + 5 2.0E + 5	0.6 LT 0.6 HVLT	8.2E + 6 6.6E + 6	3.4E + 6 2.7E + 6			
		Total 0.6 eV Failures =		0	0	0
2.5E + 5 2.0E + 5	1.0 LT 1.0 HVLT	8.5E + 7 6.8E + 7	1.9E + 7 1.6E + 6			
		Total 1.0 eV Failures =		0	0	0
		Combined Failure Rate (FITs) =			111	232
48 Hour BI Infant Mortality = 1/1199 = 0.08%						

Table 5. Failure Rate Predictions (CERDIP and PDIP Combined Data)

Actual Device Hrs	Ea (eV)	Equivalent Device Hrs		# Fail	Fail Rate in FITs (60% UCL)	
		55°C	70°C		55°C	70°C
6.1E + 5 5.0E + 5	0.3 LT 0.3 HVLT * VAF	3.6E + 6 7.4E + 7	2.3E + 6 4.8E + 7			
		Total 0.3 eV Failures =		0	0	0
6.1E + 5 5.0E + 5	0.5 LT 0.5 HVLT	1.1E + 7 9.2E + 6	5.5E + 6 4.4E + 6			
		Total 0.5 eV Failures =		0	44	92
6.1E + 5 5.0E + 5	0.6 LT 0.6 HVLT	2.1E + 7 1.7E + 7	8.5E + 6 6.8E + 6			
		Total 0.6 eV Failures =		0	0	0
6.1E + 5 5.0E + 5	1.0 LT 1.0 HVLT	2.1E + 8 1.7E + 8	4.9E + 7 3.9E + 7			
		Total 1.0 eV Failures =		0	0	0
		Combined Failure Rate (FITs) =			44	92
48 Hour BI Infant Mortality = 1/2998 = 0.03% = 675 DPM @ 60% Confidence						

Other Data (CERDIP)

Theta Ja =	83°C/W	**Temp with Theta Ja Degree Kelvin**	
Theta Jc =	18°C/W		
V_{CC} =	5.25V	T(55°C) =	335 K
I_{CC} @ 55°C =	15 mA	T(70°C) =	350 K
I_{CC} @ 70°C =	15 mA	T(125°C) =	403 K
I_{CC} @ 125°C =	12 mA	T(250°C) =	523 K

Boltzman's Constant = K = 8.62 × 10^{-5} eV/K

Thermal Acceleration Factors—

Lifetest (LT) and High Voltage Lifetest (HVLT)			**Bake (250°C)**		
Activation Energy	**55°C**	**70°C**	**Activation Energy**	**55°C**	**70°C**
0.3	5.88	3.76	0.3	n/a	n/a
0.5	19.2	9.10	0.5	727	336
0.6	34.6	14.2	0.6	2718	1075
1.0	367	82.8	1.0	n/a	n/a

Other Data (PLCC)

Theta Ja =	100°C/W	**Temp with Theta Ja Degree Kelvin**	
Theta Jc =	23°C/W		
V_{CC} =	5.25V	T(55°C) =	336 K
I_{CC} @ 55°C =	15 mA	T(70°C) =	350 K
I_{CC} @ 70°C =	15 mA	T(125°C) =	403 K
I_{CC} @ 125°C =	12 mA	T(250°C) =	413 K

Boltzman's Constant = K = 8.62 × 10^{-5} eV/K

Thermal Acceleration Factors—

Lifetest (LT) and High Voltage Lifetest (HVLT)			**Bake (140°C)**		
Activation Energy	**55°C**	**70°C**	**Activation Energy**	**55°C**	**70°C**
0.3	5.77	3.71	0.3	n/a	n/a
0.5	18.6	8.87	0.5	38.0	17.5
0.6	33.3	13.7	0.6	78.7	31.1
1.0	345	78.8	1.0	n/a	n/a

Failure Analysis

A. Isb Failure — 0.3 eV

5AC312

Device:	5AC312
Organization:	12 Macrocells
Pinout:	24 Lead, 300 mil CERDIP and PDIP (28 Lead PLCC)
Die Size:	130 x 189 mils
Transistor Count:	~17K
Process:	CHMOS IIIE, P429
Programming Voltage:	12.5V
Technology:	CMOS

Table 1. Reliability Data

Package	Burn-In 48 Hours	125°C Dynamic Lifetest		
		168 Hours	500 Hours	1K Hours
CERDIP	1/3960	0/2955	0/183	0/183
TOTALS	1/3960 A	0/2955	0/183	0/183
Additional Readouts: CERDIP	0/183 @ 2K Hours Lifetest			

Package	125°C High Voltage Dynamic Lifetest (7.0V)		
	48 Hours	168 Hours	500 Hours
CERDIP	0/97	0/93	0/92
TOTALS	0/97	0/93	0/92
Additional Readouts: CERDIP	0/80 @ 1K Hours High Voltage Lifetest		

Package	Data Retention Bake (CERDIP @ 250°C)		
	48 Hours	168 Hours	500 Hours
CERDIP	0/100	0/99	0/99
TOTALS	0/100	0/99	0/99
Additional Readouts: CERDIP	0/96 @ 1K Hours, 250°C Bake		

Table 2. Additional Qualification Stress Information

Package	Temperature Cycling (Condition "C"—150°C to −65°C)		
	200 Cycles	500 Cycles	1K Cycles
PDIP	0/234	0/234	0/234
TOTALS	0/234	0/234	0/234

Package	85°C/85% Relative Humidity		
	168 Hours	500 Hours	1K Hours
PDIP	0/219	0/219	0/219
TOTALS	0/219	0/219	0/219
Additional Readouts:			
PDIP	0/219 @ 2K Hours		

Package	Thermal Shock (Condition "C"—150°C to −65°C)		
	50 Cycles	200 Cycles	500 Cycles
PDIP	0/231	0/231	0/231
TOTALS	0/231	0/231	0/231

Package	Steam (121°C, 2 ATM)	
	96 Hours	168 Hours
PDIP	0/393	0/393
PLCC	0/304	0/304
TOTALS	0/697	0/697
Additional Readouts:		
PDIP	0/234 @ 336 Hours of Steam	

Table 3. Failure Rate Predictions (5AC312-CERDIP-Fab 1)

Actual Device Hrs	Ea (eV)	Equivalent Device Hrs 55°C	Equivalent Device Hrs 70°C	# Fail	Fail Rate in FITs (60% UCL) 55°C	Fail Rate in FITs (60% UCL) 70°C
6.90E + 05	0.3 LT	3.42E + 06	2.26E + 06	0		
8.64E + 04	0.3 HVLT * VAF	3.98E + 07	2.63E + 07	0		
		Total 0.3 eV Failures =		0	0.0	0.0
6.90E + 05	0.5 LT	9.96E + 06	5.00E + 06	0		
8.64E + 04	0.5 HVLT	1.25E + 06	6.26E + 05	0		
		Total 0.5 eV Failures =		0	81.7	162.7
6.90E + 05	0.6 LT	1.70E + 07	7.42E + 06	0		
8.64E + 04	0.6 HVLT	2.13E + 06	9.29E + 05	0		
		Total 0.6 eV Failures =		0	0.0	0.0
6.90E + 05	1.0 LT	1.44E + 08	3.62E + 07	0		
8.64E + 04	1.0 HVLT	1.80E + 07	4.53E + 06	0		
		Total 1.0 eV Failures =		0	0.0	0.0
		Combined Failure Rate (FITs) =			81.7	162.7
48 Hour BI Infant Mortality = 1/3960 = 0.0253% = 511 DPM @ 60% Confidence						

Other Data (CERDIP)

		Temp with Theta Ja Degree Kelvin	
Theta Ja =	47°C/W		
Theta Jc =	16°C/W		
V_{CC} =	5.25V	T(55°C) =	348 K
I_{CC} @ 55°C =	80 mA	T(70°C) =	363 K
I_{CC} @ 70°C =	80 mA	T(125°C) =	414 K
I_{CC} @ 125°C =	65 mA	T(250°C) =	523 K

Boltzman's Constant = K = 8.62×10^{-5} eV/K

Thermal Acceleration Factors—

Lifetest (LT) and High Voltage Lifetest (HVLT) Activation Energy	55°C	70°C	Bake (250°C) Activation Energy	55°C	70°C
0.3	4.96	3.28	0.3	n/a	n/a
0.5	14.43	7.24	0.5	727.61	335.91
0.6	24.61	10.76	0.6	2718.18	1075.15
1.0	208.28	52.47	1.0	n/a	n/a

Other Data (PDIP)

Theta Ja =	52°C/W	**Temp with Theta Ja Degree Kelvin**	
Theta Jc =	16°C/W		
V_{CC} =	5.25V	T(55°C) =	349.84 K
I_{CC} @ 55°C =	80 mA	T(70°C) =	364.84 K
I_{CC} @ 70°C =	80 mA	T(125°C) =	415.75 K
I_{CC} @ 125°C =	65 mA	T(140°C) =	413 K

Boltzman's Constant = K = 8.62×10^{-5} eV/K

Thermal Acceleration Factors—

Lifetest (LT) and High Voltage Lifetest (HVLT) Activation Energy	55°C	70°C	Bake (140°C) Activation Energy	55°C	70°C
0.3	4.84	3.21	0.3	n/a	n/a
0.5	13.83	7.00	0.5	38.00	17.54
0.6	23.39	10.33	0.6	78.65	31.11
1.0	191.27	48.96	1.0	n/a	n/a

Other Data (PLCC)

Theta Ja =	56°C/W	**Temp with Theta Ja Degree Kelvin**	
Theta Jc =	16°C/W		
V_{CC} =	5.25V	T(55°C) =	351.52 K
I_{CC} @ 55°C =	80 mA	T(70°C) =	366.52 K
I_{CC} @ 70°C =	80 mA	T(125°C) =	417.11 K
I_{CC} @ 125°C =	65 mA	T(140°C) =	413 K

Boltzman's Constant = K = 8.62×10^{-5} eV/K

Thermal Acceleration Factors—

Lifetest (LT) and High Voltage Lifetest (HVLT) Activation Energy	55°C	70°C	Bake (140°C) Activation Energy	55°C	70°C
0.3	4.74	3.16	0.3	n/a	n/a
0.5	13.37	6.81	0.5	38.00	17.54
0.6	22.46	9.99	0.6	78.65	31.11
1.0	178.85	46.37	1.0	n/a	n/a

Voltage Acceleration Factor (VAF) for HVLT on this process is 26 (6.5V) and 93 (7.0V).

NOTE:
FIT = Failure in Time. 1 FIT = 1 failure per 1×10^9 device hours.

Failure Analysis

A. 1 oxide failure − 0.3 eV

Device:	5AC324
Organization:	24 Macrocells
Pinout:	40 Lead, 600 mil CERDIP and PDIP (44 Lead PLCC)
Die Size:	241 x 187 mils
Transistor Count:	~68K
Process:	CHMOS IIIE, P429
Programming Voltage:	12.5V
Technology:	CMOS

Table 1. Reliability Data

Package	Burn-In 48 Hours	125°C Dynamic Lifetest		
		168 Hours	500 Hours	1K Hours
CERDIP	4/5721	0/2972	0/401	0/401
TOTALS	4/5721 A	0/2972	0/401	0/401
Additional Readouts: CERDIP	0/103 @ 2K Hours Lifetest			

Package	125°C High Voltage Dynamic Lifetest (7.0V)		
	48 Hours	168 Hours	500 Hours
CERDIP	0/113	0/113	0/113
TOTALS	0/113	0/113	0/113
Additional Readouts: CERDIP	0/113 @ 1K Hours High Voltage Lifetest		

Package	Data Retention Bake (CERDIP @ 250°C)		
	48 Hours	168 Hours	500 Hours
CERDIP	0/99	0/99	0/99
TOTALS	0/99	0/99	0/99
Additional Readouts: CERDIP	0/99 @ 1K Hours, 250°C Bake		

Table 2. Additional Qualification Stress Information

Package	Temperature Cycling (Condition "C"—150°C to −65°C)		
	200 Cycles	500 Cycles	1000 Cycles
CERDIP	0/176	0/176	0/176
PDIP	0/48	0/48	0/48
Additional Readouts:			
CERDIP	0/176 @ 1700 Cycles		
PDIP	0/48 @ 1700 Cycles		

Package	85°C/85% Relative Humidity		
	168 Hours	500 Hours	1K Hours
PDIP	0/291	0/291	0/291
TOTALS	0/291	0/291	0/291

Package	Steam (121°C, 2 ATM)	
	96 Hours	168 Hours
PDIP	0/104	0/104
PLCC	0/481	0/481
TOTALS	0/585	0/585
Additional Readouts:		
PDIP	0/104 @ 500 Hours of Steam	
PLCC	0/333 @ 500 Hours of Steam	

Table 3. Failure Rate Predictions (5AC324-CERDIP-Fab 1)

Actual Device Hrs	Ea (eV)	Equivalent Device Hrs		# Fail	Fail Rate in FITs (60% UCL)	
		55°C	70°C		55°C	70°C
7.93E + 05	0.3 LT	3.66E + 06	2.46E + 06	0		
1.13E + 05	0.3 HVLT * VAF	4.85E + 07	3.26E + 07	0		
		Total 0.3 eV Failures =		0	0.0	0.0
7.93E + 05	0.5 LT	1.01E + 07	5.22E + 06	0		
1.13E + 05	0.5 HVLT	1.44E + 06	7.44E + 05	0		
		Total 0.5 eV Failures =		0	79.0	153.3
7.93E + 05	0.6 LT	1.69E + 07	7.62E + 06	0		
1.13E + 05	0.6 HVLT	2.40E + 06	1.09E + 06	0		
		Total 0.6 eV Failures =		0	0.0	0.0
7.93E + 05	1.0 LT	1.30E + 08	3.44E + 07	0		
1.13E + 05	1.0 HVLT	1.85E + 07	4.90E + 06	0		
		Total 1.0 eV Failures =		0	0.0	0.0
		Combined Failure Rate (FITs) =			79.0	153.3
48 Hour BI Infant Mortality = 4/5721 = 0.0699% = 916 DPM @ 60% Confidence						

3

Other Data (CERDIP)

Theta Ja =	34°C/W	**Temp with Theta Ja**	
Theta Jc =	13°C/W	**Degree Kelvin**	
V_{CC} =	5.25V	T(55°C) =	355 K
I_{CC} @ 55°C =	150 mA	T(70°C) =	370 K
I_{CC} @ 70°C =	150 mA	T(125°C) =	420 K
I_{CC} @ 125°C =	125 mA	T(250°C) =	523 K

Boltzman's Constant = K = 8.62×10^{-5} eV/K

Thermal Acceleration Factors—

Lifetest (LT) and High Voltage Lifetest (HVLT) Activation Energy	55°C	70°C	Bake (250°C) Activation Energy	55°C	70°C
0.3	4.61	3.10	0.3	n/a	n/a
0.5	12.78	6.59	0.5	727.61	335.91
0.6	21.27	9.60	0.6	2718.18	1075.15
1.0	163.32	43.38	1.0	n/a	n/a

Other Data (PDIP and PLCC)

Theta Ja =	43°C/W	**Temp with Theta Ja**	
Theta Jc =	15°C/W	**Degree Kelvin**	
V_{CC} =	5.25V	T(55°C) =	361.86 K
I_{CC} @ 55°C =	150 mA	T(70°C) =	376.86 K
I_{CC} @ 70°C =	150 mA	T(125°C) =	426.22 K
I_{CC} @ 125°C =	125 mA	T(140°C) =	413 K

Boltzman's Constant = K = 8.62×10^{-5} eV/K

Thermal Acceleration Factors—

Lifetest (LT) and High Voltage Lifetest (HVLT) Activation Energy	55°C	70°C	Bake (140°C) Activation Energy	55°C	70°C
0.3	4.27	2.91	0.3	n/a	n/a
0.5	11.23	5.94	0.5	38.00	17.54
0.6	18.22	8.48	0.6	78.65	31.11
1.0	126.20	35.25	1.0	n/a	n/a

Voltage Acceleration Factor (VAF) for HVLT on this process is 26 (6.5V) and 93 (7.0V).

NOTE:
FIT = Failure in Time. 1 FIT = 1 failure per 1×10^9 device hours.

Failure Analysis

A. 2 passivation crack — 0.5 eV
1 metal stringer — 0.5 eV
1 oxide defect — 0.3 eV

Device:	5C032
Organization:	8 Macrocells
Pinout:	20 Lead, 300 mil CERDIP and PDIP
Die Size:	86 x 93 mils
Transistor Count:	~ 7K
Process:	CHMOS IIE, P424
Programming Voltage:	12.5V
Technology:	CMOS

Table 1. Reliability Data

Package	Burn-In 48 Hours	125°C Dynamic Lifetest		
		168 Hours	500 Hours	1K Hours
CERDIP PDIP	0/2956 1/2661	0/2956 0/2660	0/299 0/149	2/283 0/146
TOTALS	1/5617 A	0/5616	0/448	2/429 B
Additional Readouts: CERDIP 0/281 @ 2K Hours Lifetest				

Package	125°C High Voltage Dynamic Lifetest (6.5V)		
	48 Hours	168 Hours	500 Hours
CERDIP PDIP	0/200 0/150	0/200 1/150	0/179 0/149
TOTALS	0/350	1/350 C	0/328
Additional Readouts: CERDIP 0/129 @ 1K Hours High Voltage Lifetest PDIP 0/146 @ 1K Hours High Voltage Lifetest			

Package	Data Retention Bake (CERDIP @ 250°C, PDIP @ 140°C)		
	48 Hours	168 Hours	500 Hours
CERDIP PDIP	2/277 0/300	0/146 0/298	0/146 0/298
TOTALS	2/577 D	0/444	0/444
Additional Readouts: PDIP 0/298 @ 1K Hours, 140°C Bake			

Package	Temperature Cycling (Condition "C"—150°C to −65°C)		
	200 Cycles	500 Cycles	1K Cycles
CERDIP	0/232	0/75	0/75
PDIP	0/150	0/149	0/149
TOTALS	0/382	0/224	0/224

Package	Thermal Shock (Condition "C"—150°C to −65°C)		
	50 Cycles	200 Cycles	500 Cycles
PDIP	0/150	0/150	0/150
TOTALS	0/150	0/150	0/150

Package	85°C/85% Relative Humidity		
	168 Hours	500 Hours	1K Hours
PDIP	0/263	0/263	1/263
TOTALS	0/263	0/263	1/263 E

Package	Steam (121°C, 2 ATM)	
	96 Hours	168 Hours
PDIP	0/262	0/262

Additional Readouts:
PDIP 0/262 @ 500 Hours of Steam

Table 3. Failure Rate Predictions (CERDIP)

Actual Device Hrs	Ea (eV)	Equivalent Device Hrs 55°C	Equivalent Device Hrs 70°C	# Fail	Fail Rate in FITs (60% UCL) 55°C	Fail Rate in FITs (60% UCL) 70°C
8.76E + 05 1.58E + 05	0.3 LT 0.3 HVLT * VAF	4.76E + 06 4.70E + 07	3.10E + 06 3.06E + 07	0 0		
		Total 0.3 eV Failures =		0	0.0	0.0
8.76E + 05 1.58E + 05	0.5 LT 0.5 HVLT	1.47E + 07 2.64E + 06	7.18E + 06 1.29E + 06	0 0		
		Total 0.5 eV Failures =		0	52.8	108.0
8.76E + 05 1.58E + 05	0.6 LT 0.6 HVLT	2.58E + 07 4.64E + 06	1.09E + 07 1.97E + 06	0 0		
		Total 0.6 eV Failures =		0	0.0	0.0
8.76E + 05 1.58E + 05	1.0 LT 1.0 HVLT	2.46E + 08 4.43E + 07	5.88E + 07 1.06E + 07	2 0		
		Total 1.0 eV Failures =		2	10.7	44.7
		Combined Failure Rate (FITs) =			63.5	152.8
48 Hour BI Infant Mortality = 0/2956 = 0.0000% = 310 DPM @ 60% Confidence						

Other Data (CERDIP)

		Temp with Theta Ja Degree Kelvin	
Theta Ja =	83°C/W		
Theta Jc =	20°C/W		
V_{CC} =	5.25V	T(55°C) =	341.07 K
I_{CC} @ 55°C =	30 mA	T(70°C) =	356.07 K
I_{CC} @ 70°C =	30 mA	T(125°C) =	408.89 K
I_{CC} @ 125°C =	25 mA	T(250°C) =	523 K

Boltzman's Constant = K = 8.62×10^{-5} eV/K

Thermal Acceleration Factors—

Lifetest (LT) and High Voltage Lifetest (HVLT) Activation Energy	55°C	70°C	Bake (250°C) Activation Energy	55°C	70°C
0.3	5.43	3.53	0.3	n/a	n/a
0.5	16.76	8.19	0.5	727.61	335.91
0.6	29.46	12.48	0.6	2718.18	1075.15
1.0	280.99	67.11	1.0	n/a	n/a

Table 4. Failure Rate Predictions (PDIP)

Actual Device Hrs	Ea (eV)	Equivalent Device Hrs 55°C	Equivalent Device Hrs 70°C	# Fail	Fail Rate in FITs (60% UCL) 55°C	Fail Rate in FITs (60% UCL) 70°C
4.42E + 05 1.48E + 05	0.3 LT 0.3 HVLT * VAF	2.28E + 06 4.19E + 07	1.50E + 06 2.75E + 07	0 0		
		Total 0.3 eV Failures =		0	20.7	31.5
4.42E + 05 1.48E + 05	0.5 LT 0.5 HVLT	6.81E + 06 2.28E + 06	3.38E + 06 1.13E + 06	0 1		
		Total 0.5 eV Failures =		1	222.5	447.7
4.42E + 05 1.48E + 05	0.6 LT 0.6 HVLT	1.18E + 07 3.93E + 06	5.08E + 06 1.70E + 06	0 0		
		Total 0.6 eV Failures =		0	0.0	0.0
4.42E + 05 1.48E + 05	1.0 LT 1.0 HVLT	1.05E + 08 3.51E + 07	2.59E + 07 8.65E + 06	0 0		
		Total 1.0 eV Failures =		0	0.0	0.0
		Combined Failure Rate (FITs) =			243.2	479.3
48 Hour BI Infant Mortality = 1/2661 = 0.0376% = 760 DPM @ 60% Confidence						

Other Data (PDIP)

Theta Ja =	109°C/W	**Temp with Theta Ja**	
Theta Jc =	20°C/W	**Degree Kelvin**	
V_{CC} =	5.25V	T(55°C) =	345.17 K
I_{CC} @ 55°C =	30 mA	T(70°C) =	360.17 K
I_{CC} @ 70°C =	30 mA	T(125°C) =	412.31 K
I_{CC} @ 125°C =	25 mA	T(140°C) =	413 K

Boltzman's Constant = K = 8.62×10^{-5} eV/K

Thermal Acceleration Factors—

Lifetest (LT) and High Voltage Lifetest (HVLT) Activation Energy	55°C	70°C	Bake (140°C) Activation Energy	55°C	70°C
0.3	5.16	3.39	0.3	n/a	n/a
0.5	15.41	7.66	0.5	38.00	17.54
0.6	26.62	11.50	0.6	78.65	31.11
1.0	237.39	58.60	1.0	n/a	n/a

Voltage Acceleration Factor (VAF) for HVLT on this process is 55.

NOTE:
FIT = Failure in Time. 1 FIT = 1 failure per 1×10^9 device hours.

Failure Analysis

A. 1 leakage − 0.5 eV
B. 2 leakage − 1.0 eV
C. 1 leakage − 0.5 eV
D. 1 SBCL − 0.6 eV
1 passivation defect − 0.5 eV
E. 1 passivation defect − 0.5 eV

5C060

Device: 5C060
Organization: 16 Macrocells
Pinout: 24 Lead, 300 mil CERDIP and PDIP (28 Lead PLCC)
Die Size: 135 x 141 mils
Transistor Count: ~14K
Process: CHMOS IIE, P424
Programming Voltage: 12.5V
Technology: CMOS

Table 1. Reliability Data

Package	Burn-In 48 Hours	125°C Dynamic Lifetest 168 Hours	125°C Dynamic Lifetest 500 Hours	125°C Dynamic Lifetest 1K Hours
CERDIP	0/3969 1/2500	0/3969 3/2499	0/371 0/100	0/354 0/99
PDIP		0/351	0/351	0/351
TOTALS	1/6469 A	3/6819 B	0/882	0/804

Additional Readouts:
CERDIP 0/99 @ 2K Hours Lifetest
PDIP 0/351 @ 2K Hours Lifetest

Package	125°C High Voltage Dynamic Lifetest (6.5V) 48 Hours	168 Hours	500 Hours
CERDIP	0/224 0/100	0/201 0/100	2/198 0/100
TOTALS	0/324	0/301	2/298 C

Package	Data Retention Bake (CERDIP @ 250°C) 48 Hours	168 Hours	500 Hours
CERDIP	0/203 0/50	0/202 0/50	0/202 0/50
TOTALS	0/253	0/252	0/252

Additional Readouts:
CERDIP 0/127 @ 1K Hours, 250°C Bake

Table 2. Additional Qualification Stress Information

Package	Temperature Cycling (Condition "C"—150°C to −65°C)		
	200 Cycles	500 Cycles	1K Cycles
CERDIP	0/307	1/307	0/302
PDIP	0/350	0/350	—
TOTALS	0/657	1/657 D	0/302

Package	Thermal Shock (Condition "C"—150°C to −65°C)		
	50 Cycles	200 Cycles	500 Cycles
CERDIP	0/155	0/155	1/155
TOTALS	0/155	0/155	1/155 E
Additional Readouts: CERDIP	0/154 @ 1K Cycles		

Package	Steam (121°C, 2 ATM)	
	96 Hours	168 Hours
PDIP	0/100	0/100
PLCC	0/150	0/150
TOTALS	0/250	0/250
Additional Readouts: PDIP	0/100 @ 336 Hours of Steam	

Table 3. Failure Rate Predictions (5C060-CERDIP-Fab 1)

Actual Device Hrs	Ea (eV)	Equivalent Device Hrs 55°C	Equivalent Device Hrs 70°C	# Fail	Fail Rate in FITs (60% UCL) 55°C	Fail Rate in FITs (60% UCL) 70°C
1.26E + 06	0.3 LT	6.37E + 06	4.24E + 06	2		
1.51E + 05	0.3 HVLT * VAF	4.20E + 07	2.79E + 07	2		
		Total 0.3 eV Failures =		4	108.6	163.2
1.26E + 06	0.5 LT	1.88E + 07	9.54E + 06	1		
1.51E + 05	0.5 HVLT	2.25E + 06	1.14E + 06	0		
		Total 0.5 eV Failures =		1	96.0	189.1
1.26E + 06	0.6 LT	3.23E + 07	1.43E + 07	0		
1.51E + 05	0.6 HVLT	3.86E + 06	1.71E + 06	0		
		Total 0.6 eV Failures =		0	0.0	0.0
1.26E + 06	1.0 LT	2.81E + 08	7.24E + 07	0		
1.51E + 05	1.0 HVLT	3.36E + 07	8.66E + 06	0		
		Total 1.0 eV Failures =		0	0.0	0.0
		Combined Failure Rate (FITs) =			204.6	352.2
		48 Hour BI Infant Mortality = 1/6469 = 0.0155% = 313 DPM @ 60% Confidence				

Other Data (CERDIP)

Theta Ja =	54°C/W	**Temp with Theta Ja**	
Theta Jc =	17°C/W	**Degree Kelvin**	
V_{CC} =	5.25V	T(55°C) =	350.68 K
I_{CC} @ 55°C =	80 mA	T(70°C =	365.68 K
I_{CC} @ 70°C =	80 mA	T(125°C) =	419.26 K
I_{CC} @ 125°C =	75 mA	T(250°C) =	523 K

Boltzman's Constant = K = 8.62×10^{-5} eV/K

Thermal Acceleration Factors—

Lifetest (LT) and High Voltage Lifetest (HVLT)			Bake (250°C)		
Activation Energy	**55°C**	**70°C**	**Activation Energy**	**55°C**	**70°C**
0.3	5.07	3.37	0.3	n/a	n/a
0.5	14.94	7.58	0.5	727.61	335.91
0.6	25.66	11.37	0.6	2718.18	1075.15
1.0	223.24	57.52	1.0	n/a	n/a

Other Data (PDIP)

Theta Ja =	67°C/W	**Temp with Theta Ja**	
Theta Jc =	22°C/W	**Degree Kelvin**	
V_{CC} =	5.25V	T(55°C) =	356.14 K
I_{CC} @ 55°C =	80 mA	T(70°C =	371.14 K
I_{CC} @ 70°C =	80 mA	T(125°C) =	424.38 K
I_{CC} @ 125°C =	75 mA	T(140°C) =	413 K

Boltzman's Constant = K = 8.62×10^{-5} eV/K

Thermal Acceleration Factors—

Lifetest (LT) and High Voltage Lifetest (HVLT)			Bake (140°C)		
Activation Energy	**55°C**	**70°C**	**Activation Energy**	**55°C**	**70°C**
0.3	4.81	3.24	0.3	n/a	n/a
0.5	13.70	7.10	0.5	38.00	17.54
0.6	23.13	10.50	0.6	78.65	31.11
1.0	187.72	50.36	1.0	n/a	n/a

Other Data (PLCC)

Theta Ja =	61°C/W	**Temp with Theta Ja**		
Theta Jc =	20°C/W	**Degree Kelvin**		
V_{CC} =	5.25V		T(55°C) =	353.62 K
I_{CC} @ 55°C =	80 mA		T(70°C) =	368.62 K
I_{CC} @ 70°C =	80 mA		T(125°C) =	422.02 K
I_{CC} @ 125°C =	75 mA		T(140°C) =	413 K

Boltzman's Constant = K = 8.62×10^{-5} eV/K

Thermal Acceleration Factors—

Lifetest (LT) and High Voltage Lifetest (HVLT)			Bake (140°C)		
Activation Energy	**55°C**	**70°C**	**Activation Energy**	**55°C**	**70°C**
0.3	4.92	3.30	0.3	n/a	n/a
0.5	14.25	7.31	0.5	38.00	17.54
0.6	24.25	10.89	0.6	78.65	31.11
1.0	203.16	53.51	1.0	n/a	n/a

Voltage Acceleration Factor (VAF) for HVLT on this process is 55.

NOTE:
FIT = Failure in Time. 1 FIT = 1 failure per 1×10^9 device hours.

Failure Analysis

A. 1 oxide defect − 0.3 eV

B. 2 oxide defects − 0.3 eV
1 metal defect − 0.5 eV

C. 2 oxide defects − 0.3 eV

D. 1 passivation defect − 0.5 eV

E. 1 passivation defect − 0.5 eV

Device:	5C090
Organization:	24 Macrocells
Pinout:	40 Lead, 600 mil CERDIP and PDIP (44 Lead PLCC)
Die Size:	166 x 181 mils
Transistor Count:	~30K
Process:	CHMOS IIE, P424
Programming Voltage:	12.5V
Technology:	CMOS

Table 1. Reliability Data

Package	Burn-In 48 Hours	125°C Dynamic Lifetest		
		168 Hours	500 Hours	1K Hours
CERDIP				
1987	1/2123	2/2085	0/170	0/170
1989	3/3934	3/3931	0/190	0/190
1991	0/2400	0/2399		
1992	0/1200	0/1196		
TOTALS	4/9657	5/9611	0/360	0/360
Additional Readouts:				
CERDIP	0/265 @ 2K Hours LT (1987 and 1989 material)			

Package	125°C High Voltage Dynamic Lifetest (6.5V)		
	48 Hours	168 Hours	500 Hours
CERDIP			
1987	0/170	1/170	0/156
1989	0/195	0/195	0/195
1991	0/399	0/399	0/399
1992	0/200	0/100	0/100
TOTALS	0/964	1/864 (C)	0/850

Package	Data Retention Bake (CERDIP @ 250°C)		
	48 Hours	168 Hours	500 Hours
CERDIP			
1987	0/66	0/66	0/66
1989	0/99	0/99	0/99
TOTALS	0/165	0/165	0/165

Table 2. Additional Qualification Stress Information

Package	Temperature Cycling (Condition "C"—150°C to −65°C)		
	200 Cycles	500 Cycles	1K Cycles
CERDIP	0/149	0/141	1/67 D

Package	Thermal Shock (Condition "C"—150°C to −65°C)		
	50 Cycles	200 Cycles	500 Cycles
CERDIP	0/50	0/50	1/50 E

Package	85°C/85% Relative Humidity		
	168 Hours	500 Hours	1K Hours
PLCC	0/172	0/172	0/172
Additional Readouts PLCC	0/172 @ 2K Hours		

Package	Steam (121°C, 2 ATM)	
	96 Hours	168 Hours
PDIP	0/153	0/153
PLCC	3/474 F	0/471
TOTALS	3/627	0/624
Additional Readouts: PLCC	0/300 @ 500 Hours of Steam	

Table 3. Failure Rate Predictions (5C090-CERDIP-Fab 1)

Actual Device Hrs	Ea (eV)	Equivalent Device Hrs 55°C	Equivalent Device Hrs 70°C	# Fail	Fail Rate in FITs (60% UCL) 55°C	Fail Rate in FITs (60% UCL) 70°C
1.43E + 06	0.3 LT	7.54E + 06	4.95E + 06	0		
2.77E + 05	0.3 HVLT * VAF	8.04E + 07	5.28E + 07	1		
			Total 0.3 eV Failures =	1	23.0	35.0
1.43E + 06	0.5 LT	2.28E + 07	1.13E + 07	0		
2.77E + 05	0.5 HVLT	4.43E + 06	2.20E + 06	0		
			Total 0.5 eV Failures =	0	33.6	67.6
1.43E + 06	0.6 LT	3.97E + 07	1.72E + 07	2		
2.77E + 05	0.6 HVLT	7.70E + 07	3.33E + 06	0		
			Total 0.6 eV Failures =	2	65.5	151.6
1.43E + 06	1.0 LT	3.64E + 08	8.99E + 07	0		
2.77E + 05	1.0 HVLT	7.07E + 07	1.74E + 07	0		
			Total 1.0 eV Failures =	0	0.0	0.0
			Combined Failure Rate (FITs) =		122.0	254.2
48 Hour BI Infant Mortality = 4/7257 = 0.0554% = 722 DPM @ 60% Confidence						

Table 4. Failure Rate Predictions (CERDIP 5C090-Fab 4)

Actual Device Hrs	Ea (eV)	Equivalent Device Hrs		# Fail	Fail Rate in FITs (60% UCL)	
		55°C	70°C		55°C	70°C
4.3E + 5 2.3E + 5	0.3 LT 0.3 HVLT * VAF	2.3E + 6 3.1E + 7	1.5E + 6 2.7E + 7			
			Total 0.3 eV Failures =	0	0	0
4.3E + 5 2.3E + 5	0.5 LT 0.5 HVLT	6.9E + 6 3.6E + 6	3.4E + 6 1.8E + 6			
			Total 0.5 eV Failures =	0	87	176
4.3E + 5 2.3E + 5	0.6 LT 0.6 HVLT	1.2E + 7 6.3E + 6	5.2E + 6 2.7E + 6			
			Total 0.6 eV Failures =	0	0	0
4.3E + 5 2.3E + 5	1.0 LT 1.0 HVLT	1.1E + 8 5.8E + 7	2.7E + 7 1.4E + 7			
			Total 1.0 eV Failures =	0	0	0
			Combined Failure Rate (FITs) =		87	176
48 Hour BI Infant Mortality = 0/4199 = 0.00% = 219 DPM @ 60% Confidence						

Other Data (CERDIP)

		Temp with Theta Ja Degree Kelvin	
Theta Ja =	36°C/W		
Theta Jc =	13°C/W		
V_{CC} =	5.25V	T(55°C) =	345.01 K
I_{CC} @ 55°C =	90 mA	T(70°C) =	360.01 K
I_{CC} @ 70°C =	90 mA	T(125°C) =	413.12 K
I_{CC} @ 125°C =	80 mA	T(250°C) =	523 K

Boltzman's Constant = K = 8.62×10^{-5} eV/K

Thermal Acceleration Factors—

Lifetest (LT) and High Voltage Lifetest (HVLT)			Bake (250°C)		
Activation Energy	55°C	70°C	Activation Energy	55°C	70°C
0.3	5.27	3.46	0.3	n/a	n/a
0.5	15.96	7.93	0.5	727.61	335.91
0.6	27.78	11.99	0.6	2718.18	1075.15
1.0	254.79	62.82	1.0	n/a	n/a

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Other Data (PDIP)

Theta Ja =	48°C/W	**Temp with Theta Ja**	
Theta Jc =	16°C/W	**Degree Kelvin**	
V_{CC} =	5.25V	T(55°C) =	350.68 K
I_{CC} @ 55°C =	90 mA	T(70°C) =	365.68 K
I_{CC} @ 70°C =	90 mA	T(125°C) =	418.16 K
I_{CC} @ 125°C =	80 mA	T(140°C) =	413 K

Boltzman's Constant = K = 8.62×10^{-5} eV/K

Thermal Acceleration Factors—

Lifetest (LT) and High Voltage Lifetest (HVLT)			Bake (140°C)		
Activation Energy	**55°C**	**70°C**	**Activation Energy**	**55°C**	**70°C**
0.3	4.96	3.30	0.3	n/a	n/a
0.5	14.41	7.31	0.5	38.00	17.54
0.6	24.56	10.89	0.6	78.65	31.11
1.0	207.54	53.47	1.0	n/a	n/a

Other Data (PLCC)

Theta Ja =	48°C/W	**Temp with Theta Ja**	
Theta Jc =	16°C/W	**Degree Kelvin**	
V_{CC} =	5.25V	T(55°C) =	350.68 K
I_{CC} @ 55°C =	90 mA	T(70°C) =	365.68 K
I_{CC} @ 70°C =	90 mA	T(125°C) =	418.16 K
I_{CC} @ 125°C =	80 mA	T(140°C) =	413 K

Boltzman's Constant = K = 8.62×10^{-5} eV/K

Thermal Acceleration Factors—

Lifetest (LT) and High Voltage Lifetest (HVLT)			Bake (140°C)		
Activation Energy	**55°C**	**70°C**	**Activation Energy**	**55°C**	**70°C**
0.3	4.96	3.30	0.3	n/a	n/a
0.5	14.41	7.31	0.5	38.00	17.54
0.6	24.56	10.89	0.6	78.65	31.11
1.0	207.54	53.47	1.0	n/a	n/a

Voltage Acceleration Factor (VAF) for HVLT on this process is 55.

NOTE:
FIT = Failure in Time. 1 FIT = 1 failure per 1×10^9 device hours.

Failure Analysis

A. 1 SBCL − 0.6 eV
 1 polysilicon defect − 0.5 eV
 1 metal defect − 0.5 eV
 1 oxide defect − 0.3 eV
B. 2 MBCL − 0.6 eV
C. 1 oxide defect − 0.3 eV
D. 1 open metal − 0.5 eV
E. 1 hermeticity
F. 3 passivation defects − 0.5 eV

5C180

Device:	5C180
Organization:	48 Macrocells
Pinout:	68 Lead PLCC, and PGA
Die Size:	265 x 182 mils
Transistor Count:	~60K
Process:	CHMOS IIE, P424
Programming Voltage:	12.5V
Technology:	CMOS

Table 1. Reliability Data

Package	Burn-In 48 Hours	125°C Dynamic Lifetest		
		168 Hours	500 Hours	1K Hours
CERQUAD	0/378	0/376	0/102	0/102
TOTALS	0/378	0/376	0/102	0/102

Package	125°C High Voltage Dynamic Lifetest (6.5V)		
	48 Hours	168 Hours	500 Hours
CERQUAD	0/50	0/43	0/39
TOTALS	0/50	0/43	0/39

Package	Data Retention Bake (CERDIP @ 250°C)		
	48 Hours	168 Hours	500 Hours
CERQUAD	0/107	0/100	0/100
TOTALS	0/107	0/100	0/100

Table 2. Additional Qualification Stress Information

Package	Temperature Cycling (Condition "C"—150°C to −65°C)		
	200 Cycles	500 Cycles	1K Cycles
PGA PLCC	0/128 0/123	0/128 0/123	0/128 0/123
TOTALS	0/251	0/251	0/251

Package	Thermal Shock (Condition "C"—150°C to −65°C)		
	50 Cycles	200 Cycles	500 Cycles
PGA	0/117	0/117	0/177
TOTALS	0/117	0/117	0/177

Package	Steam (121°C, 2 ATM)	
	96 Hours	168 Hours
PLCC	0/77	0/77
TOTALS	0/77	0/77
Additional Readouts: PLCC	0/77 @ 500 Hours of Steam	

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Table 3. Failure Rate Predictions (5C180-CERQUAD)

Actual Device Hrs	Ea (eV)	Equivalent Device Hrs 55°C	Equivalent Device Hrs 70°C	# Fail	Fail Rate in FITs (60% UCL) 55°C	Fail Rate in FITs (60% UCL) 70°C
1.30E + 05	0.3 LT	5.81E + 05	3.94E + 05	0		
5.03E + 04	0.3 HVLT * VAF	1.24E + 07	8.39E + 06	0		
			Total 0.3 eV Failures =	0	70.6	104.2
1.30E + 05	0.5 LT	1.58E + 06	8.25E + 05	0		
5.03E + 04	0.5 HVLT	6.11E + 05	3.20E + 05	0		
			Total 0.5 eV Failures =	0	0.0	0.0
1.30E + 05	0.6 LT	2.60E + 06	1.19E + 06	0		
5.03E + 04	0.6 HVLT	1.01E + 06	4.62E + 05	0		
			Total 0.6 eV Failures =	0	0.0	0.0
1.30E + 05	1.0 LT	1.91E + 07	5.24E + 06	0		
5.03E + 04	1.0 HVLT	7.41E + 06	2.03E + 06	0		
			Total 1.0 eV Failures =	0	0.0	0.0
			Combined Failure Rate (FITs) =		70.6	104.2
48 Hour BI Infant Mortality = 0/378 = 0.0000% = 2425 DPM @ 60% Confidence						

Other Data (CERQUAD)

		Temp with Theta Ja Degree Kelvin	
Theta Ja =	42°C/W		
Theta Jc =	14°C/W		
V_{CC} =	5.25V	T(55°C) =	358.87 K
I_{CC} @ 55°C =	140 mA	T(70°C) =	373.87 K
I_{CC} @ 70°C =	140 mA	T(125°C) =	424.46 K
I_{CC} @ 125°C =	120 mA	T(250°C) =	523 K

Boltzman's Constant = $K = 8.62 \times 10^{-5}$ eV/K

Thermal Acceleration Factors—

Lifetest (LT) and High Voltage Lifetest (HVLT) Activation Energy	55°C	70°C	Bake (250°C) Activation Energy	55°C	70°C
0.3	4.47	3.03	0.3	n/a	n/a
0.5	12.14	6.35	0.5	727.61	335.91
0.6	19.99	9.19	0.6	2718.18	1075.15
1.0	147.28	40.29	1.0	n/a	n/a

Other Data (PLCC)

Theta Ja =	38°C/W	**Temp with Theta Ja Degree Kelvin**	
Theta Jc =	14°C/W		
V_{CC} =	5.25V	T(55°C) =	355.93 K
I_{CC} @ 55°C =	140 mA	T(70°C) =	370.93 K
I_{CC} @ 70°C =	140 mA	T(125°C) =	421.94 K
I_{CC} @ 125°C =	120 mA	T(140°C) =	413 K

Boltzman's Constant = K = 8.62×10^{-5} eV/K

Thermal Acceleration Factors—

Lifetest (LT) and High Voltage Lifetest (HVLT)			Bake (140°C)		
Activation Energy	55°C	70°C	Activation Energy	55°C	70°C
0.3	4.61	3.11	0.3	n/a	n/a
0.5	12.78	6.62	0.5	38.00	17.54
0.6	21.28	9.65	0.6	78.65	31.11
1.0	163.38	43.76	1.0	n/a	n/a

Other Data (PGA)

Theta Ja =	28.5°C/W	**Temp with Theta Ja Degree Kelvin**	
Theta Jc =	4°C/W		
V_{CC} =	5.25V	T(55°C) =	348.95 K
I_{CC} @ 55°C =	140 mA	T(70°C) =	363.95 K
I_{CC} @ 70°C =	140 mA	T(125°C) =	415.96 K
I_{CC} @ 125°C =	120 mA	T(250°C) =	523 K

Boltzman's Constant = K = 8.62×10^{-5} eV/K

Thermal Acceleration Factors—

Lifetest (LT) and High Voltage Lifetest (HVLT)			Bake (250°C)		
Activation Energy	55°C	70°C	Activation Energy	55°C	70°C
0.3	4.98	3.30	0.3	n/a	n/a
0.5	14.53	7.33	0.5	727.61	335.91
0.6	24.82	10.91	0.6	2718.18	1075.15
1.0	211.14	53.68	1.0	n/a	n/a

Voltage Acceleration Factor (VAF) for HVLT on this process is 55.

NOTE:
FIT = Failure in Time. 1 FIT = 1 failure per 1×10^9 device hours.

APPENDIX A

Failure Rate Calculations for 60% Upper Confidence Level

Step 1. Collect burn-in and lifetest data for each lot after 48 hours of burn-in through lifetest for each lot.

Step 2. Determine the failure mechanism and assign an activation energy (E_A) for each failure, except those occurring during the first 48 hrs.

Failure Mechanism Activation Energies Relevant to EPROMs

Failure Mode	Activation Energy
Defective bit charge gain/loss	0.6 eV
Oxide breakdown	0.3 eV
Silicon defects	0.3 eV
Contamination	1.0 eV–1.2 eV
Intrinsic charge loss	1.4 eV

Step 3. Calculate the total number of device hours accumulated beyond 48 hours of burn-in.

NOTE:

The first 48 hours of burn-in at either 5.25V or 6.5V measure infant mortality and are not included in the failure rate calculation. Monitor lots will use only 5.25V data for the infant mortality evaluation (IME). See monitor flow chart, Figure 1.

Example: 125°C Burn-In/Lifetest for a 2 lot sample

$$\frac{\#\ \text{failures}}{\text{total}\ \#\ \text{devices}}$$

	48 Hours	168 Hours	500 Hours	1K Hours	2K Hours
Lot #1	0/1000	1/1000	0/999	0/998	0/994
Lot #2	0/221	0/201	1/201	1/100	0/99
Totals	0/1221	1/1201	1/1200	1/1098	0/1093

Actual Device Hours = Σ (Number of Devices in Stress Interval) (Number of Hours in Stress Interval)

= 1201 (168 hrs−48 hrs) + 1200 (500 hrs−168 hrs)

+ 1098 (1000 hrs−500 hrs) + 1093 (2000 hrs−1000 hrs)

= 1201 (120 hrs) + 1200 (332 hrs) + 1098 (500 hrs)

+ 1093 (1000 hrs)

2.185 x 10^6 Device Hours

Step 4. Use E_A tables to find the equivalent device hours at a desired temperature for each activation energy (failure mechanism), or use the Arrhenius relation.

$$R = A \exp\left[\frac{-E_A}{KT}\right]$$

K = 8.617×10^{-5} eV/°K (Boltzmann's constant)
A = proportionality constant
R = mean rate to failure
E_A = activation energy
T = temperature in Kelvin

$$\frac{R_1}{R_2} = \frac{A_1 \exp\left[\frac{-E_A}{KT_1}\right]}{A_2 \exp\left[\frac{-E_A}{KT_2}\right]} = \exp\left[\left(\frac{E_A}{K}\right)\left(\frac{1}{T_2} - \frac{1}{T_1}\right)\right]$$

Where $A_1 = A_2 = A$ for the same failure mechanism (i.e., same E_A)

Where R_1 and R_2 are rates for a normal operating temp and an elevated temperature respectively.

$$R_1 = R_2 \times \exp\left[\left(\frac{E_A}{K}\right)\left(\frac{1}{T_2} - \frac{1}{T_1}\right)\right]$$

However, since rate (R) has the units 1/time, we can think in terms of time to one failure or MTBF.

Thus:

$$R_1 = \frac{1}{t_1} \text{ where } t_1 = \text{MTBF at some temperature } T_1$$

and:

$$R_2 = \frac{1}{t_2} \text{ where } t_2 = \text{MTBF at some temperature } T_2$$

Thus the Arrhenius relation becomes:

$$\frac{1}{t_1} = \frac{1}{t_2} \times \exp\left[\frac{E_A}{K}\left(\frac{1}{T_2} - \frac{1}{T_1}\right)\right]$$

or:

$$t_1 = \exp\left[\frac{E_A}{K}\left(\frac{1}{T_1} - \frac{1}{T_2}\right)\right] \times t_2$$

We then define the Acceleration Factor as:

$$\text{A.F.} = \frac{t_1}{t_2} = \exp\left[\frac{E_A}{K}\left(\frac{1}{T_1} - \frac{1}{T_2}\right)\right]$$

For example: For $E_A = 0.6$ eV, $T_2 = 398$°K, $T_1 = 328$°K

$$t_1 = 41.7\ t_2$$

Therefore, one hour at 125°C is equivalent to 41.7 hours at 55°C for a failure mechanism of activation energy E_A = 0.6 eV. Then 41.7 is the thermal acceleration factor for time.

NOTE:

The Arrhenius Plot (Figure 2, Page 3) is simply ln (Acceleration Factor) vs. 1/Temperature normalized for an MTBF of one hour at 250°C (T_2). This plot can also be used to determine the acceleration factor between two temperatures other than 250°C.

For example: For a 0.3 eV failure at 125°C, the acceleration factor is 8.1 relative to a 0.3 eV failure at 250°C. For a 0.3 eV failure at 25°C, the acceleration factor is 152 relative to 250°C. Therefore, the acceleration factor between 125°C and 25°C is:

$$\text{A.F.} = \frac{t_1}{t_2} = \frac{152}{8.1} = 18.7$$

Step 5. Organize the burn-in/lifetest data by E_A, Total Device Hours at the burn-in/lifetest temperature T_2, Thermal Acceleration Factors for each failure mechanism (E_A), Number of Failures for each failure mechanism, and the calculated equivalent device hours at the desired operating temperature T_1.

NOTE:

The rise in junction temperature due to the thermal resistivity of the package (θ_{JA}) must be added to the ambient temperature to arrive at the actual burn-in/lifetest temperatures.

$$T_{test} = T_J + T_{Ambient} = \theta_{JA}\,(\text{IV @ } T_{Ambient}) + T_{Ambient}$$

E_A (eV)	Total Device Hrs @ T_2	Acceleration Factors	# Fail	Equivalent Hours @ T_1
0.3	T.D.H.	X	N_1	X (T.D.H.)
0.6	T.D.H.	Y	N_2	Y (T.D.H.)
1.0	T.D.H.	Z	N_3	Z (T.D.H.)

The failure rates for individual failure mechanisms and the total combined failure rate can be predicted using the data table and the following formula:

$$\text{FITs} = \frac{\chi^2\,(n, \alpha)}{2T}\left(10^9\right)$$

Where χ^2 (n, α) is the value of the chi-squared distribution for n degrees of freedom and confidence level of α. The degrees of freedom, n = [2(# of failures) + 2] for this application. T is the total equivalent device hours at T_1. The total combined failure rate is just the sum of the individual failure rates for each failure mechanism.

For a 60% UCL (Upper Confidence Limit), the above formula converts to the following:

# Failures	FIT Rate (60% UCL)
0	$0.915 \times 10^9/T$
1	$2.02 \times 10^9/T$
2	$3.105 \times 10^9/T$
3	$4.17 \times 10^9/T$
3 < # < 15	$\left[\frac{1.049\,(\#\text{failures for a particular } E_A) + 1.0305}{T}\right]\left[10^9\right]$
> 15	$\frac{[0.2533 + \sqrt{(4 \times \#\text{Failed}) + 3}]^2}{4T}\left[10^9\right]$

Example 1:

Assume for this example, that I_{CC} active is 57 mA at $T_{Ambient}$ = 125°C and I_{CC} active is 60 mA at $T_{Ambient}$ = 55°C.

Also assume that θ_{JA} = 35°C/W.

Then,

T_2 = (35°C/W) (57 mA) (5V) + 125°C
≅ 135°C = 408°K

T_1 = (35°C/W) (60 mA) (5V) + 55°C
≅ 65°C = 338°K

E_A (eV)	Actual Device Hours @ 125°C	Acceleration Factors For 135°C to 65°C	Equivalent Hours at 55°C	# Fail	55°C FIT Rate
0.3	2.185 x 10^6	5.85	1.278 x 10^7	0	81
0.6	2.185 x 10^6	34.18	7.468 x 10^7	2	42
1.0	2.185 x 10^6	359.93	7.864 x 10^8	1	3
			Total Combined Failure Rate =		126 FITs

Example 2:

Assume than an additional lot of 800 CHMOS III-E devices is burned in using a 6.5V lifetest as shown below. Assume further that the one failure shown at 168 hours is a 0.3 eV oxide failure. Using Table 2 below, a voltage acceleration factor of 26 results from a 1.25V voltage overstress (5.25V to 6.5V).

	48 Hours	168 Hours	500 Hours
Lot #3	0/800	1/800	0/799

Actual Device Hours = 800 (48 hrs−0 hrs) + 800 (168 hrs−48 hrs) + 799 (500 hrs−168 hrs)
= 3.997 x 10^5

Table 2. Time-Dependent Oxide Failure Voltage Accelerations Relative to 5.25V

Type	Supply Voltage (Volts)	Oxide Thickness (Å)	Operating Stress (MV/cm)	Lifetest Stress Voltage			
				5.5V	6.0V	6.5V	7.0V
CHMOS III-E	5	235	2.15	1.9	7.0	26	93

ASSUMES:
1. Failure rate calculations use the appropriate acceleration factor for stress voltage versus 5.25V operating voltage (conservative).
2. Reference [2] E. Nelson Anolick.

55°C equivalent hours for E_A = 0.3 eV are added to the 6.5V burn-in/lifetest 55°C equivalent hours.

125°C Burn-In/Lifetest	E_A (eV)	Actual Device Hours @ 125°C	Acceleration Factors for 135°C to 65°C	Equivalent Hours @55°C
5.25V	0.3	2.185×10^6	5.85	1.278×10^7
6.5V	0.3	3.997×10^5	(5.85 x 26)	6.079×10^7
Total Equivalent Device Hours for 0.3 eV Failures = 7.357×10^7				

The following failure rate predictions include the total equivalent 55°C, E_A = 0.3 eV device hours found above:

E_A (eV)	Actual Device Hours @ 125°C	Acceleration Factors for 135°C to 65°C	Equivalent Hours @55°C	# Fail	55°C FIT Rate
0.3 ELT 0.3 HVELT	2.185×10^6 3.997×10^5	5.85 (5.85 x 26)	7.357×10^7	1	27
0.6 ELT 0.6 HVELT	2.185×10^6 3.997×10^5	34.18 34.18	8.834×10^7	2	35
1.0 ELT 1.0 HVELT	2.185×10^6 3.997×10^5	359.93 359.93	9.303×10^8	1	2
			Total Combined Failure Rate =		84 FITs

NOTES:
1. Additional information on calculating failure rates is contained in the April 2, 1984 International Reliability Physics Symposium editorial entitled "Calculating Failure Rates from Stress Data" by Robert M. Alexander.
2. 1 FIT = 1 Failure Unit = 0.0001%/1K hours.

Development Tools Support

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Development Tools Support

MARYANN L. LINDQUIST
PRODUCT MARKETING ENGINEER

November 1993

Order Number: 297217-002

Development Tools Support

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FPGA/PLD PROGRAMMING SUPPORT

Vendor	Product	Product Description	Module	Devices Supported				
				FLEXlogic	iPLD	85Cxxx	5Cxxx	5ACxxx
Advin Systems Inc. 1050-L Duane Ave. Sunnyvale, CA 94086 (800) 627-2456 or (408) 243-7000 FAX (408) 736-2503	PILOT-U84	84-PIN Universal Programmer	PX-20 PX-28 PX-44 AM-1800 AM-78	iFX780(11) iFX740(11)	**DIP:** iPLD610 iPLD910 iPLD22V10 **PLCC:** iPLD610 iPLD910 iPLD22V10	**DIP:** 85C060, 85C090 85C220, 85C224 85C22V10 **PLCC:** 85C060(2), 85C090(3) 85C220(1), 85C224(2) 85C22V10(2)	**DIP:** 5C031, 5C032 5C060, 5C090 **PLCC:** 5C180(4), 5C060(2) 5C090(3)	**DIP:** 5AC312, 5AC324 **PLCC:** 5AC312(2) 5AC324(3)
	PILOT-U40	40-PIN Universal Programmer	PX-20 PX-28 PX-44 AM-1800 AM-78	iFX780(11) iFX740(11)	**DIP:** iPLD610 iPLD910 **PLCC:** iPLD610 iPLD910	**DIP:** 85C060, 85C090, 85C220, 85C224, 85C22V10 **PLCC:** 85C060(2), 85C090(3), 85C220(1), 85C224(2), 85C22V10(2)	**DIP:** 5C031, 5C032 5C060, 5C090 **PLCC:** 5C180(4), 5C060(2) 5C090(3)	**DIP:** 5AC312, 5AC324 **PLCC:** 5AC312(2) 5AC324(3)
B & C Microsystems Inc. 750 N Pastoria Ave. Sunnyvale, CA 94086 (408) 730-5511 FAX (408) 730-5521 BBS (408) 730-2317	PROTEUS -UP40	40 Pin Universal Programmer (DIP40)			**DIP:** PLD610 PLD910 **PLCC:** PLD610 PLD910	**DIP:** 85C060, 85C090 85C220 **PLCC:** 85C060, 85C090 85C220	**DIP:** 5C031, 5C032 5C060, 5C090 **PLCC:** 5C060, 5C090	**DIP:** 5AC312 5AC324 **PLCC:** 5AC312 5AC324
	PROTEUS -UPLC40	40 Pin Universal Programmer (DIP48 & PLCC84)			**DIP:** PLD610 PLD910 **PLCC:** PLD610 PLD910	**DIP:** 85C060, 85C090 85C220 **PLCC:** 85C060, 85C090 85C220	**DIP:** 5C031, 5C032 5C060, 5C090 **PLCC:** 5C060, 5C090	**DIP:** 5AC312 5AC324 **PLCC:** 5AC312 5AC324

FPGA/PLD PROGRAMMING SUPPORT (Continued)

Vendor	Product	Product Description	Module	Devices Supported				
				FLEXlogic	iPLD	85Cxxx	5Cxxx	5ACxxx
	PROTEUS -UPLC56	56 Pin Universal Programmer (DIP48 & PLCC84)			**DIP:** PLD610 PLD910 **PLCC:** PLD610 PLD910	**DIP:** 85C060, 85C090 85C220 **PLCC:** 85C060, 85C090 85C220	**DIP:** 5C031, 5C032 5C060, 5C090 **PLCC:** 5C060, 5C090	**DIP:** 5AC312 5AC324 **PLCC:** 5AC312 5AC324
	PROTEUS -UPLC72	72 Pin Universal Programmer (DIP48 & PLCC84)			**DIP:** PLD610 PLD910 **PLCC:** PLD610 PLD910	**DIP:** 85C060, 85C090 85C220 **PLCC:** 85C060, 85C090 85C220	**DIP:** 5C031, 5C032 5C060, 5C090 **PLCC:** 5C060, 5C090	**DIP:** 5AC312 5AC324 **PLCC:** 5AC312 5AC324
	PROTEUS -UPLC88	88 Pin Universal Programmer (DIP48 & PLCC84)		iFX780	**DIP:** PLD610 PLD910 **PLCC:** PLD610 PLD910	**DIP:** 85C060, 85C090 85C220 **PLCC:** 85C060, 85C090 85C220	**DIP:** 5C031, 5C032 5C060, 5C090 **PLCC:** 5C060, 5C090	**DIP:** 5AC312 5AC324 **PLCC:** 5AC312 5AC324
BP Microsystems 1000 N Post Oak Road Houston, TX 77055-7237 (800) 225-2102 or (713) 688-4600 FAX (713) 688-0920 BBS (713) 688-9283	PLD-1128	28 Pins + PLCC Socket Converter (Only supports PLDs)			**DIP:** iPLD610 iPLD910 iPLD22V10 **PLCC:** iPLD610 iPLD910 iPLD22V10	**DIP:** 85C060, 85C090 85C220, 85C224 85C960 85C22V10 **PLCC:** 85C060, 85C090 85C220, 85C224 85C22V10 85C960	**DIP:** 5C031, 5C032 5C060, 5C090 **PLCC:** 5C060, 5C090 5C180	**DIP:** 5AC312 5AC324 **PLCC:** 5AC312 5AC324

FPGA/PLD PROGRAMMING SUPPORT (Continued)

Vendor	Product	Product Description	Module	Devices Supported				
				FLEXlogic	iPLD	85Cxxx	5Cxxx	5ACxxx
	CP-1128	28 Pins + PLCC Socket Converter (Supports PLDs, EPROMs, and EEPROMs)			**DIP:** iPLD610 iPLD910 iPLD22V10 **PLCC:** iPLD610 iPLD910 iPLD22V10	**DIP:** 85C060, 85C090 85C220, 85C224 85C960 85C22V10 **PLCC:** 85C060, 85C090 85C220, 85C224 85C960 85C22V10	**DIP:** 5C031, 5C032 5C060, 5C090 **PLCC:** 5C060, 5C090 5C180	**DIP:** 5AC312 5AC324 **PLCC:** 5AC312 5AC324
	BP-1200	Supports up to 240 Pins (both PQFP and PLCC)		iFX780	**DIP:** iPLD610 iPLD910 iPLD22V10 **PLCC:** iPLD610 iPLD910 iPLD22V10	**DIP:** 85C060, 85C090 85C220, 85C224 85C960 85C22V10 **PLCC:** 85C060, 85C090 85C220, 85C224 85C960 85C22V10	**DIP:** 5C031, 5C032 5C060, 5C090 **PLCC:** 5C060, 5C090 5C180	**DIP:** 5AC312 5AC324 **PLCC:** 5AC312 5AC324
BP Microsystems (Continued)	PLD-1100	20/24 Pins + PLCC Socket Converters			**DIP:** PLD610 PLD22V10 **PLCC:** PLD610 PLD22V10	**DIP:** 85C060, 85C090 85C220 85C22V10 **PLCC:** 85C060, 85C090 85C220 85C22V10	**DIP:** 5C031, 5C032 5C060 **PLCC:** 5C060	**DIP:** 5AC312 5AC324 **PLCC:** 5AC312

FPGA/PLD PROGRAMMING SUPPORT (Continued)

Vendor	Product	Product Description	Module	Devices Supported				
				FLEXlogic	iPLD	85Cxxx	5Cxxx	5ACx
Bytek Corp. Instrument Systems Div. 543 N.W. 77th Street Boca Raton, FL 33487 (800) 523-1565 (407) 994-3520 FAX (407) 994-3615	135H-U	Universal MULTIPROGRAMMER	UNICEL w/LTA00C		**DIP:** iPLD610 iPLD910	**DIP:** 85C220, 85C224 85C060, 85C090	**DIP:** 5C031, 5C032 5C060, 5C090	**DIP:** 5AC31
	145H-U	Logic Programmer			**DIP:** iPLD610 iPLD910 **PLCC:** iPLD610 iPLD910	**DIP:** 85C220 85C224 85C060 85C090	**DIP:** 5C031, 5C032 5C060, 5C090	**DIP:** 5AC31

FPGA/PLD PROGRAMMING SUPPORT (Continued)

Vendor	Product	Product Description	Module	Devices Supported				
				FLEXlogic	iPLD	85Cxxx	5Cxxx	5ACxxx
Data I/O 10525 Willows Road, N.E. P.O. Box 97046 Redmond, WA 98073 (800) 247-5700 (206) 881-6444 FAX (206) 882-1043	UNISITE 40/48	Univ. 20 to 68 Pins-CHIPSITE for PLCC	SITE 40/48		**DIP:** iPLD610 iPLD910	**DIP:** 85C220, 85C224 85C060, 85C090	**DIP:** 5C031, 5C032 5C060, 5C090	**DIP:** 5AC312, 5AC324[5]
			CHIPSITE		**PLCC:** iPLD610 iPLD910	**PLCC:** 85C220, 85C224 85C060, 85C090	**PLCC:** 5C060, 5C090 5C180	**PLCC:** 5AC312 5AC324
			PPI Base	iFX780				
			PPI Base with Adaptor #0527	iFX780				
	Model 2900	Univ. 44 Pin			**DIP:** iPLD610 iPLD910 **PLCC:** iPLD610 iPLD910	**DIP:** 85C220, 85C224 85C060, 85C090 **PLCC:** 85C220, 85C224 85C060, 85C090	**DIP:** 5C031, 5C032 5C060, 5C090 **PLCC:** 5C060, 5C090 5C180	**DIP:** 5AC312, 5AC324[5] **PLCC:** 5AC312 5AC324
			PPI Base with Adaptor #0527	iFX780				
			PPI Base with Adaptor #0229	iFX780				
	Model 3900	Univ. 84 Pins			**DIP:** iPLD610 iPLD910 **PLCC:** iPLD610 iPLD910	**DIP:** 85C220, 85C224 85C060, 85C090 **PLCC:** 85C228, 85C224 85C060, 85C090	**DIP:** 5C031, 5C032 5C060, 5C090 **PLCC:** 5C060, 5C090 5C180	**DIP:** 5AC312 5AC324 **PLCC:** 5AC312 5AC324

FPGA/PLD PROGRAMMING SUPPORT (Continued)

Vendor	Product	Product Description	Module	Devices Supported				
				FLEXlogic	iPLD	85Cxxx	5Cxxx	5ACxxx
Elan Systems 365 Woodview Ave. Suite 700 Morganhill, CA 95037 (800) 541-3526 (408) 778-7267 FAX (408) 778-2597	5-145	Programmer + PLCC Socket Converters			**DIP:** iPLD610 iPLD910 **PLCC:** iPLD610 iPLD910		**DIP:** 5C032, 5C060 5C090, 5C031 **PLCC:** 5C060, 5C031 5C090, 5C032 5C180	**DIP:** 5AC312 5AC324 **PLCC:** 5AC312, 5AC324
Elan Digital Systems Ltd. Elan House, Little Park Farm Road, Segensworth West, Fareham, Hampshire P0155SJ 0489 579799 0489 577516	6000	Univ. Pin Driven Programmer			**DIP:** iPLD610 iPLD910 **PLCC:** iPLD610 iPLD910	**DIP:** 85C220, 85C224 85C22V10 85C060, 85C090 **PLCC:** 85C220, 85C224 85C22V10 85C060, 85C090	**DIP:** 5C031, 5C032 5C060, 5C090 **PLCC:** 5C031, 5C032 5C060, 5C090	**DIP:** 5AC312 **PLCC:** 5AC312
Logical Devices Inc. 692 S Military Trail Deerfield Beach, FL 33426 (800) 331-7766 (305) 428-6868 FAX (305) 974-8531	ALLPRO 88	Univ. 88-Pin + PLCC Socket Converter		iFX780 iFX780	**DIP:** iPLD610 iPLD910 **PLCC:** iPLD610 iPLD910	**DIP:** 85C220, 85C224 85C060, 85C090 **PLCC:** 85C220, 85C224 85C060, 85C090	**DIP:** 5C031, 5C032 5C060, 5C090 **PLCC:** 5C060, 5C090 5C180	**DIP:** 5AC312 5AC324 **PLCC:** 5AC312 5AC324

FPGA/PLD PROGRAMMING SUPPORT (Continued)

Vendor	Product	Product Description	Module	Devices Supported				
				FLEXlogic	iPLD	85Cxxx	5Cxxx	5ACxxx
Minato Electronics Inc. 3628 Madison Ave., #5 North Highlands, CA 95660 (916) 348-6066 FAX (916) 348-0926	1890A					**DIP:** 85C060, 85C090 85C220, 85C224 85C22V10 **PLCC:** 85C060, 85C090 85C220, 85C224 85C22V10	**DIP:** 5C031, 5C032 5C060, 5C090 5C121	**DIP:** 5AC312
Oliver Advanced Eng. 1146 N. Central Suite 380 Glendale, CA 91202 (818) 240-0080 FAX (818) 240-6131	OMNI-28	Univ. 28 Pins	OM-S-20 LCC OM-S-24 LCC		**DIP:** iPLD610 iPLD910 **PLCC:** iPLD610(7) iPLD910	**DIP:** 85C220, 85C224 85C060, 85C090 **PLCC:** 85C220(6), 85C224(7) 85C060, 85C090	**DIP:** 5C031, 5C032 5C060 **PLCC:** 5C060(7)	**DIP:** 5AC312
	OMNI-40	Univ. 40 Pin	OM-S-40 LCC		**DIP:** iPLD610 iPLD910 **PLCC:** iPLD610(7) iPLD910(8)	**DIP:** 85C220, 85C224 85C060, 85C090 **PLCC:** 85C220(6), 85C224(7) 85C060, 85C090	**DIP:** 5C031, 5C032 5C060, 5C090 5C121 **PLCC:** 5C090(8), 5C060(7)	
	OMNI-64	Univ. 68 Pins	OM-S-68 LCC		**DIP:** iPLD610 iPLD910 **PLCC:** iPLD610(7) iPLD910(8)	**DIP:** 85C220, 85C224 85C060, 85C090 **PLCC:** 85C220(6), 85C224(7) 85C060, 85C090	**DIP:** 5C031, 5C032 5C060, 5C090 5C121 **PLCC:** 5C090(8), 5C060(7) 5C180(9)	

FPGA/PLD PROGRAMMING SUPPORT (Continued)

Vendor	Product	Product Description	Module	Devices Supported				
				FLEXlogic	iPLD	85Cxxx	5Cxxx	5ACxx
SMS North America, Inc. P.O. Box 3159 Redmond, WA 98073-8447 (206) 883-8447 FAX (206) 883-8601 BBS (206) 867-5437	Sprint Expert	Univ. 48 Pin Driver Univ. programming support for microcontrollers, logic memory, and related devices	**DIP:** Top 40 or 48 **PLCC:** Top 3, Top 44 or Top 1		**DIP:** iPLD610 iPLD910 **PLCC:** iPLD610 iPLD910	**DIP:** 85C060, 85C090 85C220, 85C224 85C508 85C22V10 **PLCC:** 85C060, 85C090 85C220, 85C224 85C508 85C22V10	**DIP:** 5C031, 5C032 5C060, 5C090 5C121, 5C180 **PLCC:** 5C031, 5C032 5C060, 5C090 5C121, 5C180	**DIP:** 5AC31 5AC32 **PLCC:** 5AC31 5AC32
SMS GMBH Im Grund 15 D-88239 Wangen, Germany 49-7522-972810	Sprint Optima	Univ. 48 Pin Driver Univ. programming support for microcontrollers, logic memory, and related devices	**DIP:** Top 40 or 48 **PLCC:** Top 3, Top 44 or Top 1		**DIP:** iPLD610 iPLD910 **PLCC:** iPLD610 iPLD910	**DIP:** 85C060, 85C090 85C220, 85C224 85C508 85C22V10 **PLCC:** 85C060, 85C090 85C220, 85C224 85C508 85C22V10	**DIP:** 5C031, 5C032 5C060, 5C090 5C121, 5C180 **PLCC:** 5C031, 5C032 5C060, 5C090 5C121, 5C180	**DIP:** 5AC31 5AC32 **PLCC:** 5AC31 5AC32
	Multisite	Univ. 48 Pin Driver Univ. GANG	**DIP:** Top 40 or 48 **PLCC:** Top 3, Top 44 or Top 1		**DIP:** iPLD610 iPLD910 **PLCC:** iPLD610 iPLD910	**DIP:** 85C060, 85C090 85C220, 85C224 85C508 85C22V10 **PLCC:** 85C060, 85C090 85C220, 85C224 85C508 85C22V10	**DIP:** 5C031, 5C032 5C060, 5C090 5C121, 5C180 **PLCC:** 5C031, 5C032 5C060, 5C090 5C121, 5C180	**DIP:** 5AC31 5AC32 **PLCC:** 5AC31 5AC32

FPGA/PLD PROGRAMMING SUPPORT (Continued)

Vendor	Product	Product Description	Module	Devices Supported				
				FLEXlogic	iPLD	85Cxxx	5Cxxx	5ACxxx
SMS North America, Inc. (Continued) **SMS GMBH** (Continued)	Sprint Plus 48	Univ. 48 Pin Driver (Low Cost)	48 Pin Socket PLCC Adapters		**DIP:** iPLD610 iPLD910 **PLCC:** iPLD610 iPLD910	**DIP:** 85C060, 85C090 85C220, 85C224 85C508 85C22V10 **PLCC:** 85C060, 85C090 85C220, 85C224 85C508 85C22V10	**DIP:** 5C031, 5C032 5C060, 5C090 5C121, 5C180 **PLCC:** 5C031, 5C032 5C060, 5C090 5C121, 5C180	**DIP:** 5AC312 5AC324 **PLCC:** 5AC312 5AC324
Stag Microsystems, Inc. 1600 Wyatt Drive, Suite 3 Santa Clara, CA 95054 (408) 988-1118 FAX (408) 988-1232	ZL-30A	Logic 28 Pin + PLCC Adaptor	30A640				**DIP:** 5C031, 5C032 5C060, 5C090[10] **PLCC[10]:** 5C060, 5C090	**DIP:** 5AC312 **PLCC[10]:** 5AC312
	System 3000				**DIP:** iPLD610 iPLD910	**DIP:** 85C220, 85C224 85C060, 85C090	**DIP:** 5C031, 5C032 5C060, 5C090	**DIP:** 5AC312
	ZL30B	Univ. 28 Pin + PLCC (Larger Library)			**DIP:** iPLD610 iPLD910	**DIP:** 85C220, 85C224 85C22V10 85C060, 85C090	**DIP:** 5C031, 5C032 5C060, 5C090	**DIP:** 5AC312

FPGA/PLD PROGRAMMING SUPPORT (Continued)

Vendor	Product	Product Description	Module	Devices Supported				
				FLEXlogic	iPLD	85Cxxx	5Cxxx	5ACxxx
System General Corp. 510 S. Park Victoria Drive Milpitas, CA 95035 (408) 263-6667 FAX (408) 262-9227	TURPRO-1	Univ. 84-Pin Programmer	**PLCC Adaptor:** P28 P32 P44 P68 P84		**DIP:** iPLD610 iPLD910	**DIP:** 85C220, 85C224 85C060, 85C090 **PLCC:** 85C060, 85C090 85C220, 85C224 85C22V10	**DIP:** 5C031, 5C032 5C060, 5C090 **PLCC:** 5C031, 5C032 5C060, 5C090 5C180	**DIP:** 5AC312 5AC324 **PLCC:** 5AC312 5AC324
	TURPRO/FX	Univ. 84 Pin Programmer	**PLCC Adaptor:** P28 P32 P44 P68 P84		**DIP:** iPLD610 iPLD910	**DIP:** 85C220, 85C224 85C22V10 85C060, 85C090 **PLCC:** 85C060, 85C090 85C220, 85C224 85C22V10	**DIP:** 5C031, 5C032 5C060, 5C090 **PLCC:** 5C031, 5C032 5C060, 5C090 5C180	**DIP:** 5AC312 5AC324 **PLCC:** 5AC312 5AC324
Xeltek 757 North Pastoria Ave. Sunnyvale, CA 94086 (408) 524-1929 FAX (408) 245-7084	SUPERPRO	40-Pin Univ. Programmer				**DIP:** 85C060, 85C090 85C220, 85C224 85C22V10 **PLCC:** 85C060, 85C090 85C220, 85C224 85C22V10	**DIP:** 5C031, 5C032 5C060, 5C090 5C180 **PLCC:** 5C031, 5C032 5C060, 5C090 5C180	**DIP:** 5AC312 **PLCC:** 5AC312

NOTES:
1. With PX-20
2. With PX-28
3. With PX-44
4. With AM-1800
5. SITE 48 only
6. With OM-S-20 LCC
7. With OM-S-24 LCC
8. With OM-S-40 LCC
9. With OM-S-68 LCC
10. With 30A640
11. With AM-78

FPGA/PLD SOFTWARE SUPPORT

Vendor	Product	Features	Intel Kit	Devices Supported				
				FLEXlogic	iPLDxxx	85Cxxx	5Cxxx	5ACxxx
Cadence Design System 555 River Oaks Parkway San Jose, CA 95134 (408) 943-1234	Frameworks II 4.2.1	• Composer schematic capture • Verilog HDL using Synergy synthesis • Compilation • Timing simulation	FLEXlogic Plus Design Kit for Cadence	iFX780	iPLD610 iPLD910 iPLD22V10	85C220 85C224 85C22V10	5C032 5C060 5C090 5C180	5AC312 5AC324
Data I/O 10525 Willows Rd., NME PO Box 97046 Redmond, WA 98073-9746 (800) 247-5700 (206) 881-6444 FAX (206) 882-1043	Abel 4.3	• Abel design language • Compilation • State-machine entry • Partitioning • Simulation	PLDs supported in Abel; FLEXlogic supported by Intel FPGA/ PLD Fitter Kit	iFX780	iPLD610 iPLD910 iPLD22V10	85C220 85C224 85C22V10	5C032 5C060 5C090 5C180	5AC312 5AC324
	Abel 5.0	• Abel design language • Compilation • State-machine entry • Partitioning • Simulation • VHDL	PLDs supported in Abel; FLEXlogic supported by Intel FPGA/ PLD Fitter Kit	iFX780	iPLD610 iPLD910 iPLD22V10	85C220 85C224 85C22V10	5C032 5C060 5C090 5C180	5AC312 5AC324
Intel (see Sales Office and Distributor Listings at back of Handbook)	PLDshell Plus	• FPGA/PLD Compiler • Functional simulator • Merge function • Timing	N/A	iFX780	iPLD610 iPLD910 iPLD22V10	85C220 85C224 85C22V10	5C032 5C060 5C090 5C180	5AC312 5AC324

FPGA/PLD SOFTWARE SUPPORT (Continued)

Vendor	Product	Features	Intel Kit	Devices Supported				
				FLEXlogic	iPLDxxx	85Cxxx	5Cxxx	5ACxxx
ISDATA US/Canada: PO Box 19278 Oakland, CA 94619 (510) 531-8553 Non-US/Canada: Daimlerstr. 51 D-7500 Karlsruhe 21 Germany 721-751087	LOG/iC	• HINT VHDL synthesis • State View flow chart entry tool • Partitioner • Compiler	No kit necessary; Support included in vendor base tool.			85C220 85C224	5C031 5C032 5C060 5C090 5C180	5AC312
Logical Devices 692 S. Military Trail Deerfield Beach, FL 33442 1-800-331-7766	CUPL 4.4	• Compilation • Simulation	No kit necessary; Support included in vendor base tool.	iFX780	iPLD610 iPLD910 iPLD22V10	85C220 85C224 85C508	5C031 5C032 5C060 5C090 5C180	5AC312 5AC324
Logic Modeling 19500 NW Gibbs Dr. PO Box 310 Beaverton, OR 97075 1-800-344-0004	Smart Model	• Timing models for simulation		iFX780	iPLD610 iPLD910 iPLD22V10	85C220 85C224	5C031 5C032 5C060 5C090	5AC312 5AC324
Mentor 8005 SW Boeckman Rd. Wilsonville, OR 97070-777 (503) 685-7000	Falcon Framework 8.1	• Design Architect schematic capture • AutoLogic/ VHDL Synthesis • Compilation • Quicksim II timing simulation	FLEXlogic Plus Design Kit for Mentor	iFX780	iPLD610 iPLD910 iPLD22V10	85C220 85C224	5C031 5C032 5C060 5C090 5C180	5AC312 5AC324

FPGA/PLD SOFTWARE SUPPORT (Continued)

Vendor	Product	Features	Intel Kit	Devices Supported				
				FLEXlogic	iPLDxxx	85Cxxx	5Cxxx	5ACxxx
Minc, Inc. 6755 Earl Dr. Colorado Springs, CO 80918-1064 (719) 590-1155	PLDesigner v3.1	• Compilation • Simulation • VHDL • Partitioning	No kit necessary; Support included in vendor base tool.	iFX780	iPLD610 iPLD910 iPLD22V10	85C220 85C224 85C508	5C031 5C032 5C060 5C090 5C180	5AC312
OrCAD 3175 NW Aloclek Dr. Hillsboro, OR 97124-7135 (503) 690-9881	OrCAD PLD386+ 2.0	• OrCAD/SDT 386+ schematic capture • Compilation • OrCAD/VST simulation	No kit necessary; Support included in vendor base tool.	iFX780	iPLD610 iPLD910 iPLD22V10	85C220 85C224	5C031 5C032 5C060 5C090 5C180	5AC312 5AC324
Viewlogic 293 Boston Post Road W. Marlboro, MA 01752 (800) 223-8429	Workview 4.1	• Viewdraw schematic capture • Compilation • Viewsim timing simulation	FLEXlogic Plus Design Kit for Viewlogic	iFX780	iPLD610 iPLD910 iPLD22V10	85C220 85C224 85C508	5C031 5C032 5C060 5C090 5C180	5AC312 5AC324
	Workview Plus 5.1	• Viewdraw schematic capture • Compilation • Viewsim timing simulation	FLEXlogic Plus Design Kit for Viewlogic	iFX780	iPLD610 iPLD910 iPLD22V10	85C220 85C224	5C031 5C032 5C060 5C090 5C180	5AC312 5AC324
	Powerview 5.1	• Viewdraw schematic capture • Compilation • Viewsim timing simulation	FLEXlogic Plus Design Kit for Viewlogic	iFX780	iPLD610 iPLD910 iPLD22V10	85C220 85C224	5C031 5C032 5C060 5C090 5C180	5AC312 5AC324

FPGA/PLD SOFTWARE SUPPORT (Continued)

Vendor	Product	Features	Intel Kit	Devices Supported				
				FLEXlogic	iPLDxxx	85Cxxx	5Cxxx	5ACxxx
Viewlogic (Continued)	ViewPLD	• Workview schematic capture • Simulation • Abel compiler	Intel FPGA/PLD Fitter Kit for compilation; FLEXlogic Plus Design Kit for Viewlogic for timing simulation	iFX780	iPLD610 iPLD910 iPLD22V10	85C220 85C224	5C031 5C032 5C060 5C090 5C180	5AC312 5AC324
	Pro Series: Pro Sim	• Viewdraw schematic capture • Viewsim simulation • Waveform processing	FLEXlogic Plus Design Kit for Viewlogic; must buy EDIF reader from vendor to support timing simulation	iFX780	iPLD610 iPLD910 iPLD22V10	85C220 85C224	5C031 5C032 5C060 5C090 5C180	5AC312 5AC324
	Pro Series: Pro Developer	• Viewdraw schematic capture • Abel compiler • Viewsim Simulation/ waveform processing	FLEXlogic Plus Design Kit for Viewlogic; must buy EDIF reader from vendor to support timing simulation	iFX780	iPLD610 iPLD910 iPLD22V10	85C220 85C224	5C031 5C032 5C060 5C090 5C180	5AC312 5AC324

Intel			Data IO*				Logical Devices	
PLD	Packages	PLDshell Plus S/W	ABEL* S/W	UNISITE*	Model 2900	Model 29B LogicPak*	CUPL S/W	ALLPRO 40/88
85C220-100/80/66	D, P N, M	V3.1	V3.2	SITE40/48 (V2.8) CHIPSITE (V3.0)	V1.1 V1.1	303A-011A (V10) 303A-011B (V05)	V3.2	1.50c 1.50c
85C220-7/10	N	V3.1	V3.2	CHIPSITE (V3.0)	V1.1	303A-011B (V05)	V3.2	1.50c
85C224-100/80/66	D, P N, M	V3.1	V4.0	SITE40/48 (V3.1) CHIPSITE (V3.1)	V1.2 V1.2	303A-011A (V14) 303A-011B (V06)	V4.0	2.1 2.1
85C224-7/10	N	V3.1	V4.0	CHIPSITE (V3.1)	V1.2	303A-011B (V06)	V4.0	2.1
85C22V10	D, P N	V3.1	V4.2	SITE40/48 (V3.7) CHIPSITE (V3.7)	V1.8 V1.8	303A-011A (V18) 303A-011B (V08)	V4.0	— —
5AC312	D, P N, M	V3.1	V4.0	SITE40/48 (V2.2) PINSITE (V3.0)	V1.0 V1.1	303A-011A (V07) 303A-011B (V06)	V3.2	V1.48 V1.48
5AC324	D, P N	V3.1	V3.2	SITE40/48 (V3.2) PINSITE (V3.3)	V1.5 V1.5	n/s n/s	V3.2	V1.50 V1.50
5C031	D	V3.1	V3.0	SITE40/48 (V1.7)	V1.0	303A-011A (V02)	V2.15	V1.46
5C032	D, P	V3.1	V3.0	SITE40/48 (V1.2)	V1.0	303A-011A (V02)	V2.15	V1.46
5C060	D, P N, M	V3.1	V3.0	SITE40/48 (V2.7) CHIPSITE (V2.7)	V1.0 V1.1	303A-011A (V01) 303A-011B (V01)	V2.15	V1.46 V1.46
5C090	D, P N, M	V3.1	V3.0	SITE40/48 (V2.7) CHIPSITE (V2.7)	V1.0 V1.1	303A-010 (V03) 303A-010 (V03)	V2.50	V1.46 V1.46
5C180	N, M	V3.1	V3.0	CHIPSITE (V2.7)	n/s	n/s	V3.0	V1.46

↑ Model 3900: All devices supported with V1.2 (NOW)

NOTES:
n/s = Will not be supported due to hardware limitation.
*Data I/O = 1-800-3-DATAIO
Logical Devices = 1-800-331-7766

Intel			Data IO*				Logical Devices	
PLD	**Packages**	**PLDshell Plus S/W**	**ABEL* S/W**	**UNISITE***	**Model 2900**	**Model 29B LogicPak***	**CUPL S/W**	**ALLPRO 40/88**
FX780	KU N	V3.1	unknown	PINSITE (V4.3)	V3.1 V3.2	n/s	unknown	unknown
PLDLV22V10	P N	V3.1	unknown	SITE40/48 (V4.3) PINSITE (V4.3)	V3.2 V3.2	n/s	unknown	unknown
PLD22V10	P N	V3.1	V4.0(1)	SITE40/48 (V3.8) CHIPSITE (V3.8)	V1.9 V1.9	303A-010 (V18) 303A-010 (V08)	V4.0(1)	2.2 2.2
PLD610	P N	V3.1	V3.0(2)	SITE40/48 (V3.8) CHIPSITE (V3.8)	V1.9 V1.9	303A-011A (V14) 303A-011B (V06)(2)	V2.15(2)	2.2 2.2
PLD910	P N	V3.1(3)	V3.0(3)	SITE40/48 (V3.8) CHIPSITE (V3.8)	V1.9 V1.9	303A-010 (V03) 303A-010 (V03)(3)	V2.50(3)	2.2 2.2

↑
Model 3900: All devices supported with V1.2 (NOW)

NOTES:
1. Complete support provided as 85C22V10
2. Complete support provided as 85C060
3. Complete support provided as 85C090

n/s = Will not be supported due to hardware limitation.
*Data I/O = 1-800-3-DATAIO
Logical Devices = 1-800-331-7766

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CUPL and ALLPRO are trademarks of Logical Devices, Inc.

intel®

PLDshell Plus Design Software

- Easy-to-Use Design Environment for Programmable Logic Design Using Intel PLDs and the FLEXlogic Family of FPGAs
- Compiles PALASM* 2-Compatible Source Files into JEDEC Programming Files
- Functionally Simulates Designs Using Source File Simulation Syntax
- Test Vector and Waveform Viewer to Simplify Design Verification
- Easy-to-Learn Menu Interface with Extensive Help and On-Line Technical Support Information
- Editor and Programming Software Configurable to Designer's Preferred Tools
- Merges Multiple PDS Files into Single Device
- Estimates Design Fit Quickly to Narrow Target Device Choices
- Run Menu Configurable to Allow Use with Designer's Existing PLD Design Tools
- Utilities Disassemble/Convert Common PAL/GAL JEDEC Files into Source or JEDEC Files for Intel PLDs
- FLEXlogic Prototyping Cable Kit Available for Use with PLDshell Plus to Program Intel FPGAs
- Software and Programming Hardware Available through Intel Authorized Sales Office/Distributor
- Standalone Software (No Programming Hardware) Available Free from Intel Literature

4

INTRODUCTION

PLDshell Plus design software provides an easy-to-use menu system for programmable logic design that allows you to invoke Intel's PLDasm compiler/simulation software or your existing programmable logic compilers and programming software. Configure the menu system with the program and directory names of your existing programmable logic design tools and you are ready to run.

PLDshell Plus software includes Intel's PLDasm logic compiler/simulator software. PLDasm software compiles PALASM* 2-compatible source files to produce JEDEC files for Intel PLDs (Programmable Logic Devices) and FLEXlogic Family of FPGAs. Simulation syntax supports functional simulation and generation of test vectors for the JEDEC file. PLDasm software allows you to use a familiar design language to evaluate the architecture of Intel PLDs and FPGAs and to implement new designs.

*PALASM and PAL are registered trademarks of Advanced Micro Devices, Inc.
*GAL is a registered trademark of Lattice Semiconductor, Inc.

October 1993
Order Number: 290422-003

PLDshell Plus OVERVIEW

The PLDshell Plus Main Menu is arranged to follow the typical PLD design flow: Edit, Compile/Simulate, View, and Program. PLDshell Plus menu options allow you to:

Edit—Edit PLD source files (or any other text file) using your preferred ASCII text editor. You can configure the edit menu to invoke whatever text editor you have installed in your system via the **Change Editor** button.

Compile/Sim—Compile and/or simulate PLDasm source files to create JEDEC files for Intel PLDs using Intel's PLDasm software. You can define compile/simulate options such as logic minimization, DeMorgan's inversion, D/T register selection, pin assignment algorithm options, and event threshold for asynchronous events (during simulation).

View—View source, error, report, or simulation files to validate your design or quickly locate design or fitting problems. When viewing an error file, you can display on-line error message help information. Simulation results can be viewed in table or wave form. (Waveforms can be viewed on Hercules, EGA, or VGA monitors.)

Program—You can change the program menu to your preferred programming software via the **Change Programming S/W** button. For a complete list of supported programming vendors, refer to the Development Tools Support section of this book.

Run—Run up to 24 user-defined programs including other PLD development tools. The menu is user-defined, with each menu option including default command line options and working directories. You can also run any program via the **Run Other** submenu.

Utilities—Provides several utility functions, including:

Disassemble, allows you to disassemble JEDEC files for common PAL/GAL devices into PLDasm source files for Intel PLDs (JEDEC file to PDS file).

Convert, performs a full conversion (common PAL/GAL JEDEC file to Intel PLD JEDEC file).

Translate, translates Intel's iPLS II software into PDS files for use with PLDasm software.

Merge, allows you to combine multiple PDS files into a single Intel PLD or FPGA.

Change Directory, **List Directory**, or **Invoke DOS Shell**.

Modify Options to change the text editor, programming software, printer port, hot keys, and other options.

Databook—View datasheet briefs on Intel PLDs, FLEXlogic Family of FPGAs and technical notes on using the software/devices, device order codes, and other pertinent technical information.

PLDasm COMPILATION/SIMULATION

PLDasm software compiles PALASM 2-compatible source files to produce JEDEC files for Intel PLDs and FLEXlogic Family of FPGAs. The typical design process is to create the source file, compile/simulate the design to create a JEDEC file, and program devices. Error, report, and waveform files are viewed throughout the cycle. The edit/compile/simulate/view process is repeated until a design is working as desired. Devices are programmed at the end of the cycle. PLDshell Plus software also offers the ability to edit/simulation/view without "fitting". This allows you to concentrate on logic design first, then fit the working design into a device.

PLDasm software offers the following features:

- Preserves your investment in learning a PLD design language and in developing source files by compiling an industry-standard language.
- Implements designs using Boolean equations, State Machine syntax, or Truth Tables *(Truth Table design is a PLDasm superset feature)*.
- Functionally simulates designs.
- Estimates design fit quickly based on basic resource criteria.
- Maps designs into device resources and performs basic logic minimization.
- Generates JEDEC programming files; these files include programming test vectors based on simulation output.

You can compile PDS files for common PAL/GAL devices using PLDasm software. PAL/GAL designs are transparently converted into JEDEC files for the appropriate Intel PLD and FLEXlogic Family of FPGAs.

DESIGN MERGE

PLDshell Plus can merge multiple PDS design files into any Intel programmable logic device, including the Intel FLEXlogic family of FPGAs. The Merge function makes it easy for designers to consolidate multiple PLDs into a single, high-performance FPGA or PLD.

JEDEC DISASSEMBLY

PLDshell Plus provides the ability to disassemble existing JEDEC files for Intel PLDs and FLEXlogic Family of FPGAs, as well as for common 20-pin and 24-pin PALs and GALs into PLDasm source files. JEDEC disassembly allows you to reconstruct source files for existing designs where the original source files have been lost, or to generate source files from existing designs to be modified for new designs. JEDEC disassembly is available via the **Utilities—Disassemble** menu selections. Note that the source file output during the disassembly process using PAL/GAL JEDEC files is for the respective Intel PLD.

JEDEC CONVERSION

PLDshell Plus provides the ability to convert existing JEDEC files for common PALs/GALs into JEDEC files for Intel PLDs. A PLDasm source file is automatically generated during the conversion process. Conversion guarantees that the target Intel PLD is functionally the same as the original design. JEDEC conversion is available via the **Utilities—Convert** menu selections.

TRANSLATION

PLDshell Plus provides an automated path for users of Intel's iPLS II software to move to PLDshell Plus and make use of its more powerful simulation features and user interface. Translations is available via the **Utilities—Translate** menu selections.

SYSTEM REQUIREMENTS

PLDshell Plus is designed to work in systems configured as follows:

- Intel 386-based PC with 2 Mbytes of extended RAM
- MS-DOS V5.0 or later
- High-density (1.44 Mbytes) diskette drive
- Hard disk with approximately 5 Mbytes of space (4 Mbytes for installation; up to 1 Mbyte for working files while running).
- VGA monitor required for waveform viewing.

ORDERING INFORMATION

PLDshell Plus software (no programming hardware) is available from Intel Literature (1-800-548-4725) or your local Intel salesperson (order code #611942).

The FLEXlogic Prototyping Cable Kit includes the cable and software required to support in-circuit reconfiguration and programming of the Intel FLEXlogic Family. It's available through Intel authorized sales offices (order code #EVFX780CBL).

The FLEXlogic Evaluation Kit includes the FLEXlogic Prototyping cable and software, combined with the Intel Evaluation Board and PLDshell Plus. Available through Intel authorized sales offices (order code #EVFX780US). Versions for Europe and Japan are also available (#EVFX780E and #EVFX780J).

FLEXlogic PLUS DESIGN KITS

- Transparent to User—Works within Native CAE Vendor Environments
- Seamless Integration into the Cadence, Mentor or Viewlogic Frameworks
- Supports Vendor VHDL and Verilog Synthesis Tools
- Intel PLDasm Compiler for Optimal Fitting of Intel Architectures
- Complete Intel Design Synthesis and Primitives Libraries Provided
- Offers a Mix of Schematic and Textual Design Descriptions in One Design
- Accurate Device Timing Models Provided for Design Verification
- Technical Support Hotline Provided
- Supports Sun Sparc, HP-700 and Intel-Based 486 and Pentium™ PCs
- Reference and Tutorial User Guides Provided

INTRODUCTION

The Intel FLEXlogic Plus Design Kits are powerful yet well-integrated tools running under the most popular Computer Aided Engineering (CAE) environments: Cadence, Mentor and Viewlogic. As can be seen from the design flow diagram, Intel Design Kits are integrated completely within the normal design flow of your favorite CAE environment. This seamless connectivity makes the FLEXlogic Plus Design Kits easy to use, and eliminates time-consuming learning curve delays.

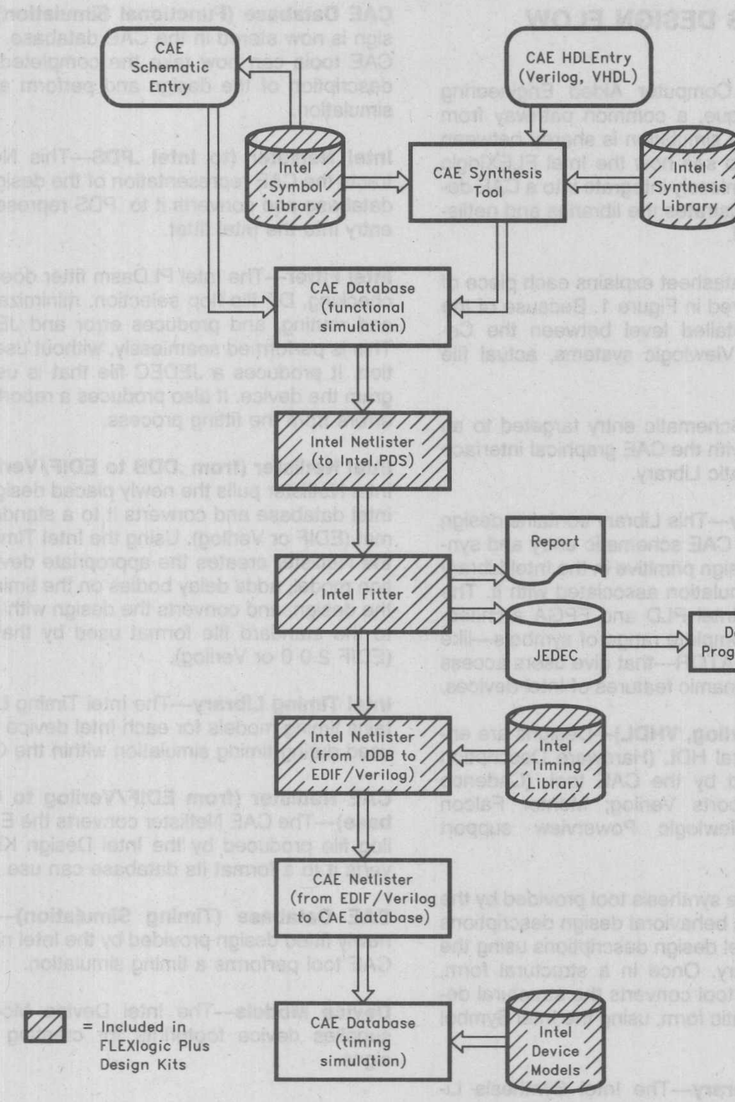
The Design Flow Diagram shows Intel's support for mixed style design entry, for functional and timing simulation, for parsing, minimizing and fitting, and for JEDEC file production. This datasheet details the following information about Intel's Design Kits:

—The overall design flow of FLEXlogic Plus at work within a CAE environment

—System requirements of the Intel Kits

—Order and technical support information

October 1993
Order Number: 290493-001



290493–1

Figure 1. Design Flow

4

DESCRIPTION

Even though each Computer Aided Engineering (CAE) system is unique, a common pathway from design entry to timing simulation is shared between most design tools. To see how the Intel FLEXlogic Plus Design Kits seamlessly integrate into a CAE design flow, Figure 1 illustrates the libraries and netlisters that are included.

This section of the datasheet explains each piece of the design flow pictured in Figure 1. Because of the differences on a detailed level between the Cadence, Mentor and Viewlogic systems, actual file names are not listed.

Schematic Entry—Schematic entry targeted to an Intel device is done with the CAE graphical interface and the Intel Schematic Library.

Intel Symbol Library—This Library contains design symbols used by the CAE schematic entry and synthesis tools. Each design primitive in the Intel Library has graphics and simulation associated with it. The Library supports all Intel PLD and FPGA architectures by offering a complete range of symbols—like SRAM and COMPARATOR—that give users access to the full range of dynamic features of Intel devices.

CAE HDL Entry (Verilog, VHDL)—Designs are entered in the behavioral HDL (Hardware Description Language) supported by the CAE tool. (Cadence Frameworks II supports Verilog; Mentor Falcon Framework and Viewlogic Powerview support VHDL.)

Synthesis Tool—The synthesis tool provided by the CAE vendor converts behavioral design descriptions to structural gate-level design descriptions using the Intel Synthesis Library. Once in a structural form, part of the synthesis tool converts the structural description to a schematic form, using the Intel Symbol Library.

Intel Synthesis Library—The Intel Synthesis Library contains structural descriptions of all gate-level symbols in the Symbol Library.

CAE tools can now take the completed gate-level description of the design and perform a functional simulation.

Intel Netlister (to Intel .PDS—This Netlister extracts the CAE representation of the design from the database and converts it to .PDS representation for entry into the Intel fitter.

Intel Fitter—The Intel PLDasm fitter does semantic checking, DT flip-flop selection, minimization, place and routing, and produces error and JEDEC files. This is performed seamlessly, without user intervention. It produces a JEDEC file that is used to program the device. It also produces a report file, listing errors from the fitting process.

Intel Netlister (from .DDB to EDIF/Verilog)—This Intel Netlister pulls the newly placed design from the Intel database and converts it to a standard file format (EDIF or Verilog). Using the Intel Timing Library, the Netlister creates the appropriate device simulation model, adds delay bodies on the timing paths of the design, and converts the design with timing data to the standard file format used by that CAE tool (EDIF 2 0 0 or Verilog).

Intel Timing Library—The Intel Timing Library contains timing models for each Intel device that will be used during timing simulation within the CAE tool.

CAE Netlister (from EDIF/Verilog to CAE database)—The CAE Netlister converts the EDIF or Verilog file produced by the Intel Design Kit and converts it to a format its database can use.

CAE Database (Timing Simulation)—Using the newly fitted design provided by the Intel netlister, the CAE tool performs a timing simulation.

Device Models—The Intel Device Model Library supplies device footprints for creating board designs.

SYSTEM REQUIREMENTS

Requirements:	Viewlogic	Cadence	Mentor
Platform	Sun Sparc Intel-based 486 PC	Sun Sparc	HP-700 Sun Sparc
Hardware:			
minimum	5 Mb	5 Mb	5 Mb
maximum	10 Mb	10 Mb	10 Mb
Memory	CAE requirements only	CAE requirements only	CAE requirements only
Software	Workview v4.1 Workview Plus v5.1 Powerview v5.1	Frameworks II v4.2.1	Falcon Framework v8.1
Distribution Media	QIC-24 tape, tar format 3.5″ diskettes (DOS)	QIC-24 tape, tar format	QIC-24 tape, tar format

ORDER AND TECHNICAL SUPPORT INFORMATION

Order FLEXlogic Plus Design Kits through the Intel Sales or Distribution Channels. A complete listing of offices can be found at the back of this handbook.

Technical support for the Design Kits is provided by the Intel Programmable Logic Hotline:

US/Canada:	1-800-628-8686 (916-356-3104)
Europe:	44-0-793-796977
Japan:	0298-47-8511

*For a complete list of the CAE tool functions that are supported, please see the Intel Third Party Tools Support Quick Reference Chart.

FPGA/PLD Fitter Kit

- Completely transparent to the user—continue to work within your preferred vendor environment
- Supports leading design tool vendors: Data I/O, Logical Devices, Minc and OrCAD
- Uses the Intel PLDasm fitter, providing the best fit for Intel FPGAs and PLDs
- Generates a working JEDEC file ready for programming
- Bundled into the vendor standard release† at no charge

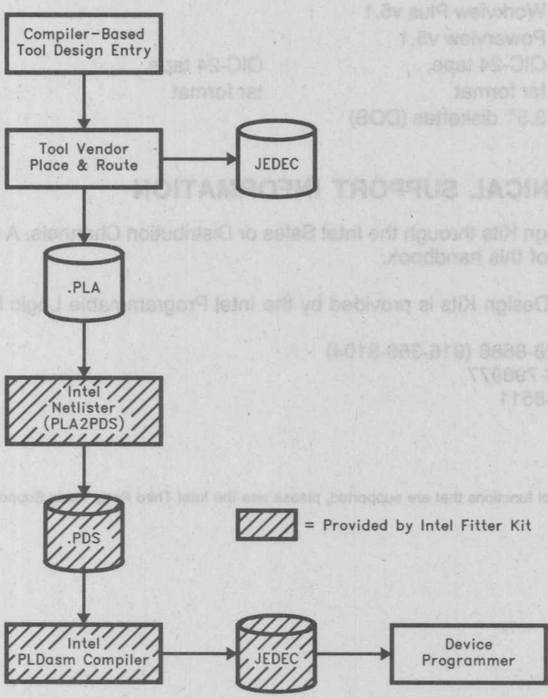


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Figure 1. High-Level Design Flow Diagram

NOTE:
†Abel support available through Intel hotline at no charge

November 1993
Order Number: 290506-001

The Intel FPSA/PLD Fitter Kits are tools that run under the most popular third-party, compiler-based design environments: Data I/O Abel, Logical Devices CUPL, OrCAD OrCAD-PLD 386+ and Minc PLDesigner-XL. This datasheet details their support for Intel devices in providing the following information:

— A high-level description of the design flow of compiler-based tools

— A detailed description of the design flow of each vendor's tool

— The vendor software version requirements and system requirements for support of Intel FPGAs

— Order and technical support information

HIGH LEVEL DESIGN FLOW DESCRIPTION

Vendor Tool Design Entry—As can be seen from the High-Level Design Flow Diagram (Figure 1), a design is entered using the compiler vendor design entry tool and then is passed to their fitter.

Vendor Place and Route—At this point there are two paths a design can take. Designs targeted at Intel PLDs are compiled within the vendor fitter and a JEDEC is produced, skipping the last half of the design flow.

.PLA File—Designs targeted at Intel FLEXlogic FPGAs are not compiled in the vendor fitter, but instead are converted to an industry-standard PLA file format.

Intel Netlister—Once in PLA format, the Intel Netlister converts the design to Intel's PDS language, launches the Intel PLDasm fitter and minimizes and compiles the design.

Intel PLDasm Compiler—After a successful compile, a JEDEC file is produced and an Intel FLEXlogic FPGA can be programmed.

The entire design flow process, from one fitter to another, is completely transparent to the user. All steps are conducted from within the familiar framework of your preferred design tool.

DETAILED DESIGN FLOW DESCRIPTION

The top four leading compiler-based design tool vendors that support Intel PLDs and FPGAs are Data I/O, Logical Devices, Minc and OrCAD. Even though each vendor handles the flow of a design through their system uniquely, the same overall process as described in Figure 1 is followed for each.

To take a detailed look at the design flow process requires an individual look at each of the four vendor's design tools. Figures 2–5 detail the design flow of each compiler-based design tool supporting Intel devices. As you can see, they follow the same approximate design flow as was discussed in the High-Level Design Flow Description, but with unique file listings, process names and report files.

After the PLA file is created, the Intel Netlister is invoked. The Netlister is a conversion tool which executes PLA2PDS, converting PLA files to the PDS format needed for the Intel compiler. Because the PLA output from each vendor varies slightly, the Intel Netlister for each vendor is unique.

Once the design is in PDS format, the Intel PLDasm compiler does syntax checking, DT flip-flop selection, minimizing, and place and routing. The PLDasm compiler offers the fastest place and route for an FPGA and the highest device utilization (>90%). After a successful fit, a JEDEC file is produced. In addition, a PDS representation of the final fitted design is produced, which can be used as a design entry file for several of the Intel CAE Design Kits to perform timing simulation.

Each compiler vendor supports various design entry features such as Boolean equations, truth tables, state diagrams, etc. The Intel Fitter Kits offer support for Intel FPGAs using your preferred design entry vendor. The Fitter Kits work seamlessly within the vendor environment, using Intel's fitter to provide the best fit for Intel devices. The Design Flow Diagram shows the simple design flow using the Fitter Kits, from the vendor design entry system through the Intel compiler and out to a JEDEC file.

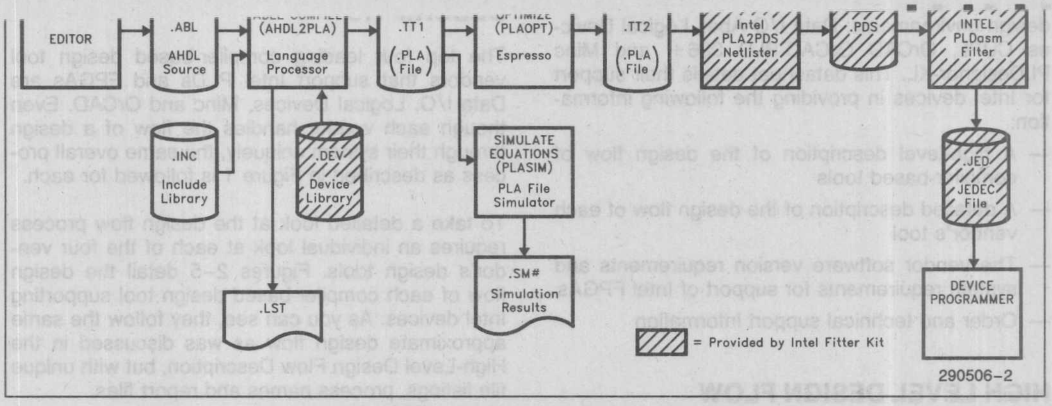

Figure 2. Intel-Data I/O Fitter Kit Design Flow Diagram

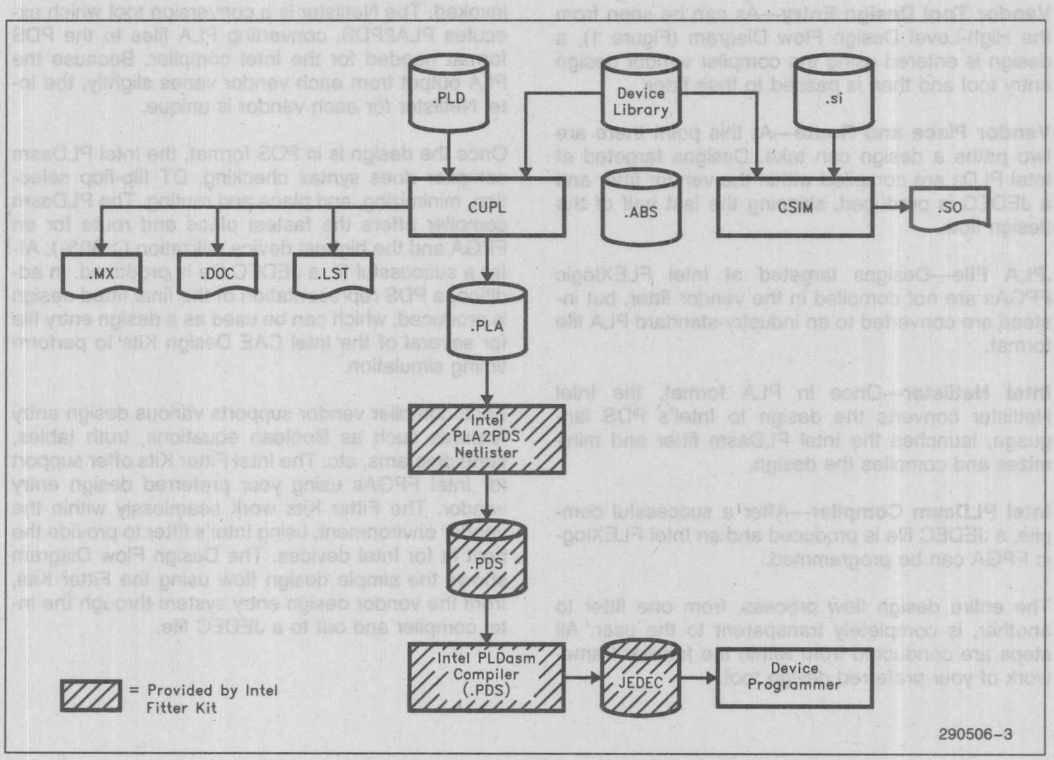

Figure 3. Intel-Logical Devices Fitter Kit Design Flow Diagram

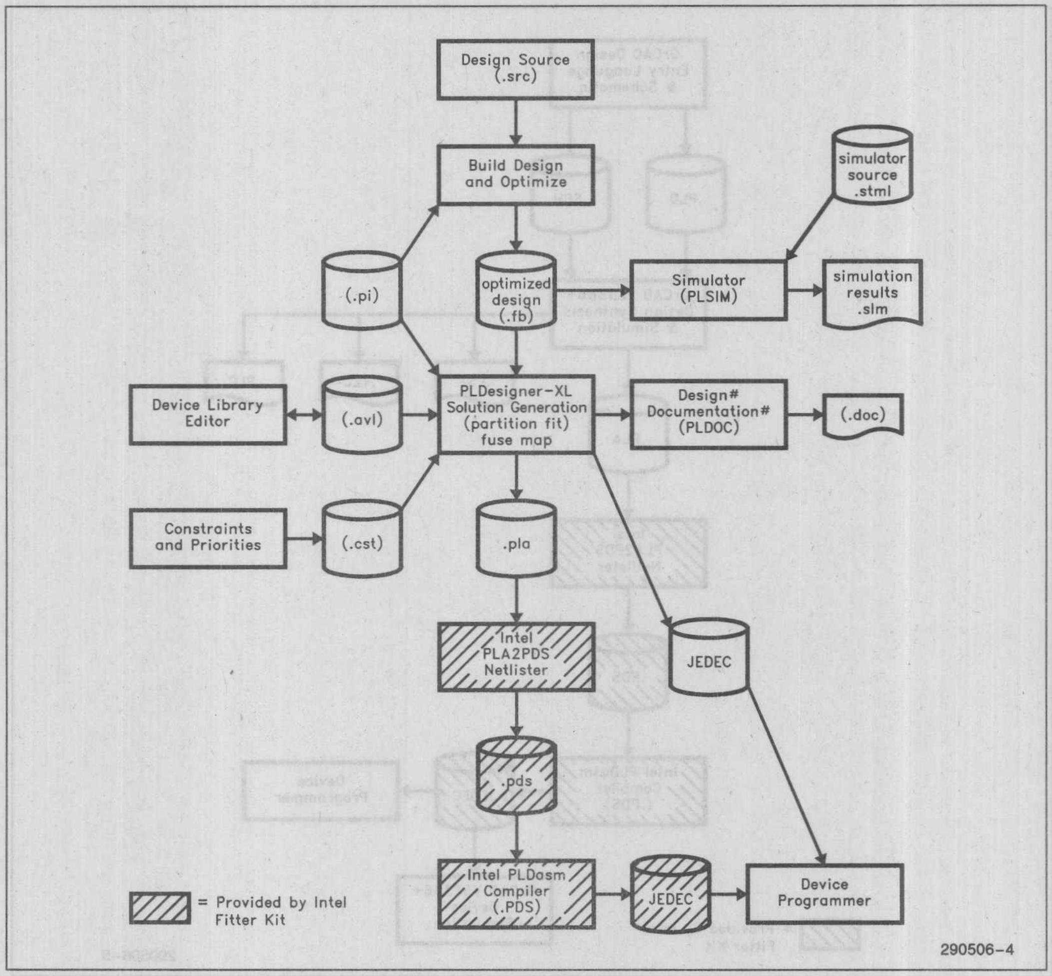

Figure 4. Intel-Minc Fitter Kit Design Flow Diagram

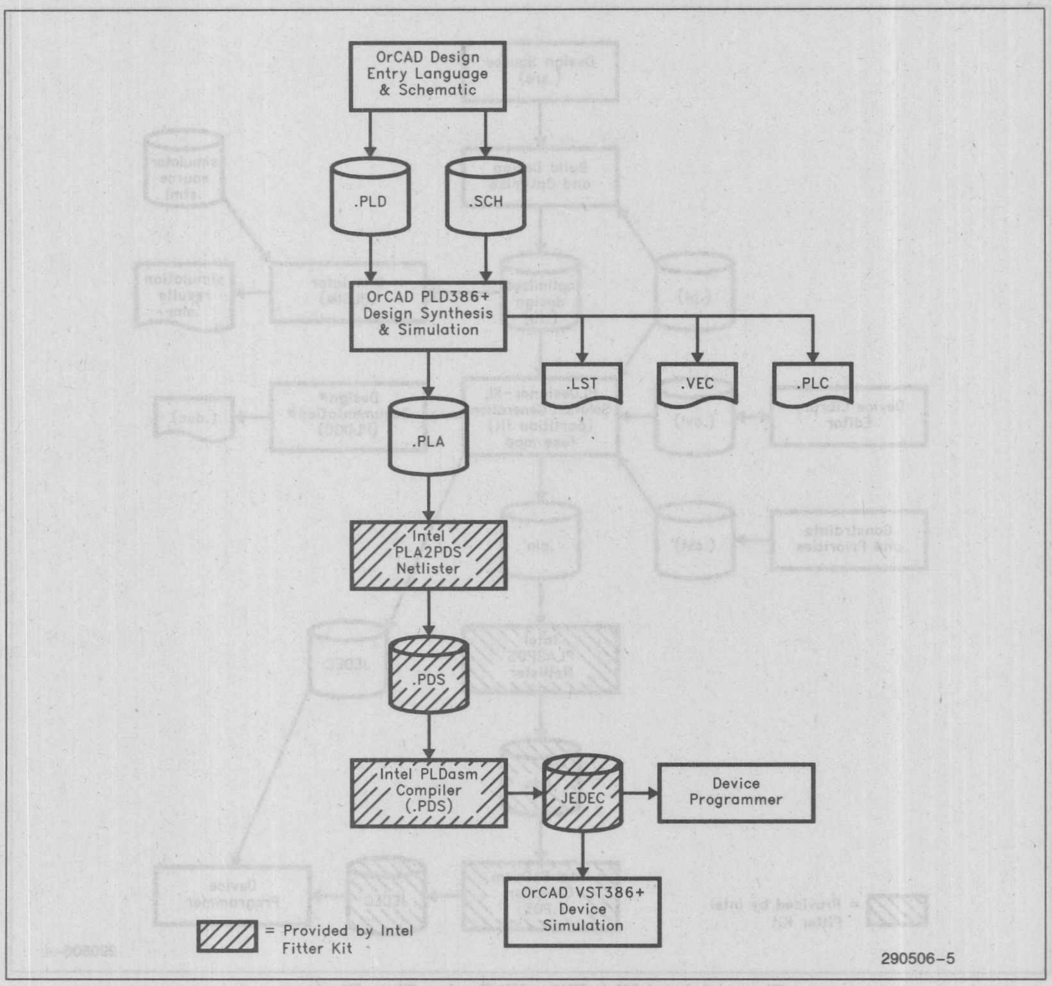

Figure 5. Intel-OrCAD Fitter Kit Design Flow Diagram

SYSTEM REQUIREMENTS/ TECHNICAL SUPPORT

For complete details on the system requirements for compiler-based design tools supporting Intel devices, please refer to the PLD/FPGA Vendor Software Support Chart in the Tools section of this Programmable Logic Handbook.

To receive the Open Abel Fitter Kit at no charge to you, call the Intel Hotline or BBS. All other Fitter Kits are available directly from the vendor at no charge.

PLDs & FPGAs

Personalizing PLD design work

By Jay Sturges
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Folsom, Calif.

Recent years have brought a spate of advances in PLD-development tools and their underlying technology, including the transition from device-dependent, restricted PLD design languages to device-independent, Boolean equation and finite state-machine design languages. An associated advancement is the integration of standard PLD development systems with major CAE vendor design environments. However, with all these improvements, there is still no intuitive PLD design tool set where a designer can achieve true universal PLD device and vendor support.

With hundreds of PLD architectures, made by dozens of IC vendors, it's not surprising that no single tool provides all the engineer's support. By the same token, a designer can't find a PLD design tool that can cover his various PLD design method and language requirements. Thus, engineers are forced to use multiple PLD tools to meet their needs and have additional learning requirements.

Currently, there are three distinct types of PLD-design tools—manufacturer-specific, universal and comprehensive. Each tool in these three categories offers the engineer some solutions to the development cycle. However, each has problems that lead the engineer to use more than one PLD-design tool.

Manufacturer-specific tools provide support for early development of new PLD architectures (before universal tools can bring up their support). By providing PLD tools, makers ensure that system-design engineers will have immediate development capability for their most-advanced PLD devices. Some manufacturers will even make this capability available prior to the availability of new PLD silicon.

In addition, manufacturer-specific tools will generally provide highly optimized support for their new PLD architectures. By using proprietary fitting, allocation and simulation technologies, PLD makers can optimize the design tools to best use their family of devices.

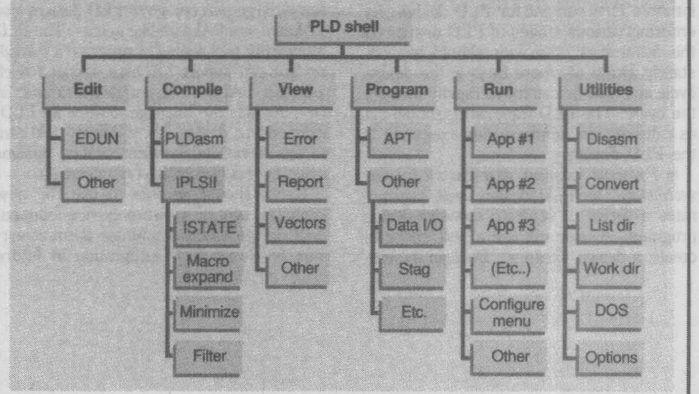
The downside to using manufacturer-specific tools is that they generally don't support the architectures of other PLD makers. They also incorporate new functionality (requiring additional learning) so that advanced device support can be optimized. As an example, optimal support for a complex device, such as Intel's 5AC312, requires the ability to "borrow" groups of logic in the device and "allocate" them as the user targets his design in the device.

The company's manufacturer-specific tool does this using software algorithms but requires the user to leave pin definitions unassigned. Many users will not take advantage of this capability, because the other tools they employ require pin assignment prior to use. So, to use the tool, a change in PLD design method as compared with other PLD design tools is required.

Universal PLD tool vendors provide tools offering a level of PLD device and vendor independence. Universal vendors promote device-independent systems, sometimes including languages with higher levels of abstraction and partitioning algorithms. Their support includes as large a list of PLD manufacturers as possible. This gives the system design engineer the ability to select from a large list of PLD devices and vendors. Yet, trying to support a large list of architecturally different PLDs means that support for particular devices, including the most advanced ones, is commonly sacrificed.

Among the most comprehensive PLD tools are those supplied by major CAE vendors, who provide an entire design methodology integrating universal and manufacturer-specific PLD tools, as well as other semicustom capabilities. They try to solve design problems by providing a complete electronic design automation (EDA) methodology. Typically referred to as frameworks, these solutions are supported by alliances between the CAE vendors and manufacturer-specific and/or universal PLD tool vendors.

PLD shell default and user-configurable features



these alliances are generally limited to a small number of vendors. An engineer can't always get the tool set he requires within the framework. Furthermore, the costs of using these frameworks is often very high in both dollar outlays and engineer training.

For each of the three PLD-tool types, shortcomings exist for providing universal, low-cost support for the design of PLDs.

This introduces an idea for a new class of PLD tools: a PLD micro-framework. Such a tool should be built around the theme of letting the engineer "have it his way." It should provide a workbench for PLD development, providing design engineers with a way to integrate different PLD tools, methods and languages. It should be structured around an intuitive user interface.

The PLD micro-framework should provide a generic environment for editing, compiling, viewing, simulating, programming and even disassembling ID. These are the steps needed to generate a PLD design, independent of the PLD device or vendor selected. Within each of these steps, the engineer should be able to configure the programs he runs to his individual needs. There are a few requirements of a PLD micro-framework software design package:

- *Consistent user interface*: The tool should try to minimize the user's learning curve for incorporating new PLD capabilities by presenting users with a consistent, intuitive environment for PLD design. By entering various stages of PLD design via the framework, the user should be constantly aware of where he is in the design cycle and how he can move rapidly through the cycle. The PLD framework should act as a dispatcher, administering execution of the PLD design.

- *Preserve existing user-knowledge investment*: The PLD design cycle incorporates a series of separate software-design programs. A user will use a text editor to create a design file (e.g., Boolean expressions), a compiler to translate the design file into a target device (e.g., minimize Boolean equations, produce Jedec programming files). After completing the design, the engineer will program the file into a target device.

The user may use different vendors for each of the programs. As an example, an AEDIT text editor, Intel PLD compiler (iPLS), and Data I/O programmer (e.g., Unisite) may be chosen. For each of these systems, an investment has been made in training. The framework should allow these investments to be preserved. This should be made possible by enabling the user to configure the framework for editing, compiling and programming software.

- *Allow integration of multiple-PLD compilers*: There's a constant stream of new PLD design tools (manufacturer-specific) to support new PLD devices. These enable fast time-to-market for support of new PLD products. These also can offer more optimum device utilization than can universal tools. The framework should provide an environment for running many different PLD compiler programs.

Users should be able to quickly add and inventory PLD tools from both manufacturer-specific and universal vendors. This would result in the ability of design engineers to move easily between different types of design tools to incorporate new PLD devices and better optimize their individual PLD designs.

- *Import and upgrade the PALasm syntax*: A large percentage of PLD designs use PALasm or a PALasm-like syntax. The PLD framework tool should incorporate a compiler that can import PALasm syntax (which assumes PALs as target devices) and, in fact, upgrade the language to allow for PLD-independent design. By migrating PALasm to this device-independent syntax, designs could be easily migrated between ID.

Users should be able to use the new language syntax to store device-independent design modules and use them at various levels of PLD integration in future port PALasm syntax, mobility would exist between these tools.

- *Additional PLD design utilities*: The framework should include the ability to disassemble Jedec files into source, view files quickly and move easily within the DOS environment. The disassemble utility would allow engineers to identify functionality of ID without source files readily accessible. By reading a device's Jedec pattern (for example, from a programmer), the designer can disassemble the Jedec into a source file that includes the Boolean representation of functionality.

Intel is now providing a tool aimed at filling the needs outlined above. The company's PLDshell program provides a new capability in PLD tools. It provides the micro-framework outlined above for PLD design. It includes a user interface tailored specifically for the PLD design engineer. Within this interface, the user can customize editors, compilers and programming environments to preserve past investment in learning (see figure).

Additional capability also has been provided specifically for PLD design. A new PLDasm compiler is included that allows new capabilities in a very familiar format. The user can upgrade designs initially targeted for PALs to use the advanced capabilities available in newer PLD devices. PALasm files can also be imported. Moreover, users can recover design information by disassembling existing Jedec files.

Since 1988, Jay Sturges has worked as a senior software engineer for Intel's programmable logic focus group. He has been involved in CAD and CAE for the past 10 years. Prior to Intel, he helped create SuperCads, a small development company in northern California.

Appendix 5

5

PAL*/GAL* to Intel PLD Replacement

Already in wide use throughout the electronics industry are numerous different Programmable Logic Devices. Most common PALs and GALs can be replaced or upgraded with the following Intel PLDs:

85C220

The 85C220 is a direct, drop-in replacement for most 20-pin PALs/GALs, although some PALs have an incompatible architecture. The 85C220 runs at 80 MHz with external feedback. 85C220 to 20V8 cross programming is now available through the cross programming menu on Data IO's Unisite, Autosite 2900 and 3900 programmers.

85C220 As a 20-Pin PAL Replacement

100% Compatible	
10H8, -2	16R6A
12H6, -2	16R4A
14H4, -2	16L8A
16H2, -2	16RP6A
10L8, -2	16RP4A
12L6, -2	16P8A
16L8, A-2, A-4	16R8A
16R4, A-2, A-4	16RP8A
14L4, -2	16V8A
16L2, -2	18P8
16R8, A-2, A-4	18V8
16R6, A-2, A-4	
16P8, -2	
16RP8, -2	
16RP6, -2	
16RP4, -2	
16V8	

85C224

The 85C224 is a direct, drop-in replacement for most 24-pin PALs/GALs, although some PALS have an incompatible architecture. The 85C224 runs at 80 MHz with external feedback. 85C220 to 20V8 cross programming is now available through Data IO's Unisite, Autosite 2900 and 3900 programmers.

85C224 As a 24-Pin PAL Replacement

100% Compatible	
14L8	20L8A
16L6	20R8A
18L4	20R6A
20L2	20R4A
20L8	20V8
20R8	
20R6	
20R4	

iPLD22V10

The iPLD22V10 is 100% pin-, function- and JEDEC-compatible with industry standard 22V10 devices. JEDEC files developed for 22V10 devices can be used "as is" to program the iPLD22V10.

iPLD22V10 As a 22V10 PAL/GAL Replacement

100% Compatible	
AmPAL22V10	PALC22V10L
AmPAL22V10A	GAL22V10
PAL22V10	GAL22V10B
PALCE22V10H	PAL20L10A
PAL22V10C	PAL20L10
PAL22VP10C	TIBPAL22V10A
PALC22V10	TIBPAL22V10
PALC22V10B	TIBPAL22VP10

*PAL is a registered trademark of Advanced Micro Devices.
*GAL is a registered trademark of Lattice Semiconductor, Incorporated.

The 5C031

The 5C031 is a direct, drop-in replacement for most 20-pin PALs, although some PALs have an inpcompatible architecture.

5C031/5C032 As a 20-Pin PAL Replacement

100% Compatible	Functionally Compatible
10H8, -2	
12H6, -2	
14H4, -2	
16H2, -2	
10L8, -2	
12H6, -2	16R6A
16L8, A-2, A-4	16R4A
16R4, A-2, A-4	16R8A
14L4, -2	16RP6A
16L2, -2	16RP6A
16R8, A-2, A-4	16P6A
16R6, A-2, A-4	16R8A
16P8, -2	16RP8A
16RP8, -2	
16RP6, -2	
16RP4, -2	
16V8	
These are 25 ns–45 ns PALs	These are 15 ns PALs

The 5AC312

The 5AC312 is a direct, drop-in replacement for the 20RA10 as well as many of the other simple 24-pin logic devices. The 5AC312 can also serve as a drop-in replacement for most designs using the 22V10 or 32V10 devices.

5AC312 As a 24-Pin PAL Replacement

100% Compatible	100% Compatible (Qualified)
20LB 20R8 20R6 20R4 20RA10	22V10 32V10 Dependent on the number of product terms used.

Intel PLD and FPGA Feature Comparison

		85C220									
	5C031	5C032	85C224	iPLD22V10	iPLD610	iPLD910	5C180	5AC312	5AC324	iFX780	iFX740
INPUTS											
Dedicated	10	10	14	12	4	12	12	10	12	22	10
Maximum	18	18	22	22	20	36	60	22	36	102	50
Input Latches/Registers								Y	Y	N	N
I/O											
Number	8	8	8	10	16	24	48	12	24	80	40
Tri-State	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
Programmable Polarity	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
Dual-Feedback								Y	Y	Y	Y
MACROCELLS	8	8	8	10	16	24	48	12	24	80	40
REGISTERS											
Number	8	8	8	10	16	24	48	12	24	80	40
Types	D	D	D	D	D/T/ RS/JK	D/T/ RS/JK	D/T/ RS/JK	D/T/ RS/JK	D/T/ RS/JK	D/T/ RS/JK	D/T/ RS/JK
By-Pass	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
Reset to 0	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
Preset to 1	Y							Y	Y	Y	Y
PRODUCT TERMS											
Number	74	72	72	92	160	240	480	200	394	480	240
Allocation								Y	Y	Y	Y
LOCAL/GLOBAL BUSES							Y				
GLOBAL CLOCK PINS	1	1	1	1	2	2	4	2	2	2	2
Asynchronous Clocking					Y	Y	Y	Y	Y	Y	Y
SECURITY BIT	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
TURBO BIT (Standby Mode)	Y	Y	Y	N	Y	Y	Y	Y	Y	N	N

5

Industrial Temperature Devices

Intel offers industrial temperature PLDs. Unless otherwise specified, commercial temperature specifications apply to industrial temperature devices. The table below lists the industrial temperature devices.

Device	Package	Speeds	Order as
5C032	D, P	35, 40	TD5C032-35 TD5C032-40 TP5C032-35 TP5C032-40
5C060	D, N, P	45, 55	TD5C060-45 TN5C060-45 TP5C060-45 TD5C060-55 TN5C060-55 TP5C060-55
5C090	D, N, P	50, 60	TN5C090-50 TD5C090-60 TN5C090-60 TP5C090-60
5C180	N	75, 90	TN5C180-75 TN5C180-90
5AC312	D, N	30	TN5AC312-30
5AC324	N	30	TN5AC324-30
85C220	D, N	66	TD85C220-66 TN85C220-66
PLD22V10	D, N, P	15	TDPLD22V10-15 TNPLD22V10-15 TPPLD22V10-15
PLD610	D, N	12, 15, 25	TNPLD610-12 TDPLD610-15 TNPLD610-15 TDPLD610-25 TNPLD610-25
PLD910	D, N	12, 15, 25	TNPLD910-12 TDPLD910-15 TNPLD910-15 TDPLD910-25 TNPLD910-25

Military Devices

Intel offers the following military PLDs.

Device	Package	Speeds	Order as
5C060	D	55	MD5C060-55
5C090	D	60	MD5C090-60
5C180	A, K	90	MG5C180-90 MQ5C180-90
5AC312	D	35	ME5AC312-35
85C220	D	50, 66	MD85C220-50 MD85C220-66
85C224	D	50, 66	MD85C224-50 MD85C224-66
PLD22V10	D	10, 15, 20	MDPLD22V10-10 MDPLD22V10-15 MDPLD22V10-20
PLD610	D	15, 25, 35	MDPLD610-15 MDPLD610-25 MDPLD610-35
PLD910	D	20, 25, 30	MDPLD910-20 MDPLD910-25 MDPLD910-30

For detailed information on military devices, refer to the *Military Products Handbook,* Order Number 210461.

Tape and Reel Packaging

Intel offers tape and reel packaging of PLCC devices.

Please contact your local Intel sales representative for details.

Pre-Programmed Devices

Intel has the capability of providing pre-programmed and specially tested devices. Please contact your local Intel sales representative for details.

Register Preload

Most Intel PLD macrocell registers can be preloaded with any pattern to allow testing of all possible logic states. Information on register preload for test purposes is available from Intel.

Ordering Information

Intel PLDs and FPGAs are identified as follows:

```
M   D   5   C   X   X   X   -   S   S
                \___Device___/      \_Speed_/

Family
    FX - FLEXlogic FPGA (Field Programmable Gate Array)
   PLD - Industry Standard Architecture
   85C - High Speed Enhanced Architecture PLD
   5AC - Advanced Architecture PLD
    5C - Standard Architecture PLD
Package Type
    D - Hermetic, Type D (Cerdip) DIP
    N - Plastic, Leaded Chip Carrier
    P - Plastic Dip and Plastic Flatpack
    X - Unpackaged Device
   KU - Plastic Quad Flat Pack
```

000273–1

A — Indicates automotive operating temperature range (−40°C to +125°C)

J — Indicates a JAN qualified device, but is for internal identification purposes only. All JAN devices must be ordered by M38510 part number. (Example: M38510/42001 BQB), and will be marked in accordance with MIL-M-38510 specifications.

L — Indicates extended operating temperature range (−40°C to +85°C) express product with 160 + 8 hrs. dynamic burn-in.

*M — Indicates military operating temperature range (−55°C to +125°C)

Q — Indicates commercial temperature range (0°C to +70°C) express product with 160 + 8 hrs. dynamic burn-in.

T — Indicates extended temperature range (−40°C to +85°C) express product without burn-in.

— No letter indicates commercial temperature range (0°C to +70°C) without burn-in.

Examples:

QD5C060-45 Commercial with burn-in, ceramic Dip, 060 (600 gate) device, 45 nanosecond.

*On military temperature devices, B suffix indicates MIL-STD-883C level B processing.

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